These schematics use 74HCT but most components can be replaced directly with either 74LS or 74HC. Two notes to keep in mind: (1) 74LS uses more power and has lower V_{OH}. E.g., when replacing the OUT register with 74LS, adjust the RGB resistors accordingly. (2) For the clock 74HCT always gives the most desirable duty cycle and reliability.

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Sheet: / File: Gigatron.sch
Title: Gigatron TTL microcomputer
Size: 44 Date: 2020-03-20
Rev: Release
Edit Ed.4, Head 4.0.6 Id: 1/8
Multilayer F1 helps protect the upstream power supply against faults/shorts in the computer (e.g. those caused by build errors or abuse).

A decoupling (or bypass) capacitor in close proximity to every IC's power pin provides transient current when switching between logic levels.

Zener diode D1 protects the circuit against reverse current and overvoltage.

The 0.7pf of C3 provides an additional CLE2-CLE1 shift of 5ns, which is required when using the original 70ns SRAM at 6.25MHz, or when overclocking in general. It is not needed when using a 55ns SRAM module at 6.25MHz.

1. Power comes from the +5V that a USB charger provides. The data lines are not used.
2. The oscillator generates 6.25MHz square waves. The HCT-Inverter gives a long 2nd clock phase. This is useful for the /WE pulse derived from it. (3) The Power-On Reset (POR) supervisory Circuit holds /RESET low for 350ms during power up and brown outs.

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Sheet: FCR
File: FCR.sch

Title: Gigatron Power, Clock and Reset
Size: 44 Date: 2020-03-20 Rev: Release
Ered E.D. Head 4.0.6 Id: 2/8
The 16-bit program counter (PC) normally increments by one for every clock cycle. Conditional branches can go to any location within the current 256-word page. Unconditional jumps go to any location in program memory. When there is no branching, the memory space is linear and PC will cross page boundaries.

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Sheet: PRG
File: PRG.ch

Title: Gigatran Instruction Fetch
Size: 44
Date: 2020-03-20
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Ed. B.A. 4.0.6
Id: 3/8
This unit is the equivalent of two large 4-bit 74181 ALU chips that were at the heart of many 1970s minicomputers. This design is inspired by Dieter Hueller’s excellent notes starting from http://6502.org/users/dieter/a1/a1_4.htm

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Sheet: ALU
File: ALUgray

Title: Gigatron Arithmetic and Logic Unit
Size: 44 Date: 2020-03-20 Rev: Release
File ed: 4.0.6

Each of the eight logic unit packages contains two 4:1 multiplexers we call L and R. R is fully programmable by the truth table hosted in the control unit (AR0/3). It performs logic functions on both accumulator (A) and bus data (B). L will either be zero or the value of the accumulator. Therefore it needs just one control line (AL).

The stage with two 4-bit adders combines L and R for a final result. The table lists resulting operations that we use.

During jump instructions, ‘A’ is computed so that the carry out (CO) indicates if the accumulator is zero.
During store instructions, ‘A’ is ‘computed’ so that, depending on addressing mode, the accumulator can be copied to X or Y as well.
Besides PC there are four user registers: AC, X, Y and OUT. Each has 8-bits.
AC is the accumulator for calculations, X and Y are used to form memory addresses.
Y is also used by the JMP instruction. OUT is the primary output register.
Only AC can write back to the bus and memory, the others are effectively write-only.

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Sheet: PEG
File: PEG.sch

Title: Gigatron User Registers

Size: 44  Date: 2020-03-20  Rev: Release
File: EDA. H1cd 4.0.6  Id: 7/8