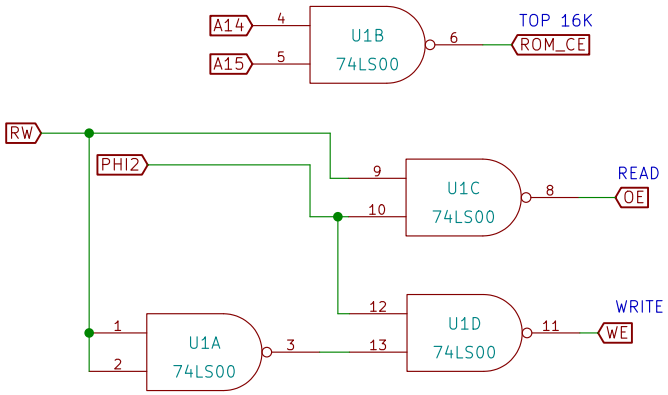
A simple address decoder block, giving 16k ROM and 32k RAM. RAM/ROM decoding circuit is based off Grant Searle's simple 6502 computer: http://zx80.netai.net/grant/6502/Simple6502.html
One benefit of this decoding scheme is that it has a very low propagation delay (meaning the address decoding signals only go through one set of logic blocks to reach their intended targets)

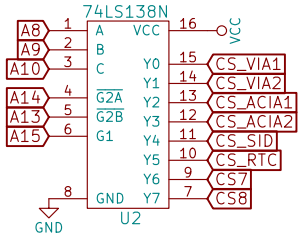
NOTE: You can substitute the 74LS logic chips with 74HC or 74AC (or HCT/ACT for TTL logic compatibility) to further lower the propagation delay of this block.

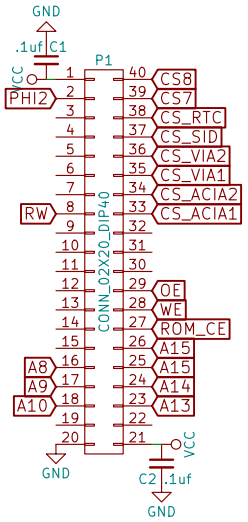
NOTE: PHI2 input isn't needed on chip select/peripheral decoding logic. This is because the PHI2 has already been accounted for in the read/write sequence during RAM/ROM decoding.

RAM/ROM DECODING



PERIPHERAL DECODING





Memory Map

RAM START: ($0000) = 0000 0000 0000 0000
RAM END: ($7FFF) = 0111 1111 1111 1111
VIA1: ($8000) = 1000 0000 0000 0000
VIA2: ($8100) = 1000 0001 0000 0000
ACIA1: ($8200) = 1000 0010 0000 0000
ACIA2: ($8300) = 1000 0011 0000 0000
SID: ($8400) = 1000 0100 0000 0000
RTC: ($8500) = 1000 0101 0000 0000
CS7: ($8600) = 1000 0110 0000 0000
CS8: ($8700) = 1000 0111 0000 0000
ROM START: ($C000) = 1100 0000 0000 0000
ROM END: ($FFFF) = 1111 1111 1111 1111

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