CPLDuino v0.4.5

Reference Manual

XCACDV45 April 23, 2015

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CPLDuino v0.4.5 Reference Manual

Overview

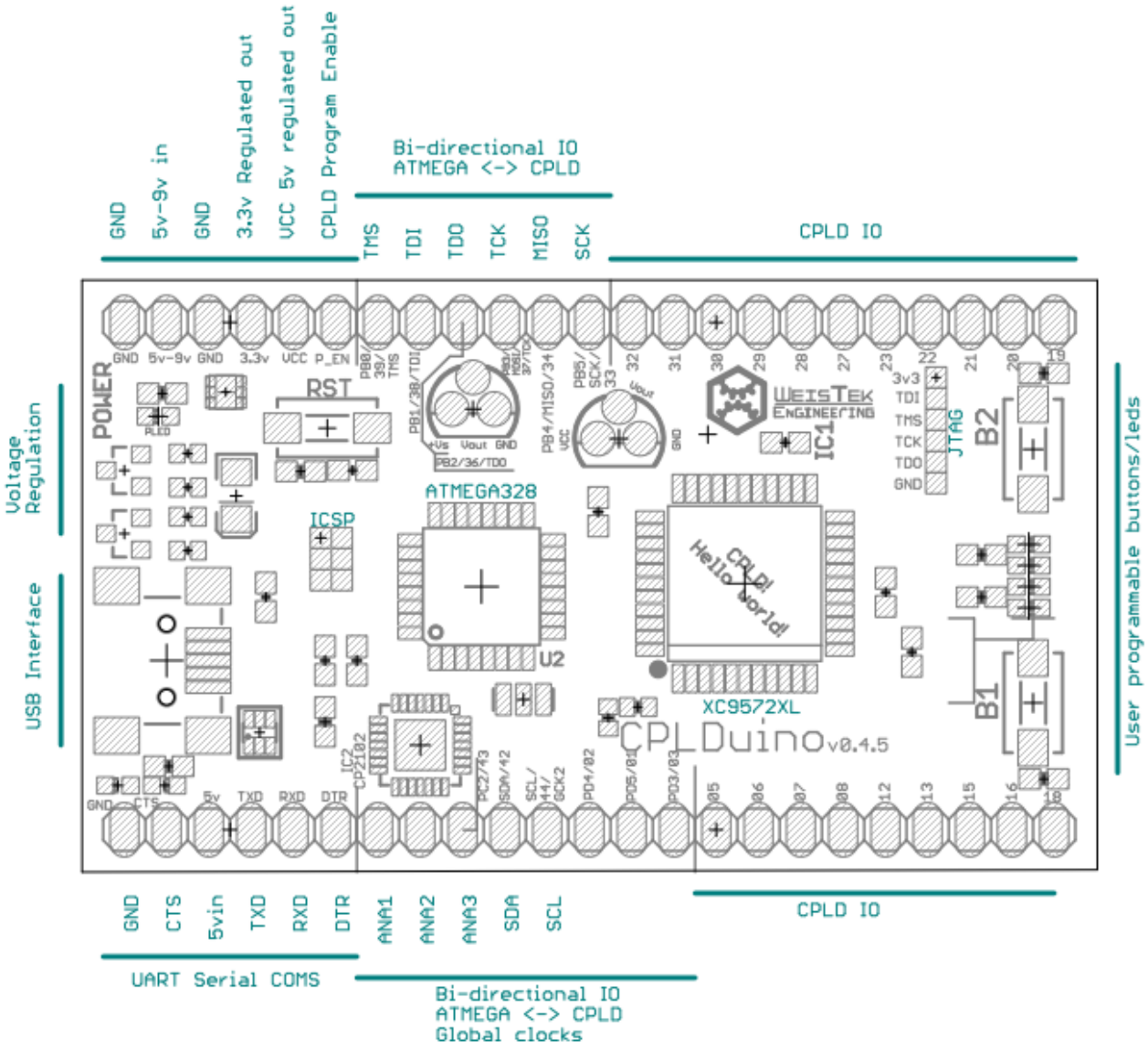
The XCACDV3, CPLDuino is a single board solution to meld Atmels ATmega 328 RISC microcontroller with a Xilinx XC9536XL[1] CPLD. Allowing for rapid prototyping of digital circuits without the need for a breadboard. The CPLDuino is capable of passing information from the on board ATMega328 to the CPLD and vice versa, allowing for real-time data monitoring. Thanks to the on-board CP2102 USB to Serial UART, data can be viewed and manipulated via the virtual com port.

Board features include:

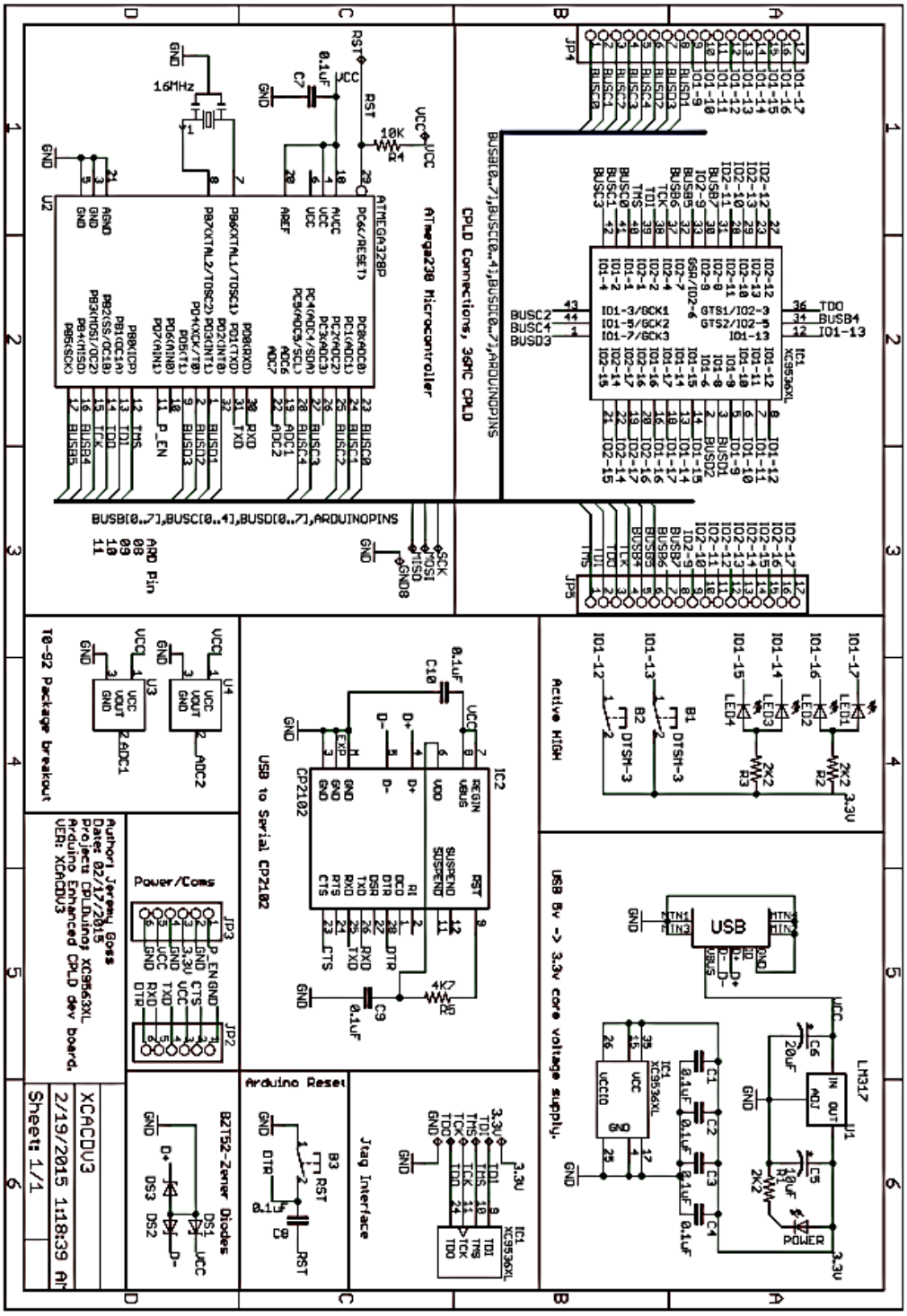
- On-board USB→UART controller (CP2102) and mini USB connector providing board power and programming.
- On-board voltage regulation 5v & 3.3v, broke out to .1" spaced headers
- Multiple programming options include, USB, UART broke out to .1" spaced headers, ICSP header, Jtag header.
- On board ATmega 328 8 bit microcontroller 32Kbytes in-system self-programmable flash program memory, 2Kbytes internal SRAM, 1Kbytes EEPROM, with 14 I/O's broke out to .1" spaced headers and directly connected to the XC9572XL CPLD.
- 3 I/O's connected directly to the CPLD's GCK1,2,3 pins for custom clock configurations.
- Two standard T0-92 type unpopulated package connections for use with various sensors.
- XC9572XL 36 MacroCell 3.3v core, 5v tolerant I/O Xilinx CPLD
- 2 user programmable buttons connected to the XC9536XL I/O's
- 4 user programmable LED's connected to the XC9536XL I/O's

[1] XC9572XL for board version .4.5

Board Overview: Basic View



Board Schematic



Required Software & Installation.

Arduino compatible IDE, the Arduino IDE can be obtained from www.arduino.org.

For the CPLDuino v0.4.5 we recommend Xilinx ISE 14.7 to create the required VHDL and or schematic diagrams that iMPACT will use to create the .xvf file for programming the CPLD.

If you are installing Xilinx 14.7[2] on Windows 8.1 operating system please see the notes section at the end of this document for installing the ISE on Windows 8.1 operating systems.

To use the CPLDuino v0.4.5 development board with the Arduino IDE. Make sure the CPLD P_EN pen is not jumped to ground leave this pin floating or connect the pin to VCC, then simply select your com port and under boards selection select ArduinoUNO and code away.

You will also need a custom avrdude.conf[3].

To program the CPLD you will need BitTwiddler in order to talk to the CPLD on board, make sure the CPLD P_EN pin is jumped to VCC (Held HIGH). This tells the bootloader that you wish to program the CPLD.

[Small tutorial for BitTwiddler program, in progress].

[2] See notes section for instruction installing Xilinx ISE 14.7 on Windows 8.1
[3] See notes section on how to obtain the custom avrdude.conf

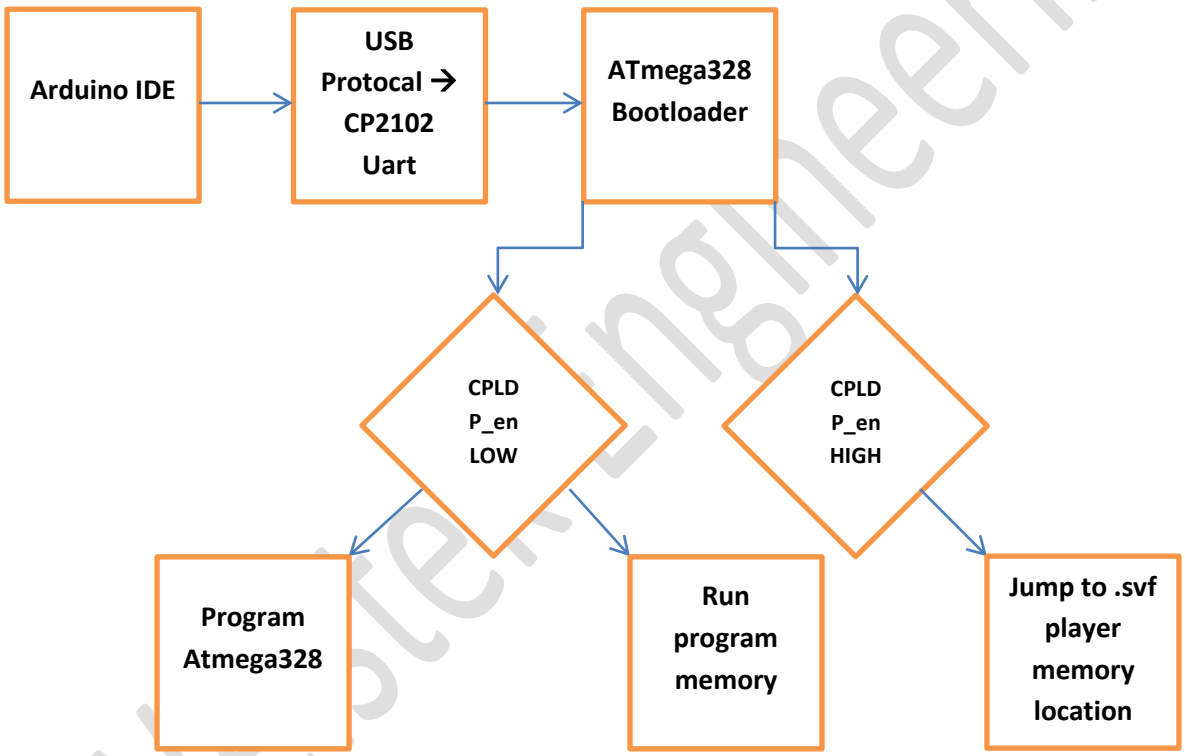
Bootloader operation.

XCACDV3 Boot loader operation.

This is a quick demonstration of the CPLDuino's boot loader enhanced with .xvf player capabilities.

USB → UART → 328 programming → Serial Communications → CPLD Jtag programming.

.svf player memory location ideally will be 0x0000 and protected by the boot loader, eg the boot loader will program user applications starting at a yet undetermined program memory location. Ideally this block of code should be no more than 2.5kb in size. Leaving the user with ~28KB code space of the 32KB available.

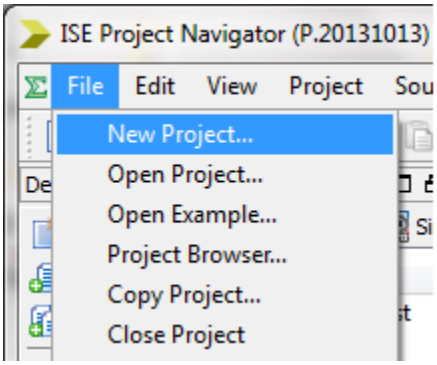


CPLDuino Primer Using VHDL

(CPLDuino Primer using Xilinx ISE 14.7)

Using the CPLDuino with Xilinx ISE webpack 14.7 IDE

To get started open the Xilinx ISE IDE on your desktop or from your start menu, click on [file] → [New Project]



The New Project Wizard will appear. Enter the name of your project, in our case tut1. A [Working directory] and a [Location] field, you can leave these fields as they are for now. You may also add a short description in the [Description] field "CPLDuino Practice project." Leave [Top-Level source type] as HDL, click next.

The next section is used to tell the ISE what chip you will be compiling for, in our case the XC9536XL CPLD.

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	XC9500XL CPLDs
Device	XC9536XL
Package	VQ44
Speed	-10
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	

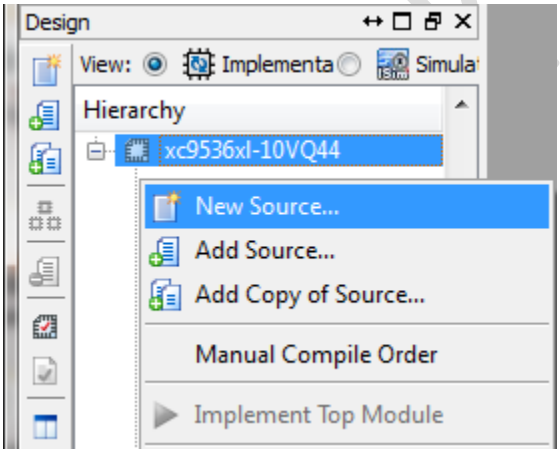
Using the CPLDuino with Xilinx ISE webpack 14.7 IDE (continued.)

Here is a quick breakdown of the fields used above. Only the fields currently altered are explained here. The information used here can be found on the etching on top of the chip or via the XC9536XL datasheet. In our case the top of the chip reads

[first line [XC9536XL] second line [VQ44] fourth line[10c]]

- [Family] each CPLD resides in a family tree so to speak, selecting the proper family allows us to select what device of that family we wish to use.
- [Device] in our case the XC9536XL CPLD, you can find the name of the chip if you look at the etching on the top of the chip, this also provides other bits of other useful information as well. [4]
- [Package] The XC9536XL on the CPLDuino is in a package form called VQFP with 44 pins thus we select VQ44 as our package type. This can also be seen on the information etched on the top of the chip.
- [Speed] CPLD's are very fast, but ours has a limit and that limit is 10ns (Nano seconds), this information is also etched on the chip as well.
- [Preferred Language] VHDL this is what we will use to code the logic for the CPLD.

Click next then click finish. You will be presented with an empty workspace for your project. Right click on add source..



This will allow us to add the required VHDL source file as well as the User Constraints file [UCF] used to assign our pin definitions. Once the Select Source Type dialog has appeared make sure you select [VHDL Module] then give is a name like "tut1main", using main at the end allows you to quickly identify what file is the top most part of your source code.

[3] Change this to XC9572XL if you have a 4.5 version of the board.

Using the CPLDuino with Xilinx ISE webpack 14.7 IDE (continued.)

The next section allows us to set pin definitions, you can do this here or manually edit the [UCF] file, for now click next we will manually edit the [UCF] file. Then click finish.

You will be presented with a default VHDL template such as this. You may fill in the comment section at the top. This allows you to keep track of what you have done to your project.

```
1  ----------------------------------------------------------------------------------
2  -- Company:       WeisTek Engineering
3  -- Engineer:      Jeremy G
4  --
5  -- Create Date:    18:20:03 04/23/2015
6  -- Design Name:    CPLDuino_Primer
7  -- Module Name:    CPLDuino_Primer - Behavioral
8  -- Project Name:   CPLDuino_Primer
9  -- Target Devices: XC9536XL
10 -- Tool versions:  14.7
11 -- Description:    VHDL Primer project for CPLDuino V0.4.5
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity CPLDuino_Primer is
33 end CPLDuino_Primer;
34
35 architecture Behavioral of CPLDuino_Primer is
36
37 begin
38
39
40 end Behavioral;
```

Using the CPLDuino with Xilinx ISE webpack 14.7 IDE (continued.)

Comments may be inserted into the VHDL file using two –‘s, this is different while designing the UCF file comments are created in the UCF by typing a # symbol before your comment. Comments are not multiline like in C/C++ each separate line of comments must have its comment designator symbols before the comment.

For now you can get rid of all the comments after line 21 these are not needed. For this tutorial we are going to wire the onboard led’s such that when the user pushes BTN1, LED1,3 are on. Same with BTN2 except LED2,4 will turn on, pressing both will light all leds on board.

Distributor.

The XCACDV3, CPLDuino development board is currently only sold by WeisTek engineering. www.weistekengineering.com

Limited quantity runs available please email Jeremy.goss@weistekengineering.com with subject line “XCACDV3 stock availability / Purchase Request” for stock updates or to place an order.

Notes.

Documentation Revisions.

02-16-2015 Ver 0.2

** Reference manual created.
** Added board layout description, Demo firmware flow, and Board schematic.

02-18-2015 Ver 0.3

** Board features and description added to Reference manual.
** Added Distributor information section.

02-21-2015 Ver 0.4

** Added bootloader flow chart demonstration, Changed font to Times New Roman.
** Added required software section, Fixed formatting issues.
** Fixed error's in documentation,

02-22-2015 Ver 0.5

** Added Weistek Logo to header.

03-01-2015 Ver 0.6

** Added CPLD getting started tutorial.

04-23-2015 Ver 7

** Cleaned up documentation.
** Added basic board overview.
** Added document Bookmarks.

Still TODO LIST.

Demonstration.

Power Supplies.

User programmable CPLD clocks.

User I/O

Troubleshooting.