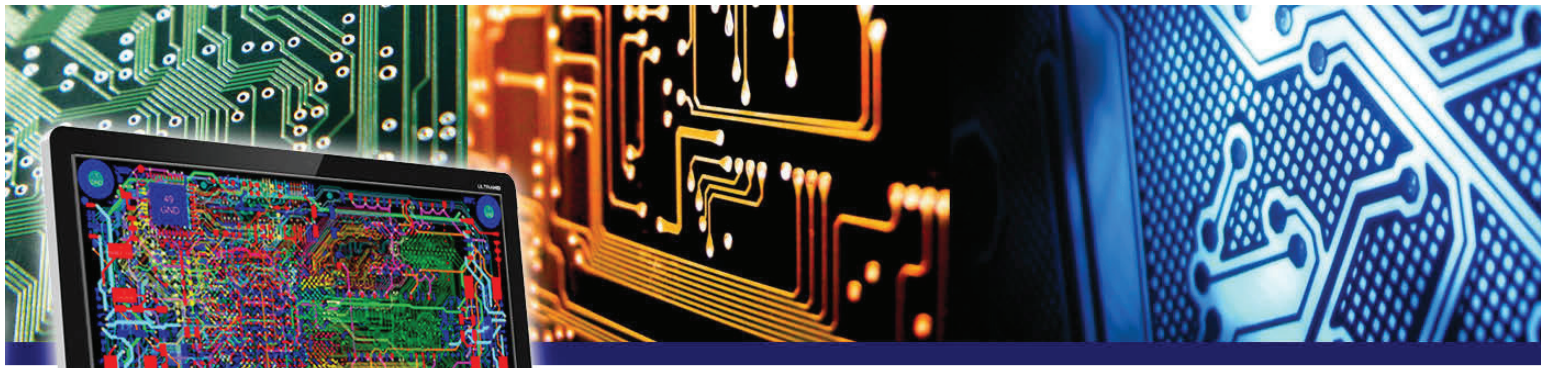




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- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

The Perfect Stackup (for High-Speed Design)

by **Barry Olney**

IN-CIRCUIT DESIGN PTY LTD, AUSTRALIA

This application note discusses how to plan a multilayer PCB stackup to obtain the ideal stackup for high-speed design.

Throughout the past 30 years, the concept of the perfect stackup has changed considerably. Especially in more recent years, where engineers and designers have had the opportunity to use simulation tools that act as another pair of eyes when it comes to understanding the intricacies of the effects of transmission lines on multilayer PCBs.

In previous articles, I have discussed the selection of reference planes and routing pairs, why high-speed signals should be embedded between the planes and methods of reducing EMI. However, if we fail to get the substrate correct then all of the above techniques are worthless. Planning the multilayer stackup configuration is one of the most important aspects in achieving the best possible performance of a product, yet it is something that few of us do (or should I say, do well).

A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission increasing emissions and crosstalk and can make the product more susceptible to external noise. These issues can cause intermittent operation due to timing glitches and interference, dramatically reducing the products performance and long-term reliability.

In contrast, a properly built PCB substrate can effectively reduce electromagnetic emissions, crosstalk and improve the signal



integrity, providing a low-inductance power distribution network (PDN). Additionally, from a fabrication point of view, it can also improve the manufacturability of the product and reduce costs.

Suppressing the noise at the source rather than trying to elevate the problems once the product has been built makes sense. Having the project completed 'Right the First Time,' on time and to

budget means that you cut costs by reducing the design cycle, have a shorter time to market and an extended product life cycle.

Interplane Capacitance

A good place to start is with the PDN. More importantly, how we can provide a low inductance PDN and thus reduce the high-frequency noise?

Decoupling capacitors (Dcaps) supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers.

Every decoupling capacitor has a finite series inductance, which causes its impedance to increase at high frequencies. In order to reduce this inductance as much as possible, a number of small-value Dcaps should be placed in parallel as close as possible to each power pin using a thick, short trace. This is not always possible as

circuit density increases with the use of fine-pitch BGAs, so an alternative option is to take advantage of interplane capacitance to distribute capacitance across the board. This is not to say that the Dcaps aren't required—every little bit counts.

The power to ground plane capacitance provides an ideal capacitor in that it has no series lead inductance and no equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies. The interplane capacitance needs to be calculated to establish the optimal use of the planes to create the ideal stackup.

$$C_{\text{interplane}} = \frac{0.225 \cdot \epsilon_r \cdot A}{d}$$

where: ϵ_r is the Dielectric Constant (FR4 is 4.3)

A is the area of the PCB

d is the distance between the planes

Good interplane capacitance can be achieved by using 4-MIL plane spacing resulting in 241 pF/in². The higher the better. Whereas, 10-MIL spacing will only achieve 96.75 pF/in² and 60 MIL a dismal 16 pF/in². Therefore, this goes right in the middle of the substrate to maintain symmetry.

Reference Planes and Signal Layers

The next step in building the ideal stackup is to consider that every signal layer needs to have a reference plane (either ground or power) adjacent to it in order to provide a return current path. This limits the number of signal layers embedded between the planes to two

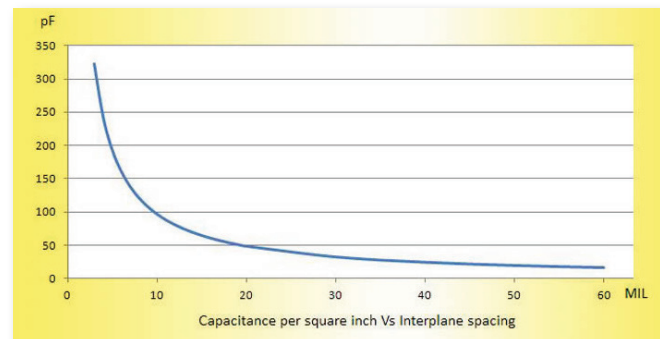


Figure 1.

and on the top and bottom (outer) layers to one.

However, routing two signal layers between planes is not a good idea for high-speed designs as the close proximity of signals will inevitably create broadside coupling (crosstalk) unless the two signal layers are routed orthogonally to each other to limit the coupling area. This limits the stackup to one signal layer between planes.

Inner layer 3 is added in Figure 3. This will provide 100-ohm differential clocks at 4/8 (trace width/clearance). Alternatively, in Figure 4 we change the trace width/clearance to 7/16, using the same substrate, to provide USB differential signals of 90- and 50-ohm single-ended (characteristic) impedance on this layer.

Soldermask—Effects on Impedance

Another point often missed is the effects of soldermask (conformal coating) on microstrip (outer layer) impedance. Without soldermask, the differential impedance of the top microstrip layer is 103.94 ohms.

Layer Number	Layer Name	Material Type	Dielectric		Copper Thickness	Trace		Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
			Constant	Thickness		Clearance	Width					
1	VCC	Conductive	4.3	4	1.4							Plane
		Dielectric										Core
2	GND	Conductive			1.4							Plane

Figure 2. Interplane capacitance is 241 pF/in²

Layer Number	Layer Name	Material Type	Dielectric		Copper Thickness	Trace		Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
			Constant	Thickness		Clearance	Width					
2	GND	Conductive	4.3	8	1.4							Plane
		Dielectric										Core
3	Inner 3	Conductive	4.3	12	1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	4	1.4							Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4	1.4							Core
5	GND	Conductive			1.4							Plane

Figure 3. Inner layer 3, 100 ohm differential pairs.

Layer Number	Material Name	Material Type	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description
			Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	16	7	0.47	50.72	89.54		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Figure 4. USB differential pairs of 90 ohm.

Adding the soldermask to Figure 6 illustrates how the impedance drops by nearly 4 ohms for the differential pair and 2 ohms for the signal-ended trace. If you don't consider soldermask then the calculation could be as much as 4% out, which is significant since the process margin is +/- 10%.

It is also important to note that particularly on the outer microstrip layers the signal-to-plane spacing should be kept to a minimum. This reduces crosstalk significantly.

Having determined the basic structure of the stackup with the aid of the ICD Stackup Planner (download from www.icd.com.au) we now need to consider how many layers will be required to route the board.

Determining the Layer Count

The technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable whilst minimizing PCB fabrication costs. Technology of 4/4 MIL

(trace/clearance) and vias of 20/8 MIL (pad/hole) are generally required for complex high-speed design incorporating ball grid arrays (BGA). However, if you can use less demanding dimensions then this will reduce cost and improved fabrication yield.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50-ohm Zo and 100-ohm Zdiff are used. Keep in mind that lower impedance will increase the di/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and make the design more susceptible to outside interference. Therefore, a good range of Zo is 50 – 60 ohms.

The total number of layers required for a given design is dependent on the complexity of the design. Factors include the number of signal nets that must break out from a BGA, the number of power supplies required by the

Layer Number	Material Name	Material Type	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description
			Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Conductive			1.4	8	4	0.31	55.64	103.94		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Figure 5. Microstrip layer without soldermask.

Layer Number	Material Name	Material Type	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description
			Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Conductive			1.4	8	4	0.31	53.53	99.99		Soldermask
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Figure 6. Soldermask over microstrip.

THE PERFECT STACKUP (FOR HIGH-SPEED DESIGN) *continues*

UNITS: MIL ICD STACKUP PLANNER – www.icd.com.au 9/27/2011 Total Board Thickness: 61.2

		Differential Pairs >		USB	DDR2	SATA	ETHERNET	LVDS				
Layer	Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled		
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Dielectric	3.3	0.5								Soldermask
		Conductive			1.4	8	4	0.31	53.53	99.99		Signal
2	GND	Dielectric	4.3	3	1.4							Prepreg
		Conductive										Plane
3	Inner 3	Dielectric	4.3	8	1.4	8	4	0.31	62.39	99.59		Core
		Conductive										Signal
4	VCC	Dielectric	4.3	12	1.4							Prepreg
		Conductive										Plane
5	GND	Dielectric	4.3	4	1.4							Core
		Conductive										Plane
6	Inner 6	Dielectric	4.3	12	1.4	12	6	0.42	54.11	91.56		Prepreg
		Conductive										Signal
7	GND	Dielectric	4.3	8	1.4							Core
		Conductive										Plane
8	Bottom	Dielectric	4.3	3	1.4	4	4	0.31	53.53	89.98		Prepreg
		Conductive										Signal
		Dielectric	3.3	0.5								Soldermask

Figure 7. Completed eight-layer stackup.

UNITS: MIL ICD STACKUP PLANNER – www.icd.com.au 9/27/2011 Total Board Thickness: 90.8

		Differential Pairs >		USB	DDR2	SATA	ETHERNET	LVDS				
Layer	Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled		
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Dielectric	3.3	0.5								Soldermask
		Conductive			1.4	8	4	0.31	53.53	99.99		Signal
2	GND	Dielectric	4.3	3	1.4							Prepreg
		Conductive										Plane
3	Inner 3	Dielectric	4.3	6	1.4	12	4	0.31	56.4	98.4		Core
		Conductive										Signal
4	GND	Dielectric	4.3	10	1.4							Prepreg
		Conductive										Plane
5	Inner 5	Dielectric	4.3	6	1.4	12	4	0.31	56.4	98.4		Core
		Conductive										Signal
6	VCC	Dielectric	4.3	10	1.4							Prepreg
		Conductive										Plane
7	GND	Dielectric	4.3	4	1.4							Core
		Conductive										Plane
8	Inner 8	Dielectric	4.3	10	1.4							Prepreg
		Conductive										Signal
9	VDD	Dielectric	4.3	6	1.4	12	5	0.37	51.96	90.66		Core
		Conductive										Signal
10	Inner 10	Dielectric	4.3	10	1.4	6	4	0.31	56.4	89.06		Prepreg
		Conductive										Plane
11	GND	Dielectric	4.3	3	1.4							Core
		Conductive										Plane
12	Bottom	Dielectric	4.3	6	1.4	4	4	0.31	53.53	89.98		Prepreg
		Conductive										Signal
		Dielectric	3.3	0.5								Soldermask

Figure 8. 12-layer extension of the ideal eight-layer PCB.

BGAs and component density and package types.

Experienced designers get a feel for it after a while, but a good way to check if you have enough layers is to autoroute the board. With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable. The performance of the autorouter also affects the completion rate. You may have to re-evaluate the placement a couple of times to get the best results.

The above stackup represents the perfect stackup. Why perfect?

- There is good interplane capacitance of 241 pF/in².
- All signal layers are adjacent to a reference plane, creating a clear return path and eliminating broadside crosstalk.
- The signal-ended and differential impedance for a number of different technologies that must share the sample layers is determined.
- Microstrip layers are closely coupled to the planes, reducing crosstalk.
- The effects of soldermask on impedance have been realized.

If you are risk averse, this is the stackup to use. Of course, this can be extrapolated to include more routing layers if there is a need. Simply keep the closely coupled planes in the centre and add more signals layers and planes keeping symmetry. The dielectric thickness may also need to be adjusted to achieve the desired impedances and total board thickness. The selection process can be simplified by using the HDI Designer Edition of the ICD Stackup Planner, which assists in the definition of multiple technologies sharing the one substrate and allows groups of layers to be cut/copied/pasted to build up a substrate. I have provided an example of adding two more routing layers in the 12-layer stackup of Figure 8. **PCB**

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Barry Olney is Managing Director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among others through the years, ICD was awarded "Top 2005 Asian Distributor Marketing" and "Top 2005 Worldwide Distributor Marketing by Mentor Graphics, Board System Division. For more information, contact Barry Olney at +61 4123 14441 or email at b.olney@icd.com.au.

IPC APEX DISCUSSES KEY INDUSTRY ISSUES IN FREE SESSIONS

They are the subjects of countless headlines and industry tweets—the impact on industry of conflict minerals, embedded technology, process defects and supply line issues such as counterfeit parts—and the topics of two full days' worth of free BUZZ sessions at IPC APEX EXPO 2012, to be held February 28–March 1, at the San Diego Convention Center. Seven BUZZ sessions will offer industry members an ideal forum to learn about issues from subject-matter experts

The BUZZ sessions kick off on the afternoon of February 28 with Bob Willis and Christopher Hunt, Ph.D., of the National Physical Laboratory, presenting Tin Whiskers, Delamination, Copper Dissolution, CAF, Coating Adhesion. Hunt and Willis will share the results of some of the most interesting and innovative research work conducted at NPL on these defects. Their session will continue with free mini sessions and individual troubleshooting on the show floor at the NPL Defect Database Clinic.

Jack Fisher of Interconnect Technology Analysis Inc., will highlight key discoveries of the 2012 IPC

International Technology Roadmap and how the document can be used as a sort of GPS to guide companies in their development of business and market strategies and to validate and justify capital investment.

In Embedded: Emerging Technologies on February 29, Mark Beesley, MB Manufacturing, and Vern Solberg, Solberg Technical Consulting, will provide an in-depth look at where embedded technology is going and what the industry can expect to see in the coming years.

The session, Are Conflict Minerals the New RoHS? will host a respected panel of experts who will provide the latest information on the SEC regulations, guidance, and industry tools to help companies meet legal and customer requirements that will rapidly flow through the entire supply chain.

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