PORTATILE PER ACUBE ACB_0001_0

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Version Control

Version	Date	Modifications
V0.1	2018/12	First release of Schematics
V0.2	2019/09	Second release of Schematics

PROTO

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Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PAGE LISTING		
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SYSTEM BLOCK DIAGRAM

PROTO

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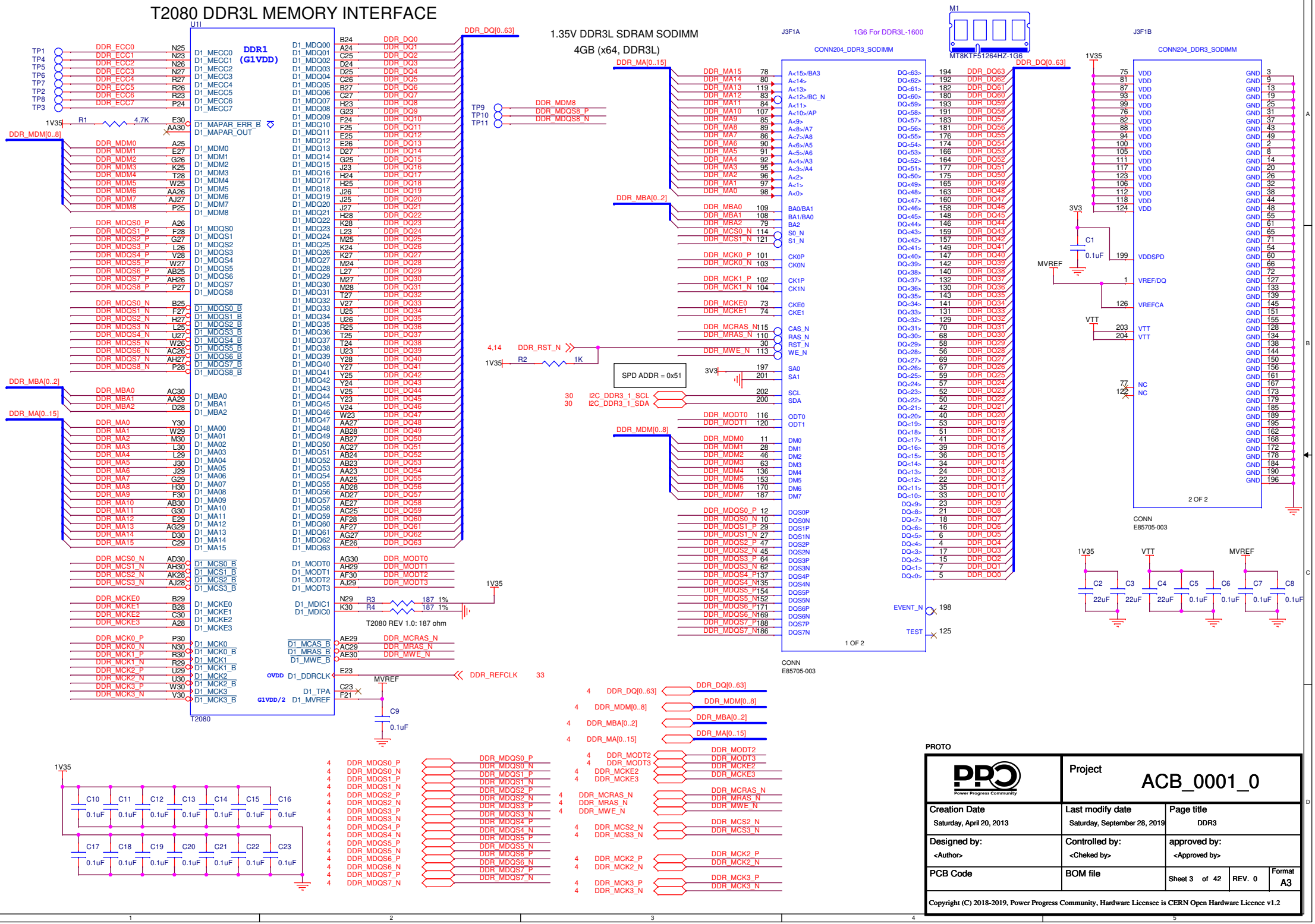
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 2 of 42	REV. 0	Format A3

T2080 DDR3L MEMORY INTERFACE



1.35V DDR3L SDRAM SODIMM

4GB (x64, DDR3L)

J3F2A

1G6 For DDR3L-1600

CONN204_DDR3_SODIMM

M16

MT8KTF51264HZ-1G6

DDR_DQ[0..63]

DDR_DQ[0..63]

DDR_MA[0..15]

DDR_MA[0..15]

DDR_MBA[0..2]

DDR_MBA[0..2]

DDR_MCS2_N

DDR_MCS3_N

DDR_MCK2_P

DDR_MCK2_N

DDR_MCK3_P

DDR_MCK3_N

DDR_MCKE2

DDR_MCKE3

DDR_MCRAS_N

DDR_MRAS_N

DDR_RST_N

R938 1K

1V35

DDR_MWE_N

SPD ADDR = 0x52

3V3

I2C_DDR3_2_SCL

I2C_DDR3_2_SDA

DDR_MODT2

DDR_MODT3

DDR_MDM[0..8]

DDR_MDM[0..8]

DDR_MDQS0_P

DDR_MDQS0_N

DDR_MDQS1_P

DDR_MDQS1_N

DDR_MDQS2_P

DDR_MDQS2_N

DDR_MDQS3_P

DDR_MDQS3_N

DDR_MDQS4_P

DDR_MDQS4_N

DDR_MDQS5_P

DDR_MDQS5_N

DDR_MDQS6_P

DDR_MDQS6_N

DDR_MDQS7_P

DDR_MDQS7_N

1 OF 2

CONN

E85705-003

J3F2B

CONN204_DDR3_SODIMM

1V35

3V3

C1090 0.1uF

MVREF

VTT

VDDSPD

VREF/DQ

VREFCA

NC

NC

2 OF 2

CONN

E85705-003

1V35 VTT MVREF

C1091 22uF C1092 22uF C1093 22uF C1094 0.1uF C1095 0.1uF C1096 0.1uF C1097 0.1uF

1V35

C1098 C1099 C1100 C1101 C1102 C1103 C1104

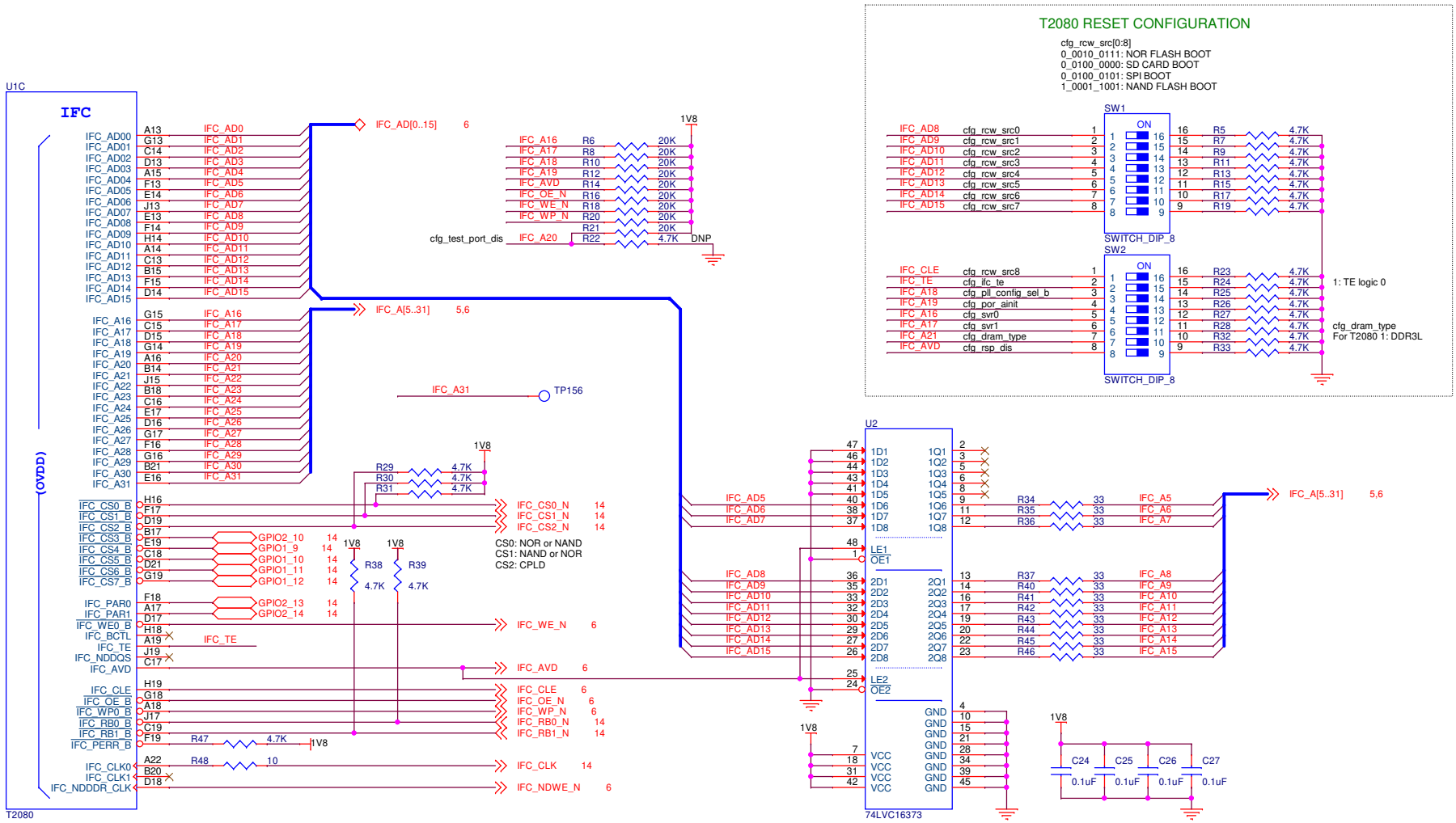
C1105 C1106 C1107 C1108 C1109 C1110 C1111

0.1uF

PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Sunday, September 22, 2019	Last modify date: Saturday, September 28, 2019	Page title: DDR3_2
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 4 of 42 / REV. 0 / Format A3

T2080 IFC INTERFACE



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PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: IFC	
Designed by:	Controlled by:	approved by:	
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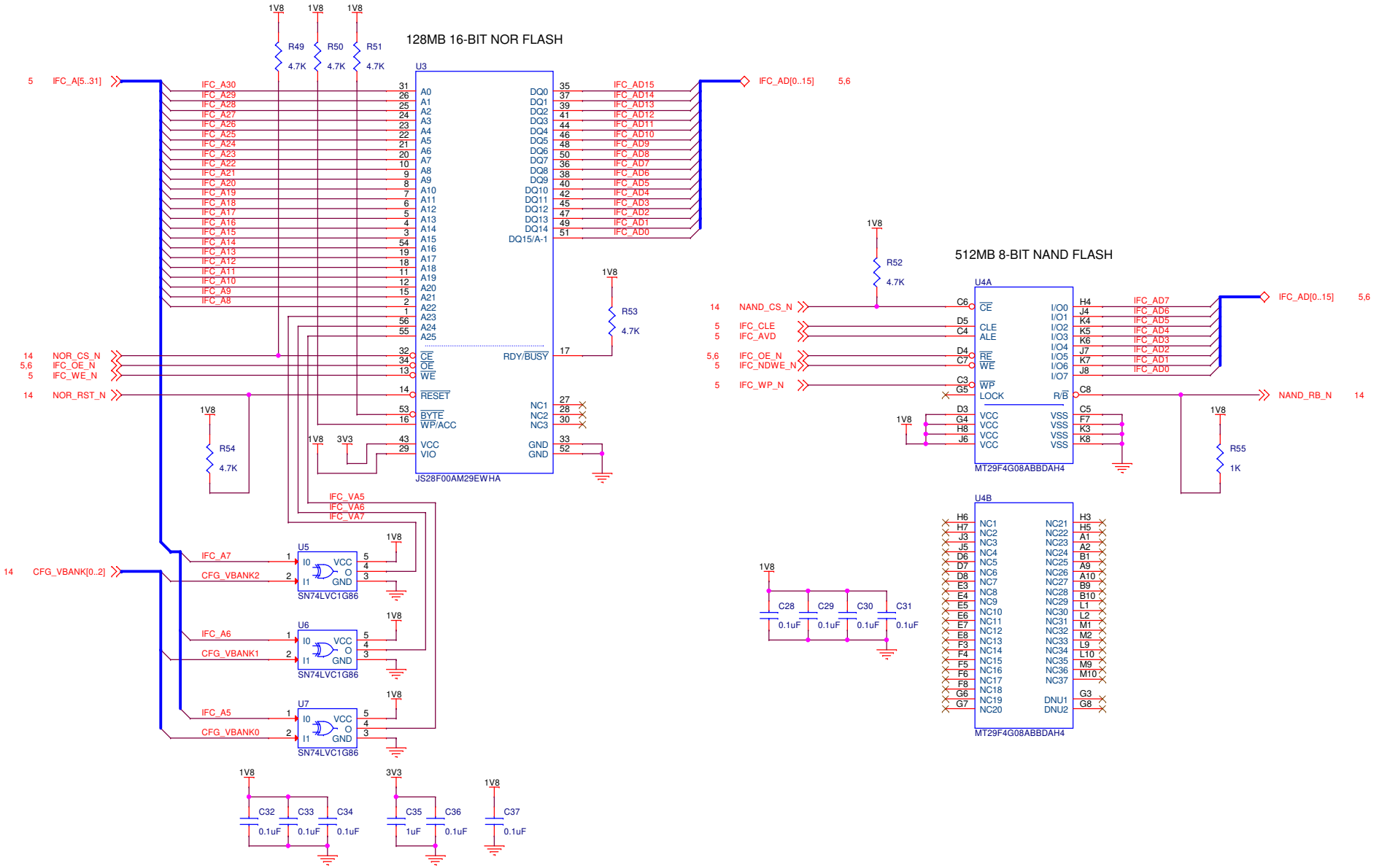
T2080 NOR and NAND FLASH INTERFACE



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PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: FLASH
Designed by:	Controlled by:	approved by:
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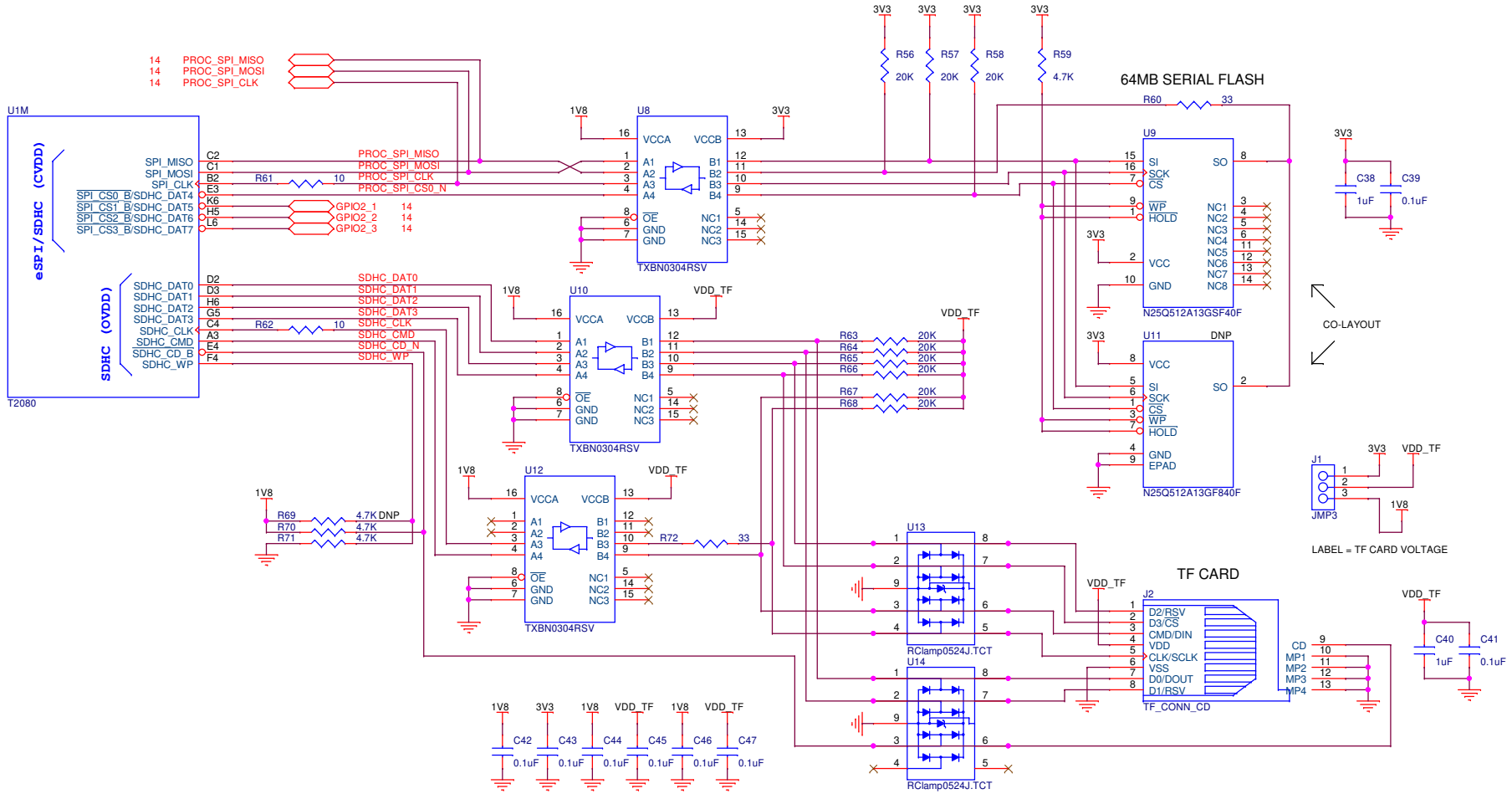
T2080 SPI FLASH and SDHC INTERFACE



PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: SPI&SDHC
Designed by:	Controlled by:	approved by:
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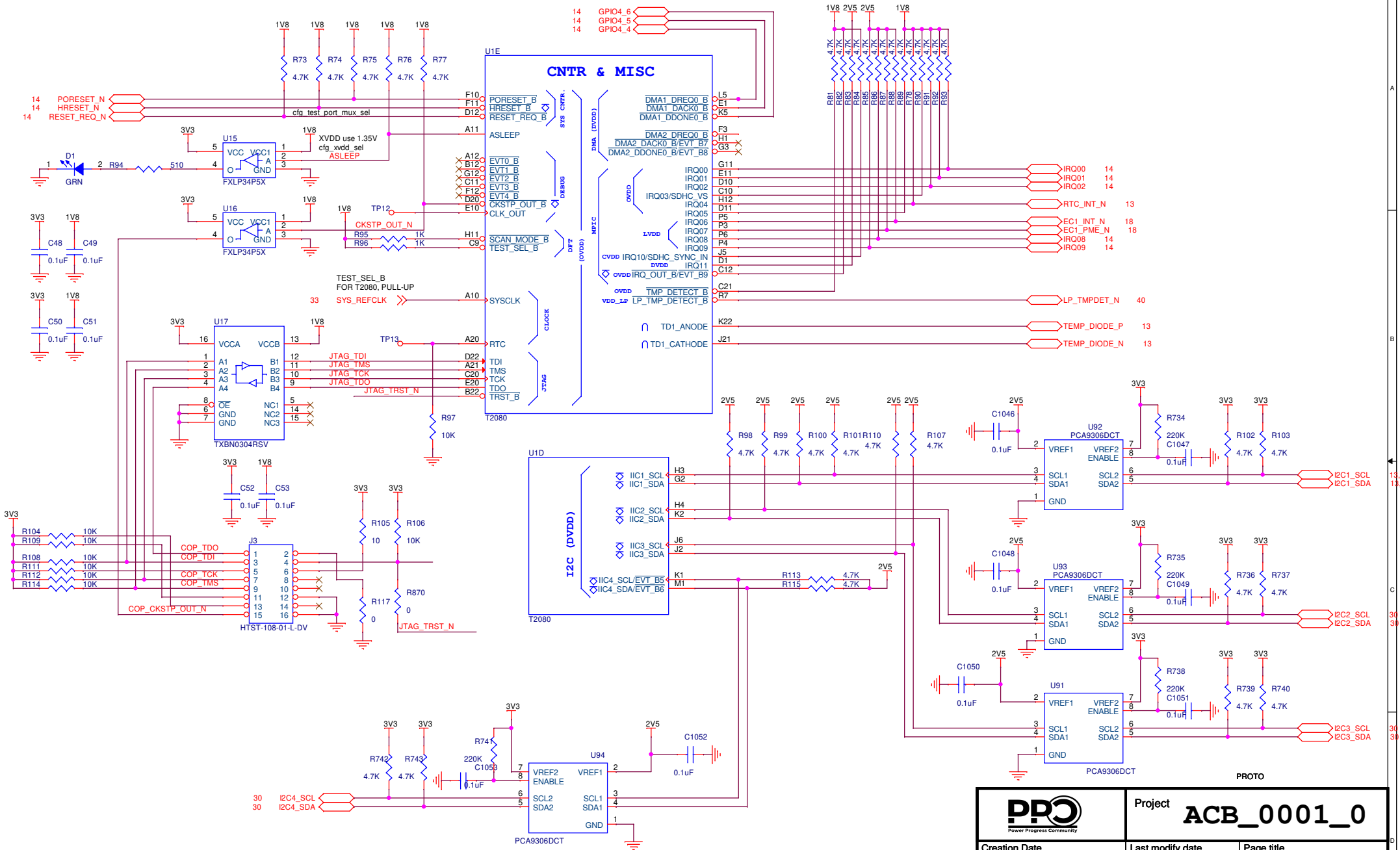
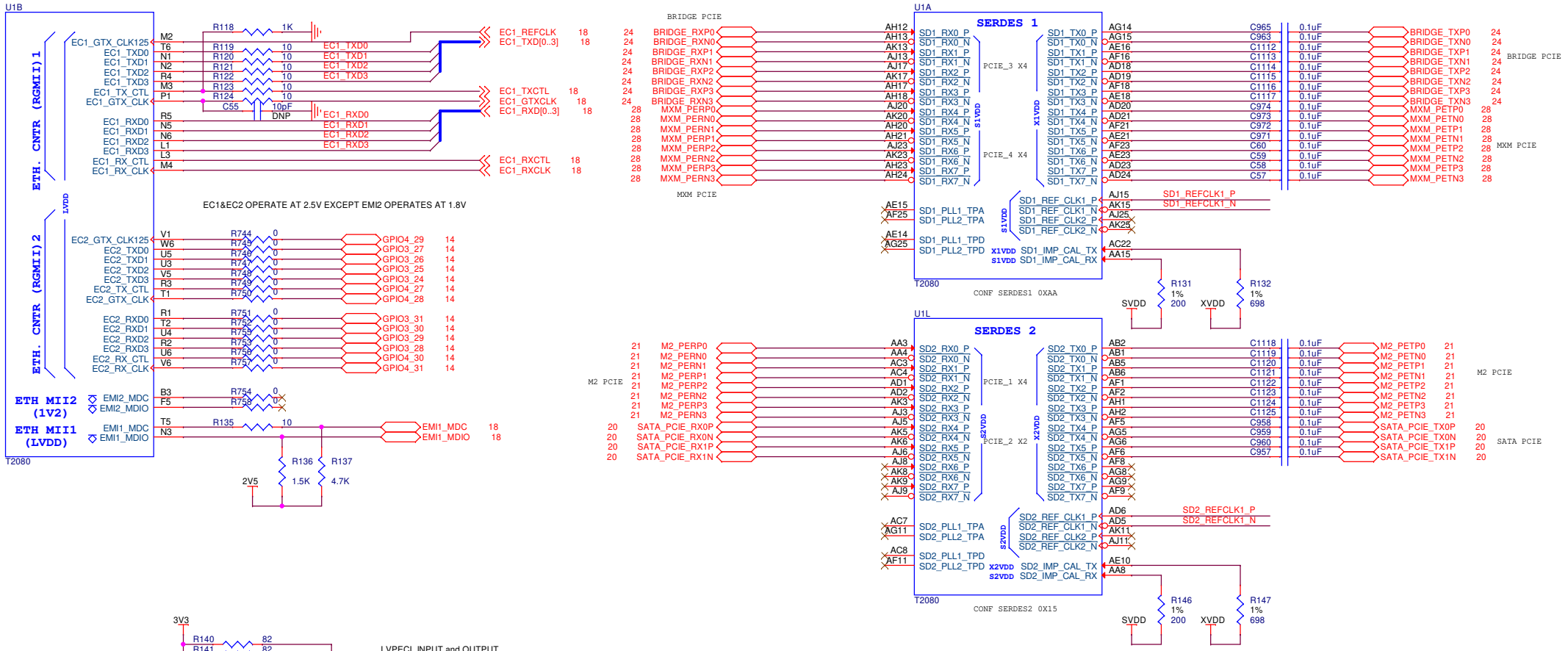
T2080 SYSTEM LOGIC INTERFACE



PPC Power Progress Community	Project **ACB_0001_0**		
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: SYS	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 8 of 42 / REV. 0	Format A3

T2080 ETHERNET and SERDES INTERFACE



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PPC Power Progress Community	Project **ACB_0001_0**		
Creation Date	Last modify date	Page title EC&SD	
Designed by: Saturday, September 28, 2019	Controlled by:	approved by:	
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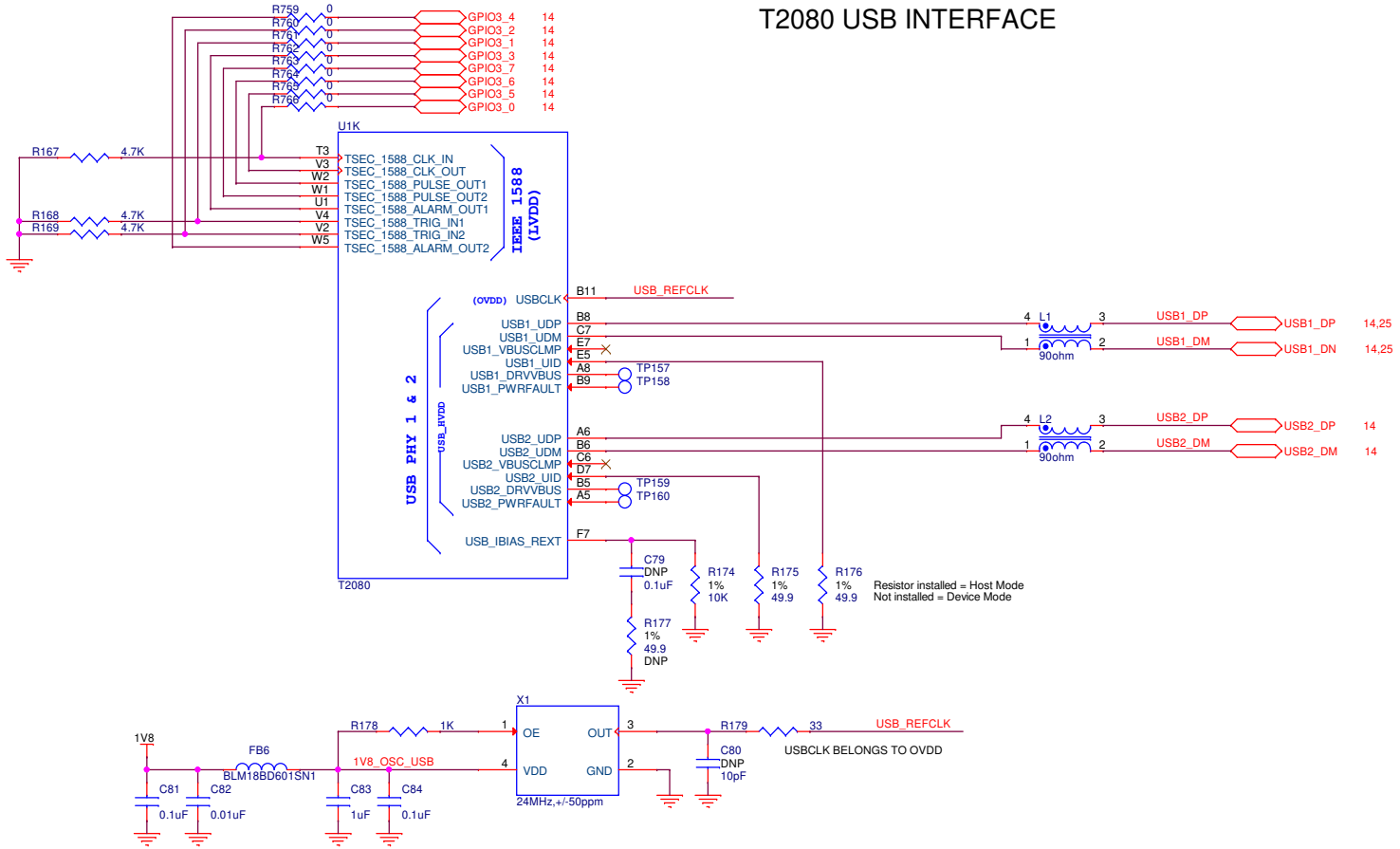
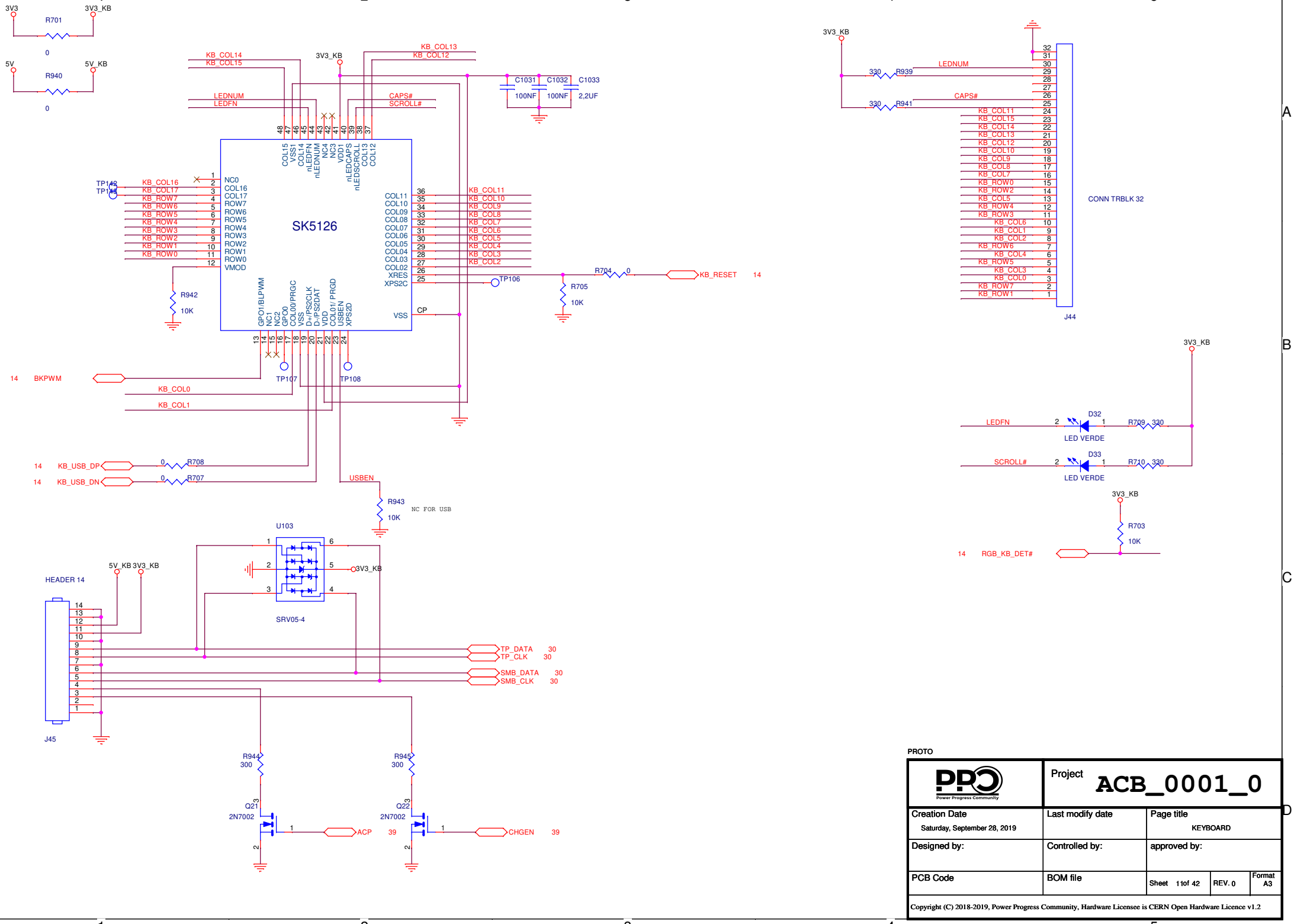
T2080 USB INTERFACE



PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date	Last modify date	Page title: USB
Designed by: Saturday, September 28, 2019	Controlled by:	approved by:
PCB Code	BOM file	Sheet 10of 42 / REV. 0 / Format A3



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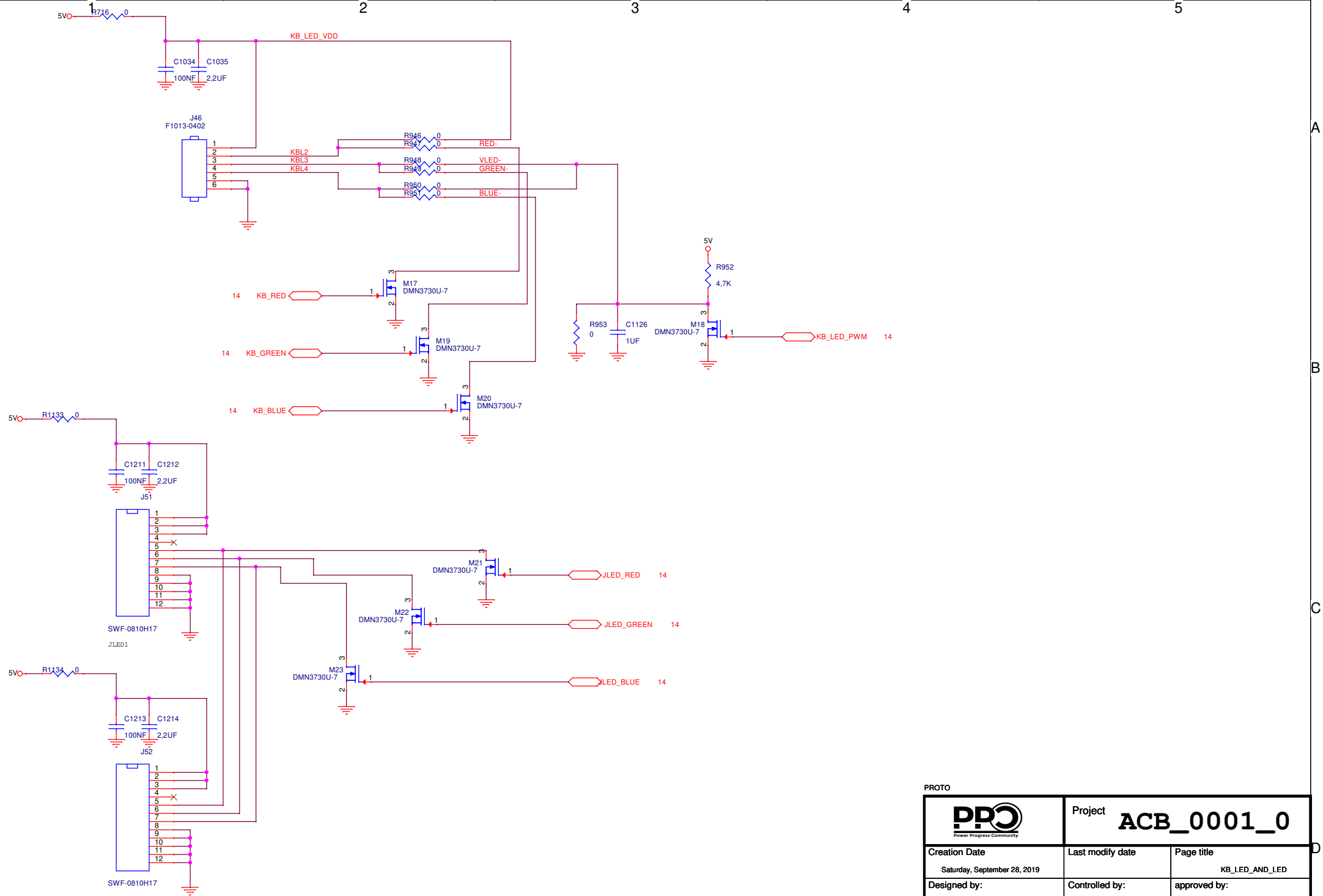
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: KEYBOARD
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 11of 42 / REV. 0 / Format A3



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PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: KB_LED_AND_LED
Designed by:	Controlled by:	approved by:
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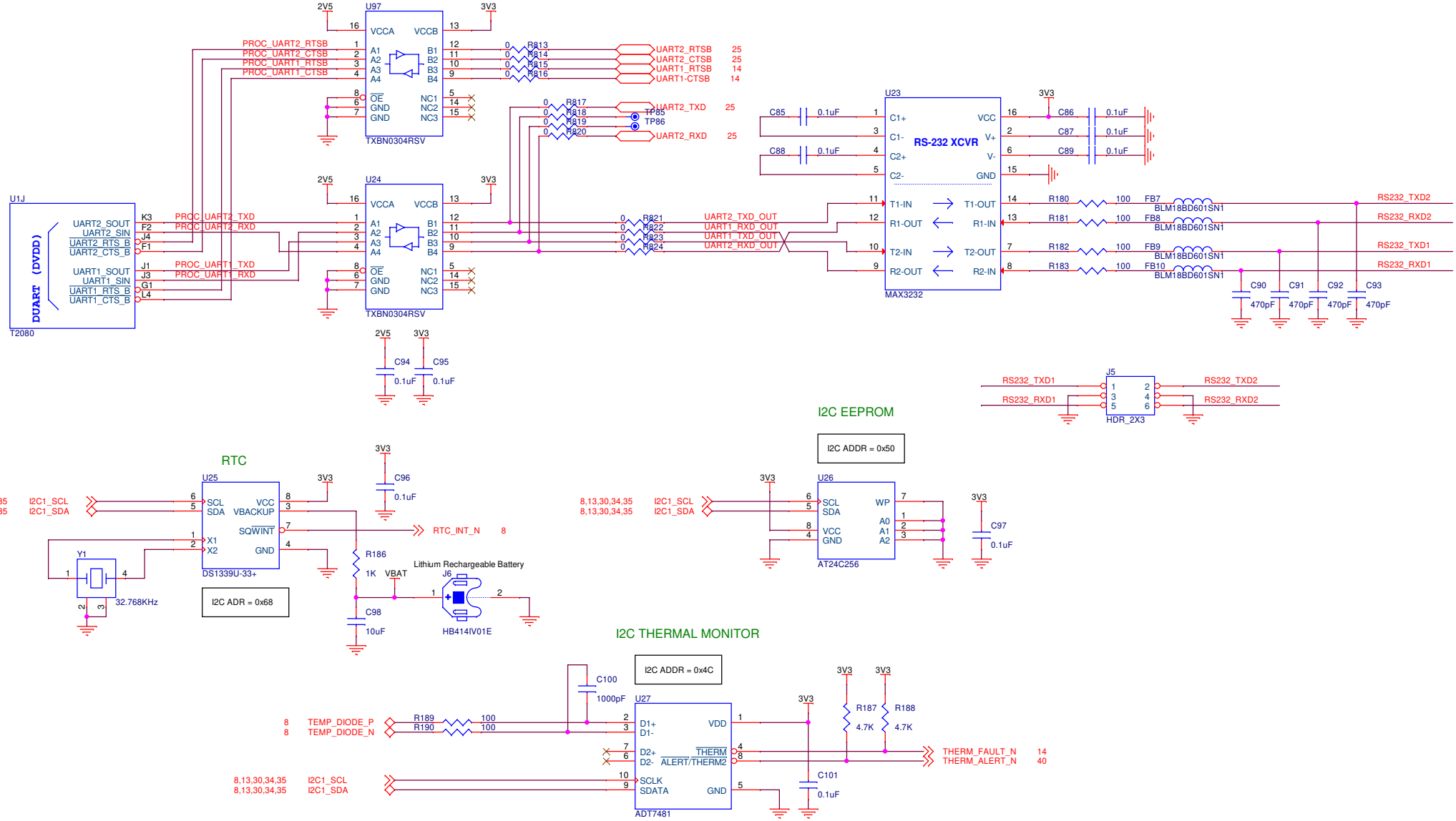
T2080 DUART and I2C DEVICE INTERFACE



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PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: UART&I2C
Designed by:	Controlled by:	approved by:
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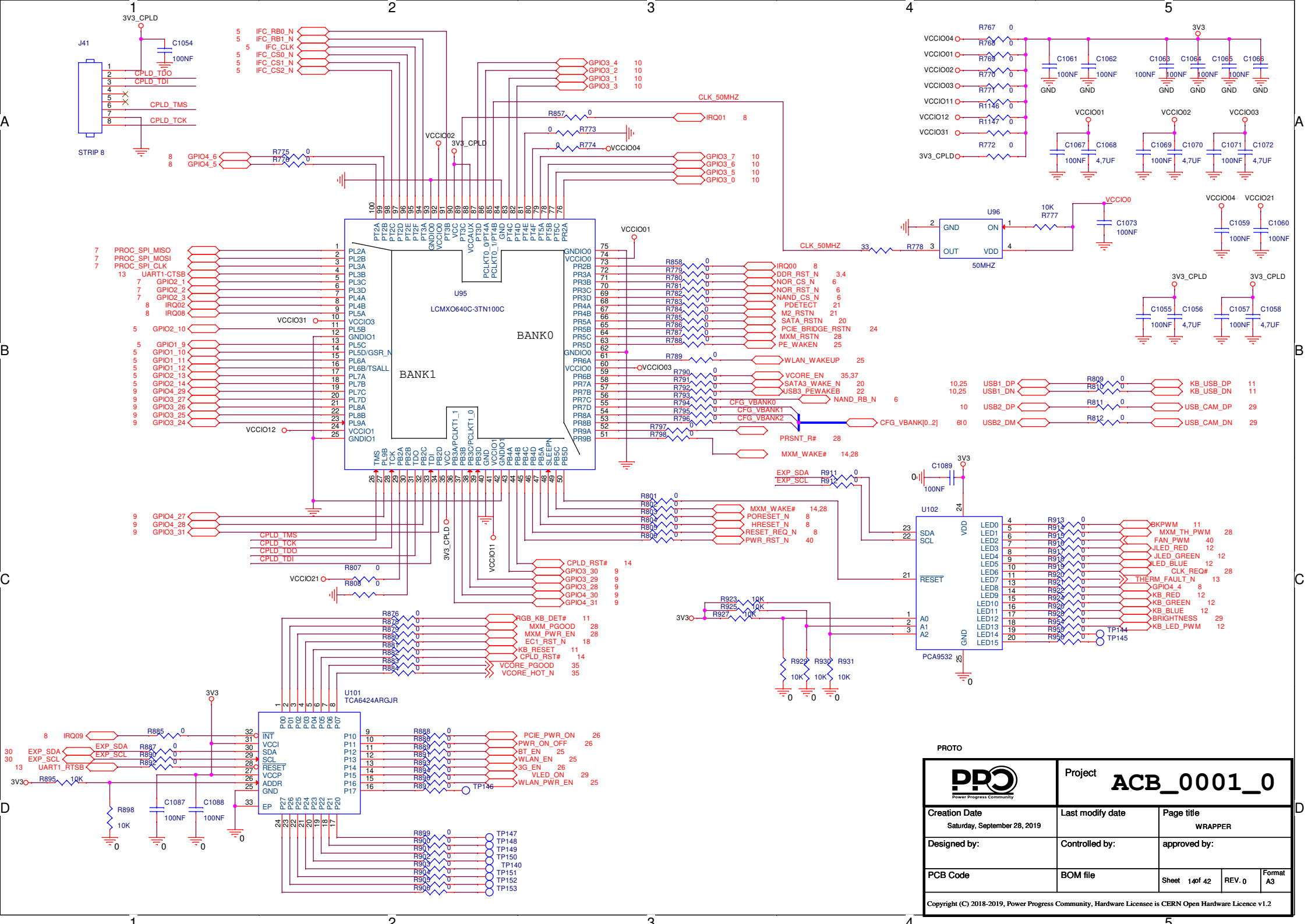
U95
LCMXO640C-3TN100C
BANK0
BANK1
U96
U102
PCA9532
U101
TCA6424ARGJR
J41
STRIP 8
3V3_CPLD
VCCIO01
VCCIO02
VCCIO03
VCCIO04
VCCIO12
VCCIO21
VCCIO31
CLK_50MHZ
50MHZ
IRQ00
IRQ01
DDR_RST_N
NOR_CS_N
NOR_RST_N
NAND_CS_N
PDETECT
M2_RSTN
SATA_RSTN
PCIE_BRIDGE_RSTN
MXM_RSTN
PE_WAKEN
WLAN_WAKEUP
VCORE_EN
SATA3_WAKE_N
USB3_PEWAKEB
NAND_RB_N
CFG_VBANK0
CFG_VBANK1
CFG_VBANK2
CFG_VBANK[0..2]
PRSNT_R#
MXM_WAKE#
USB1_DP
USB1_DN
USB2_DP
USB2_DM
KB_USB_DP
KB_USB_DN
USB_CAM_DP
USB_CAM_DN
EXP_SDA
EXP_SCL
CPLD_RST#
PROTO
Project
ACB_0001_0
Creation Date
Saturday, September 28, 2019
Last modify date
Page title
WRAPPER
Designed by:
Controlled by:
approved by:
PCB Code
BOM file
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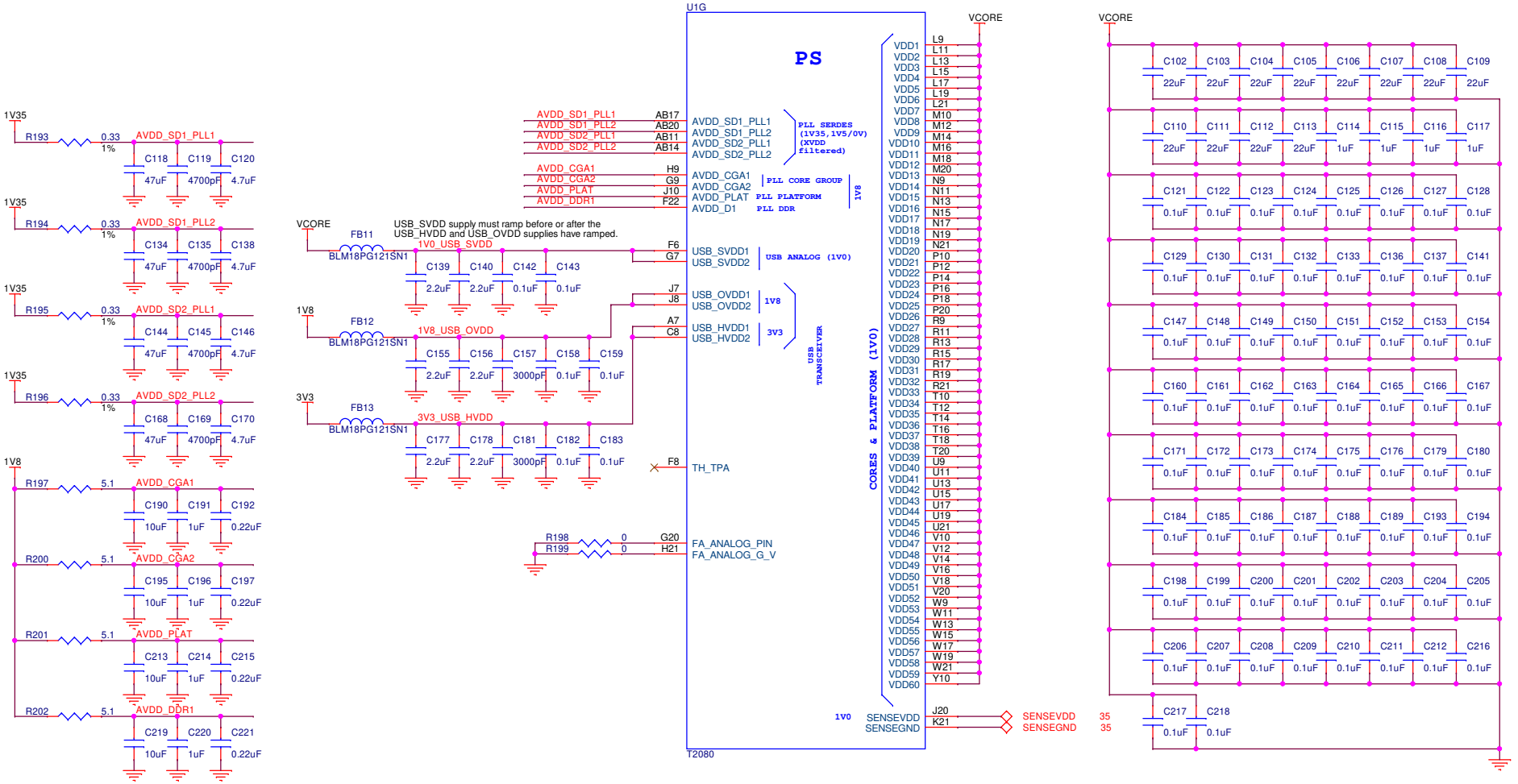
REV. 0
Format A3
Copyright (C) 2018-2019, Power Progress Community, Hardware Licensee is CERN Open Hardware Licence v1.2

T2080 POWER SUPPLY



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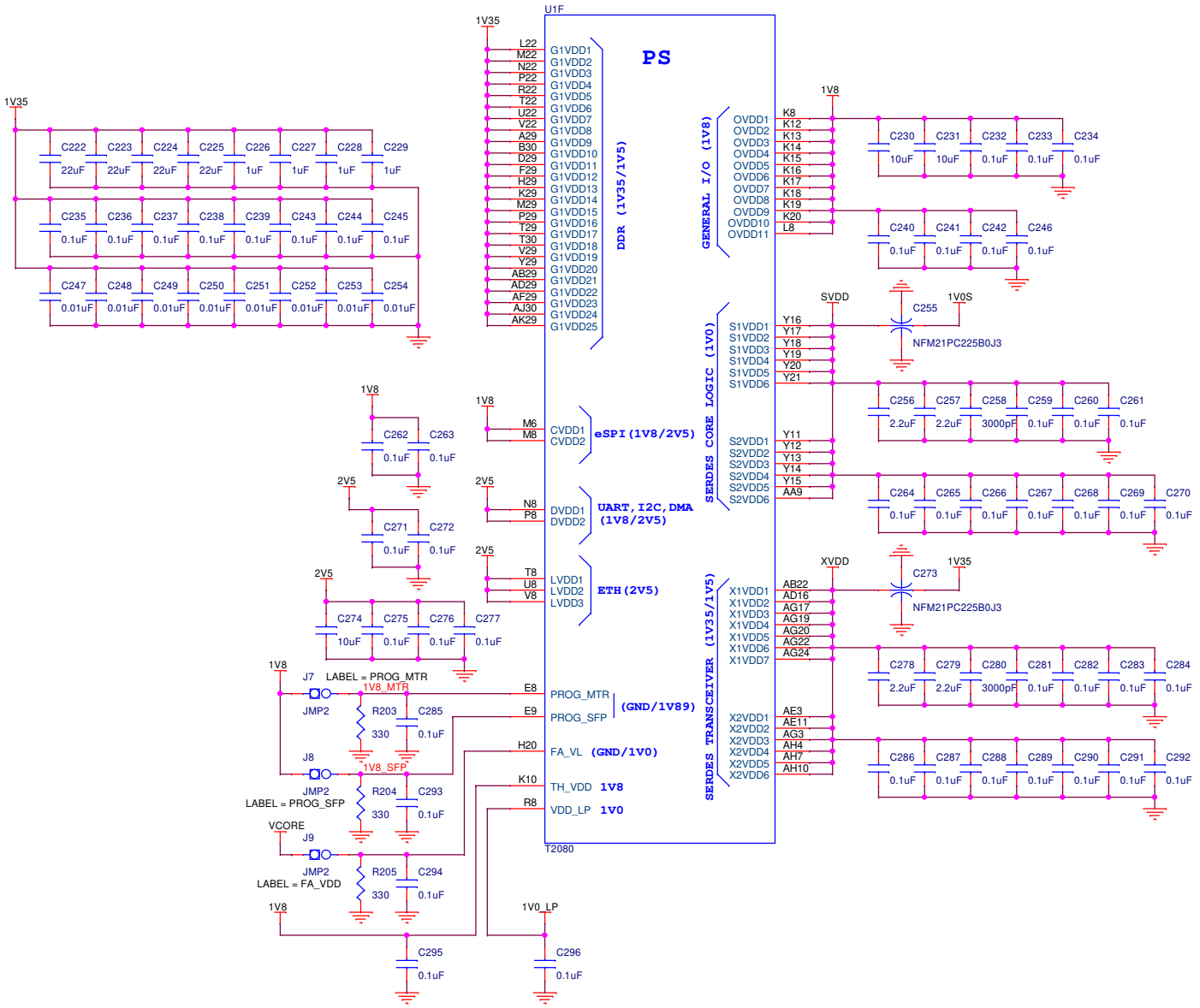
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PROC PWR1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 15of 42 / REV. 0 / Format A3

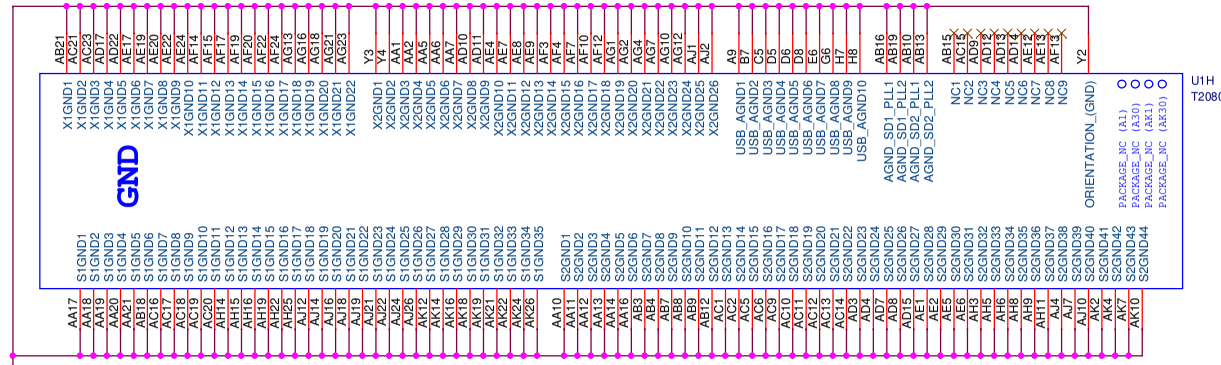
T2080 POWER SUPPLY (cont.)

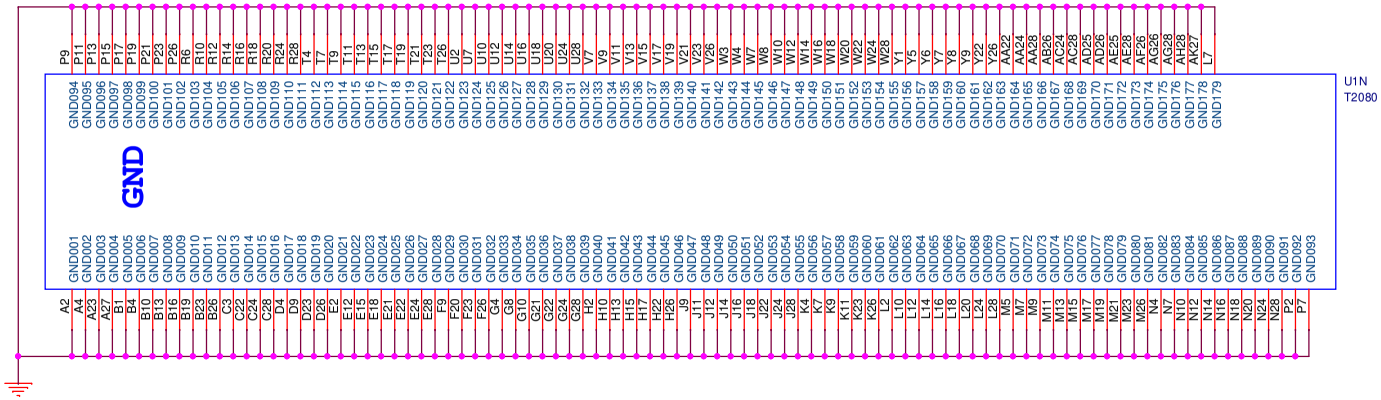


PROTO

PPC Power Progress Community	Project **ACB_0001_0**		
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PROC PWR2	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet16 of 42 / REV. 0	Format A3

T2080 GROUND





PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PROC GND
Designed by:	Controlled by:	approved by:
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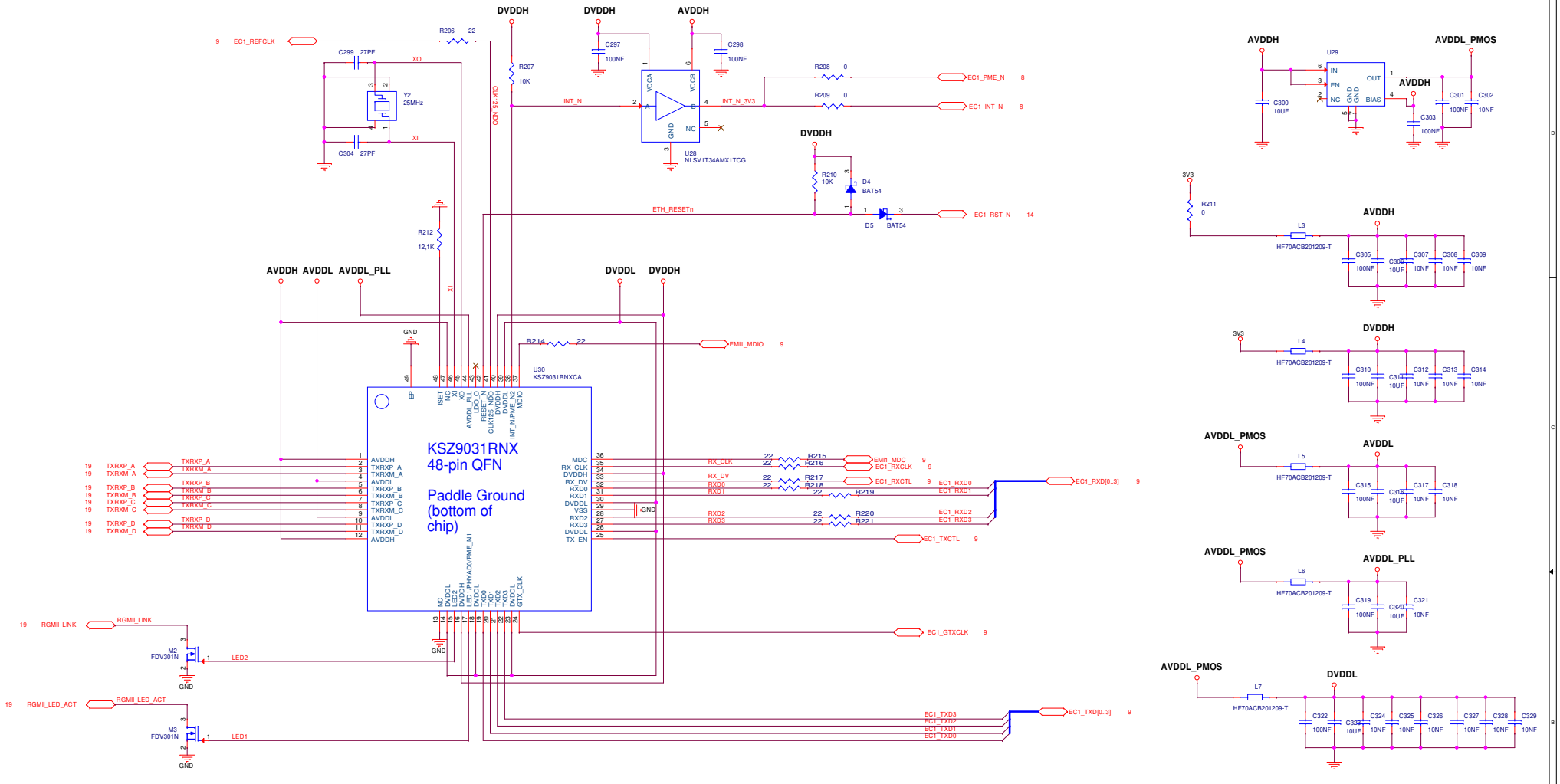
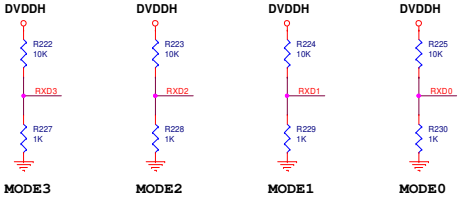


Strapping Pins



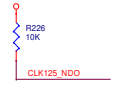
MODE[3:0]	Description
0000	reserved
0001	reserved
0010	reserved
0011	reserved
0100	NAND Tree mode
0101	reserved
0110	reserved
0111	Chip Power Down

MODE[3:0]	Description
1000	reserved
1001	reserved
1010	reserved
1011	reserved
1100	Advertise 1000BT full-duplex only (RGMII)
1101	Advertise 1000BT full- and half-duplex only (RGMII)
1110	Advertise all capabilites, except 1000BT half-duplex (RGMII)
1111	Advertise all capabilites (RGMII)

Strapping Pin

Single LED Mode

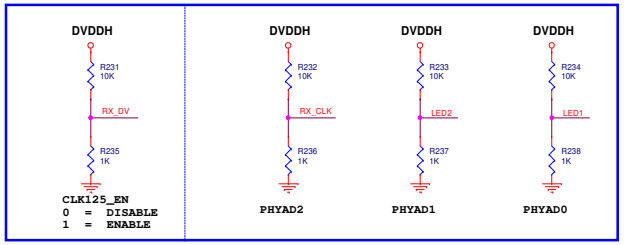
LED MODE



Single LED Mode

Pin	Description
LED2	1 : Link off 0 : Link on (any speed), solid color
LED1	Blinking : Activity (RX, TX)

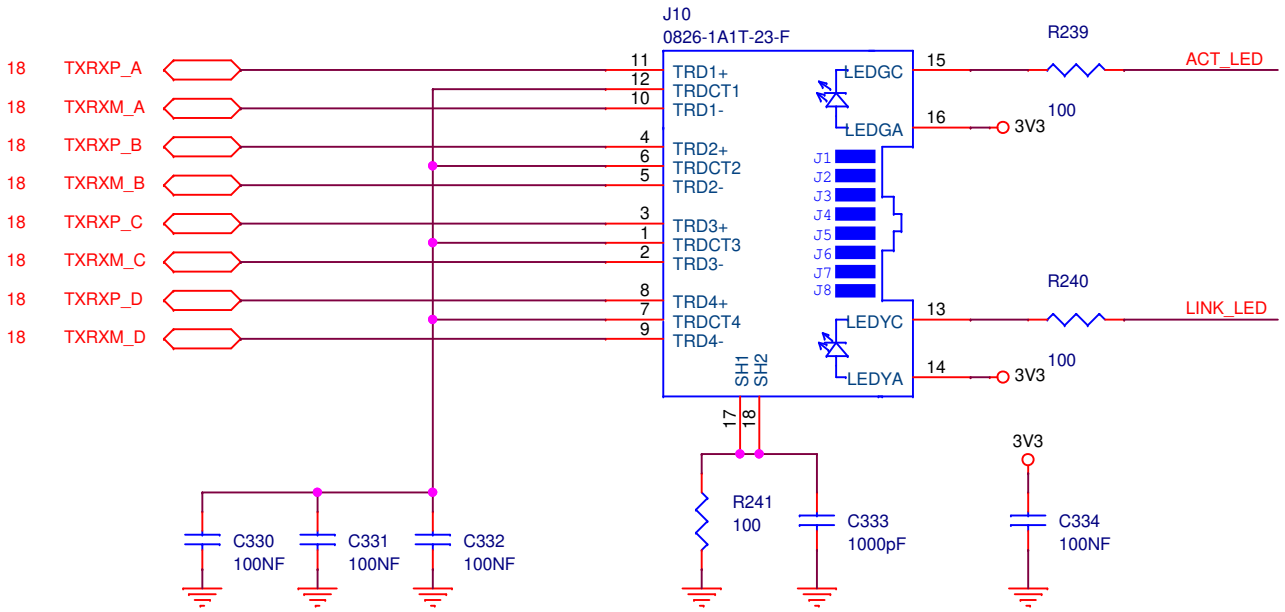
Strapping Pins

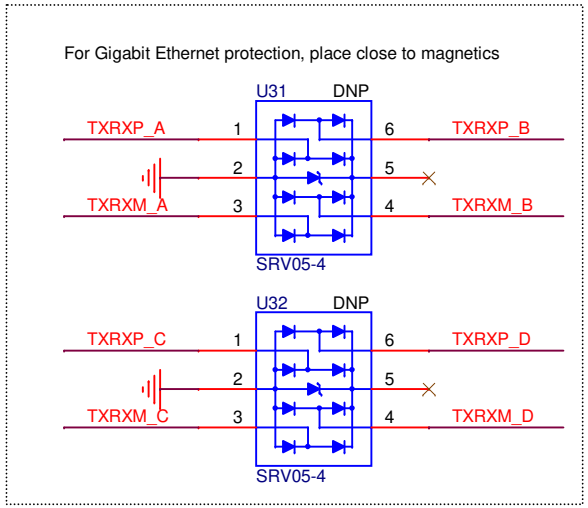


PROTO

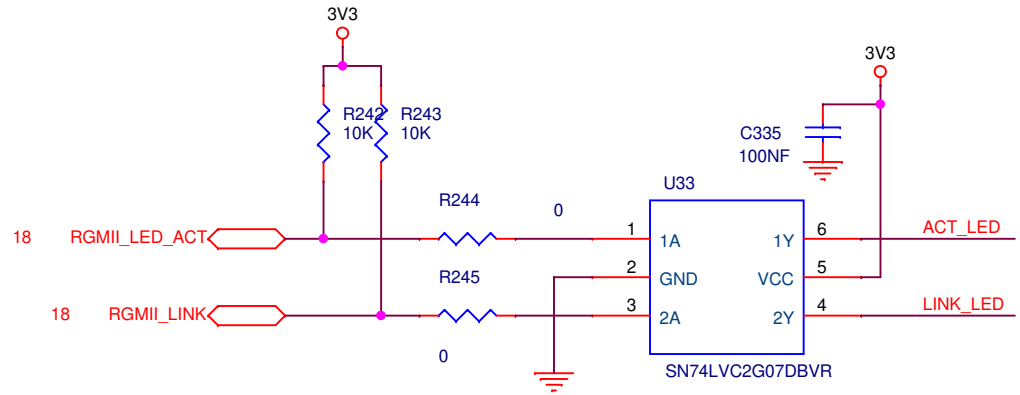
PPC Power Progress Community	Project: ACB_0001_0	
Creation Date: Friday, August 17, 2018	Last modify date: Saturday, September 28, 2019	Page title: EC1 PHY
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 18 of 42 / REV. 0 / Format A2

Gigabit Ethernet





Led Ethernet Buffer



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PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, August 17, 2018	Last modify date: Saturday, September 28, 2019	Page title: ETHERNET CONN		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
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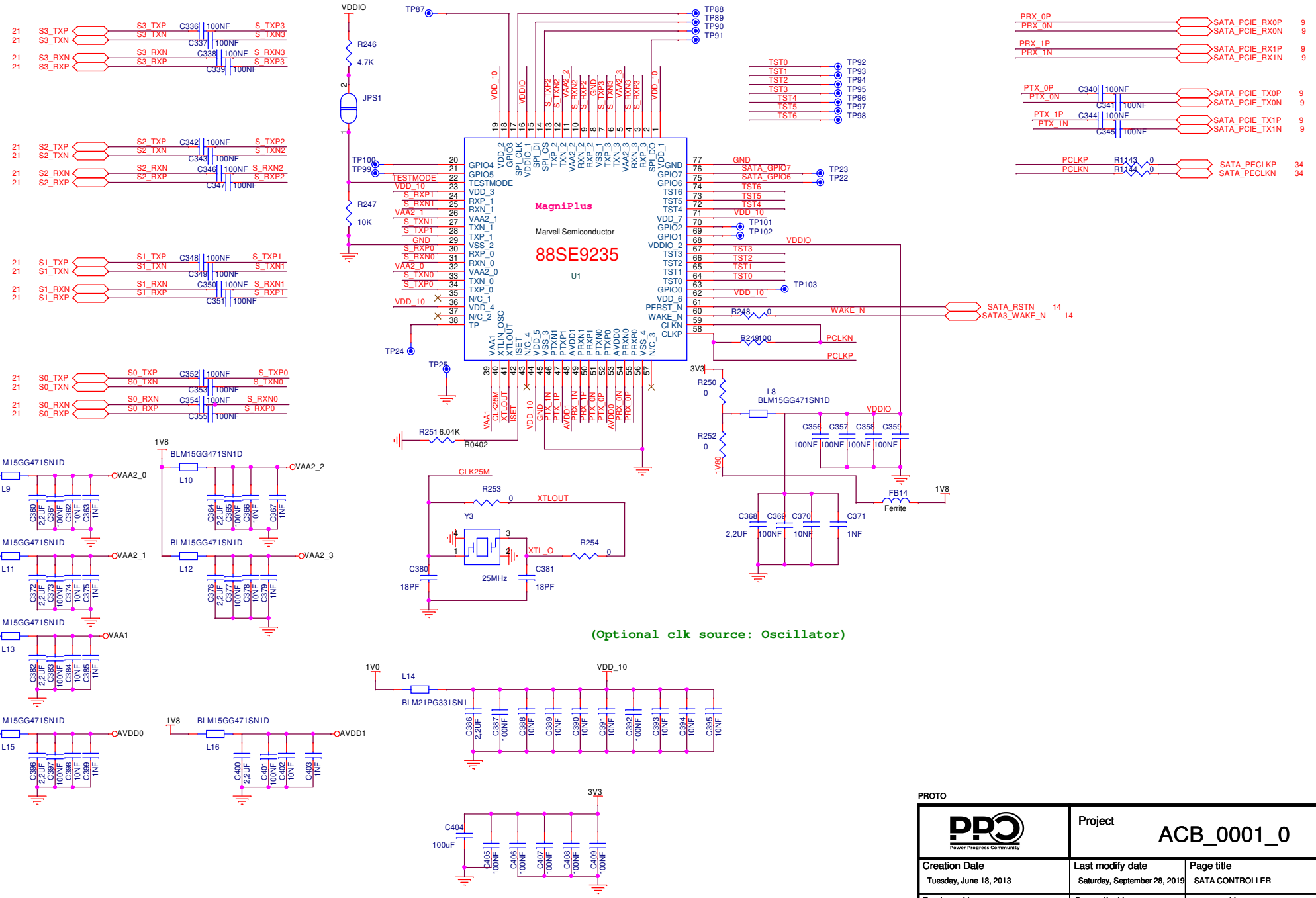
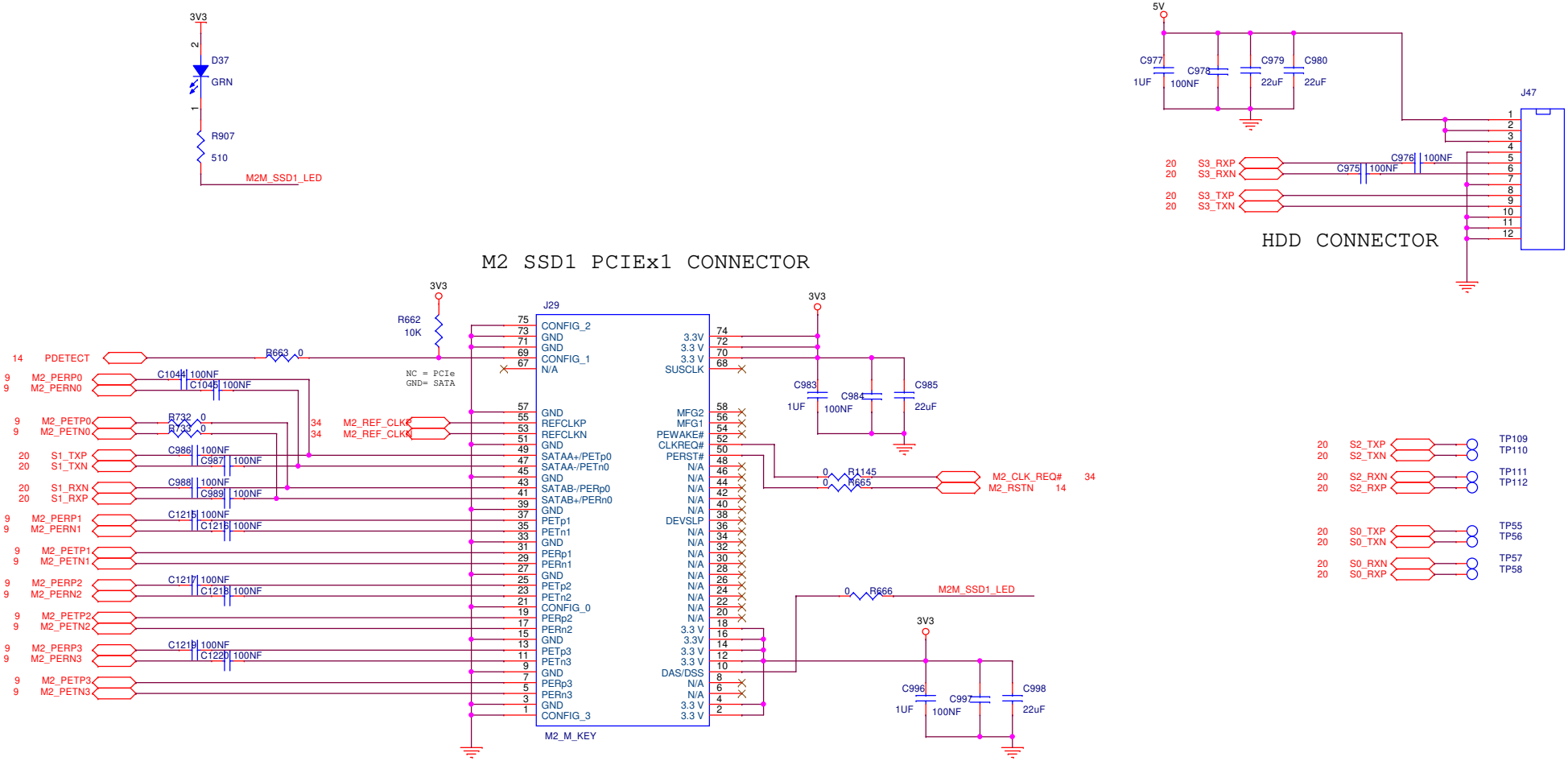
MagniPlus -SATA Interface



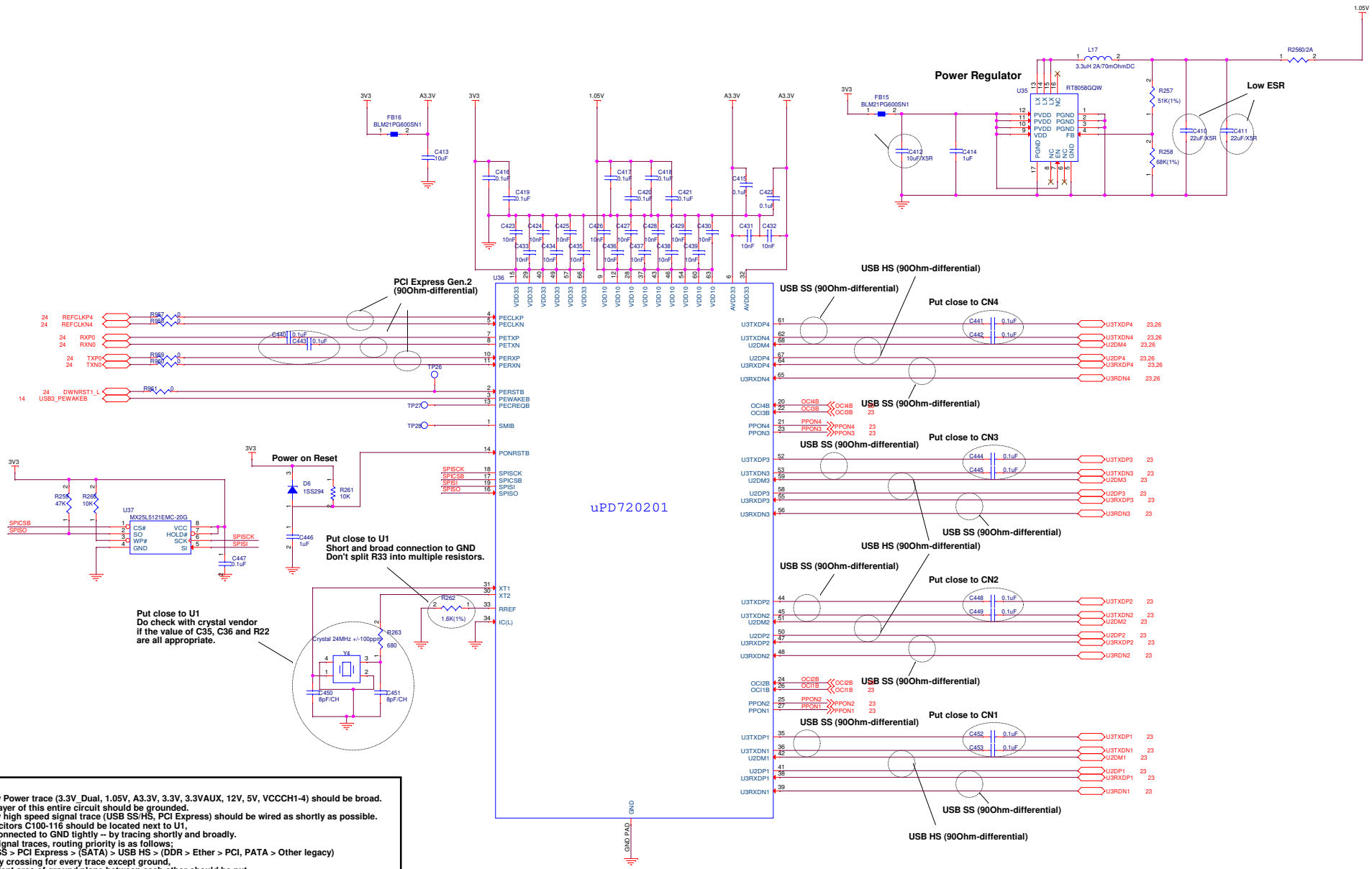
PROTO

PPC Power Progress Community	Project: ACB_0001_0	
Creation Date: Tuesday, June 18, 2013	Last modify date: Saturday, September 28, 2019	Page title: SATA CONTROLLER
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 20 of 42 / REV. 0 / Format A3



PROTO

PPC Power Progress Community	Project: ACB_0001_0	
Creation Date: Friday, November 30, 2018	Last modify date: Saturday, September 28, 2019	Page title: SATA CONNECTOR
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 21 of 42 / REV. 0 / Format A3



Note:

1. Every Power trace (3.3V_Dual, 1.05V, A3.3V, 3.3V, 3.3VAUX, 12V, 5V, VCCCH1-4) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express) should be wired as shortly as possible.
4. Capacitors C100-116 should be located next to U1,
   and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
   USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground,
   sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
   > Remove any impairment or discontinuity.
   > Keep same length by each other.
   > Keep same width and spacing.
8. The differential impedance of nominal value is as follows.
   > USB 3.0 / 2.0 --- 90ohm
   > PCI express Gen 1.(2.5GT/s) --- 100ohm PCI express Gen 2.(5GT/s) --- 85ohm

PCB trace impedance would be a non-continues value by its design rules.
The differential impedance adopt the nearest value that can be manufactured at PCB
For more information please refer to 'USB3.0 Board Design Guide' in design kit.

PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: USB3 CONTROLLER
Designed by:	Controlled by:	approved by:
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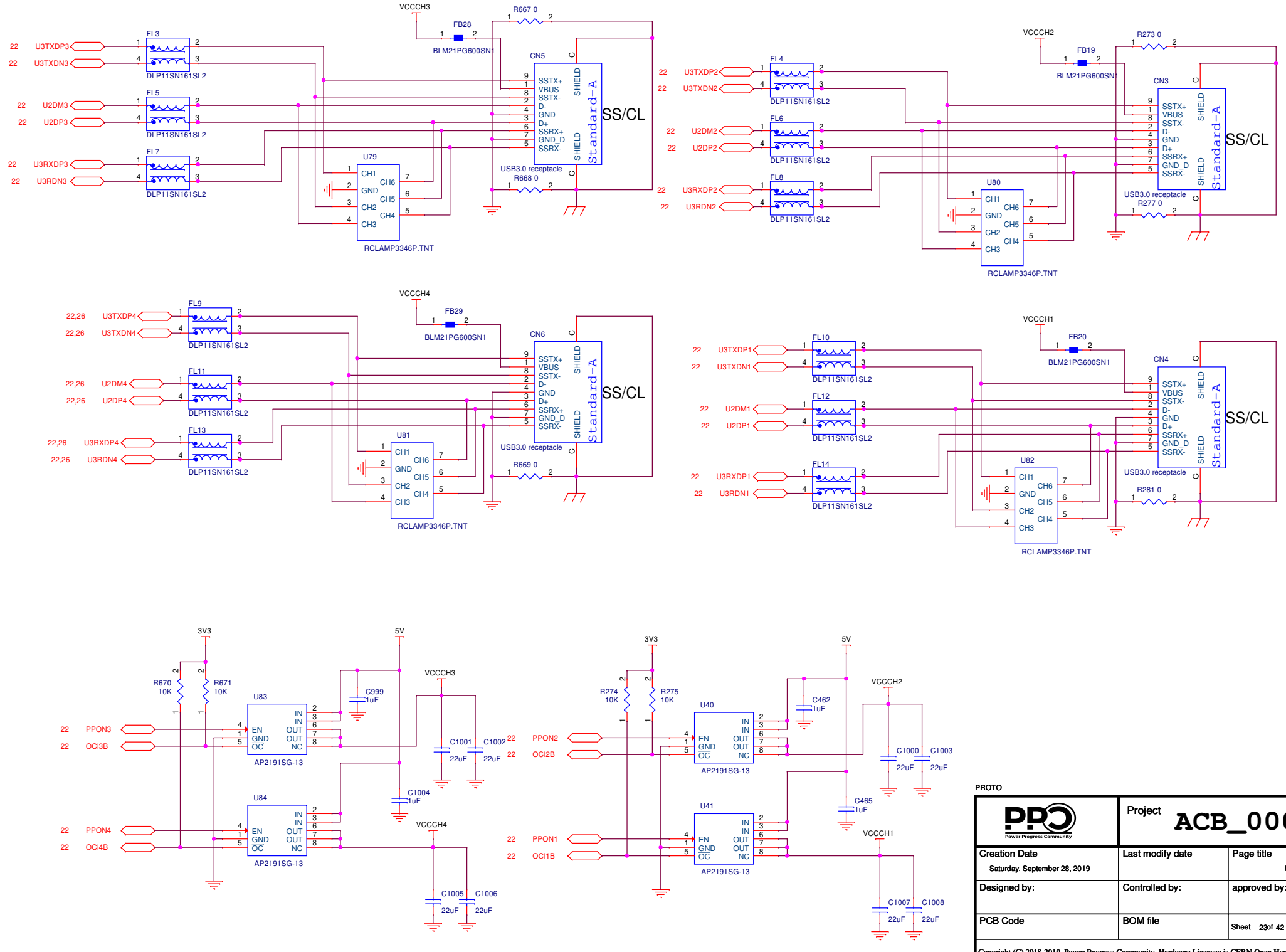

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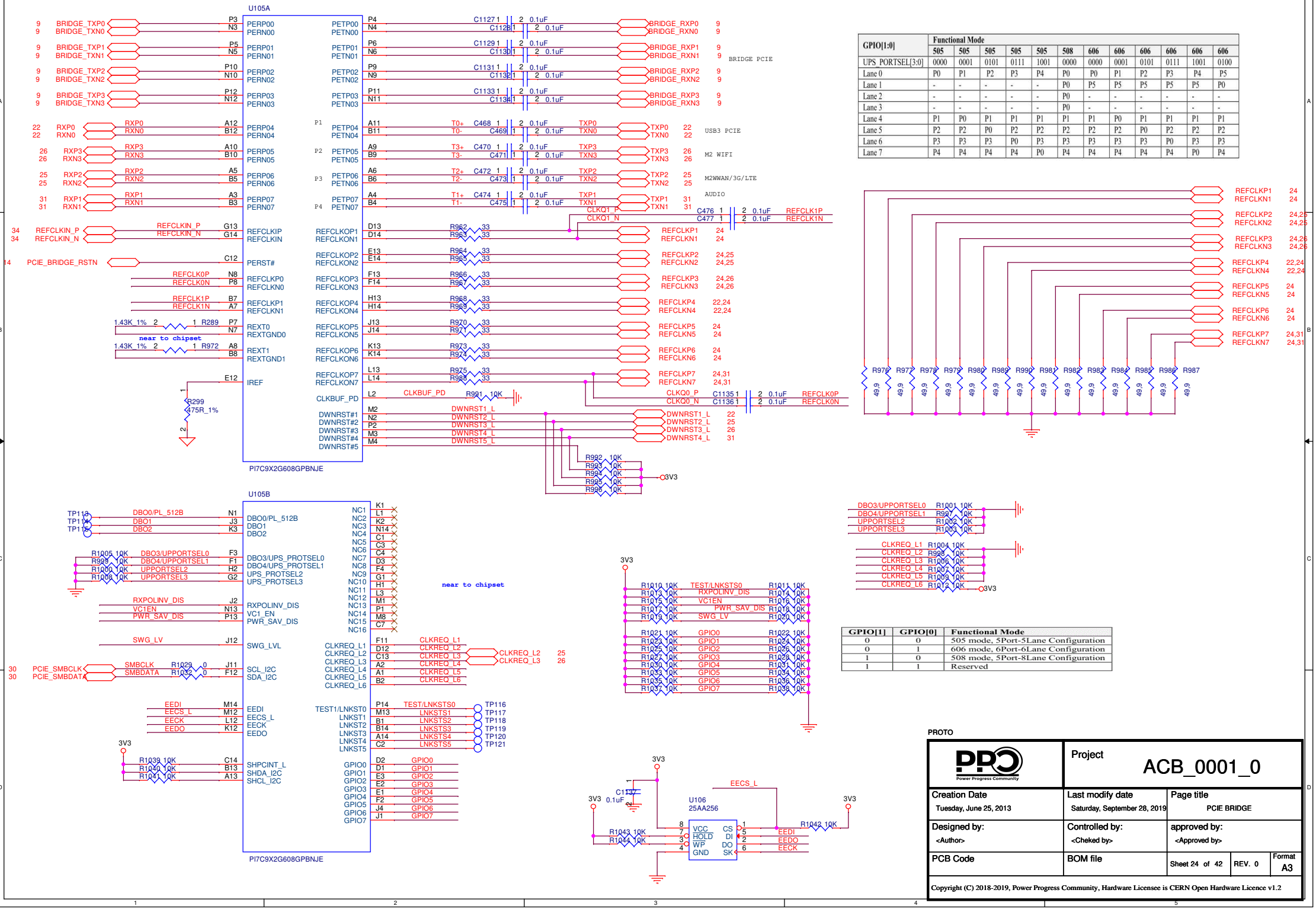
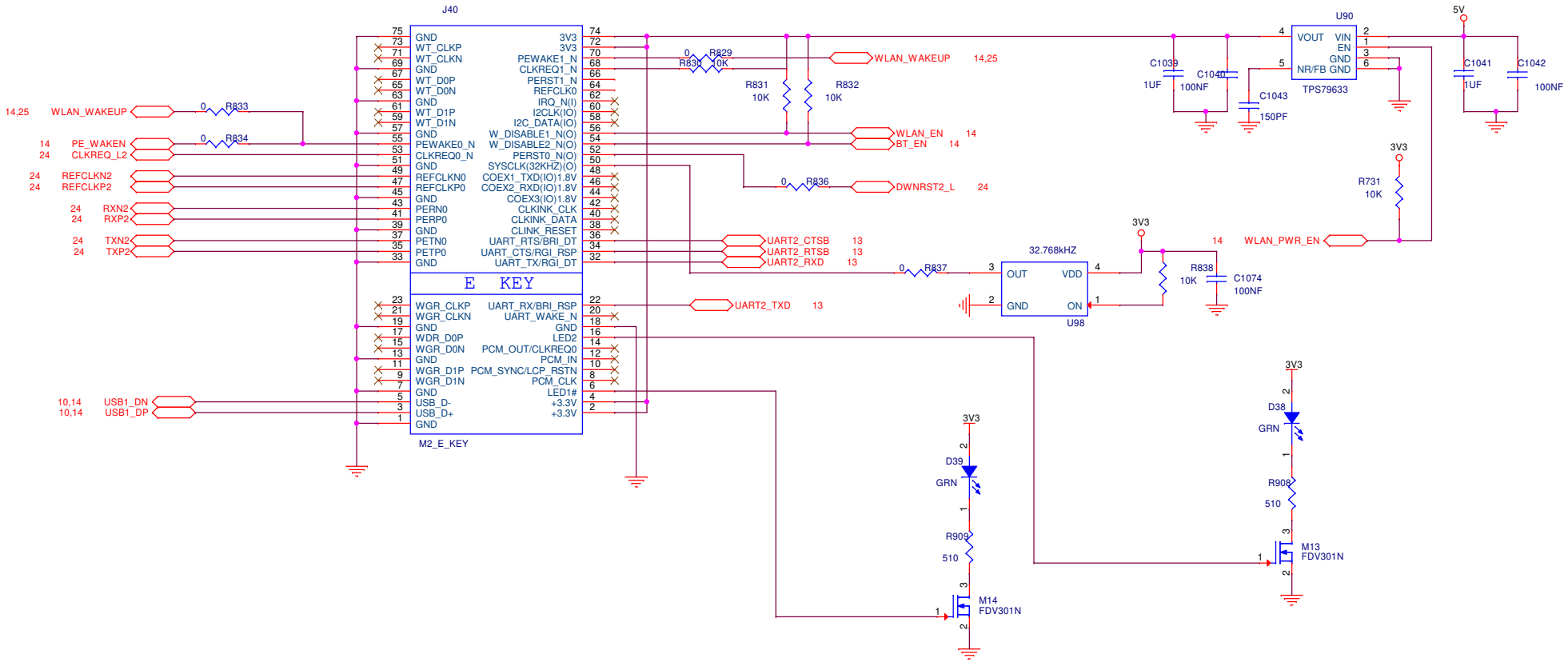
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: USB3 PORTS
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 23of 42 / REV. 0 / Format A3



GPIO[1:0]	Functional Mode											
	505	505	505	505	505	508	606	606	606	606	606	606
UPS_PORTSEL[3:0]	0000	0001	0101	0111	1001	0000	0000	0001	0101	0111	1001	0100
Lane 0	P0	P1	P2	P3	P4	P0	P0	P1	P2	P3	P4	P5
Lane 1	-	-	-	-	-	P0	P5	P5	P5	P5	P5	P0
Lane 2	-	-	-	-	-	P0	-	-	-	-	-	-
Lane 3	-	-	-	-	-	P0	-	-	-	-	-	-
Lane 4	P1	P0	P1	P1	P1	P1	P1	P0	P1	P1	P1	P1
Lane 5	P2	P2	P0	P2	P2	P2	P2	P2	P0	P2	P2	P2
Lane 6	P3	P3	P3	P0	P3	P3	P3	P3	P3	P0	P3	P3
Lane 7	P4	P4	P4	P4	P0	P4	P4	P4	P4	P4	P0	P4

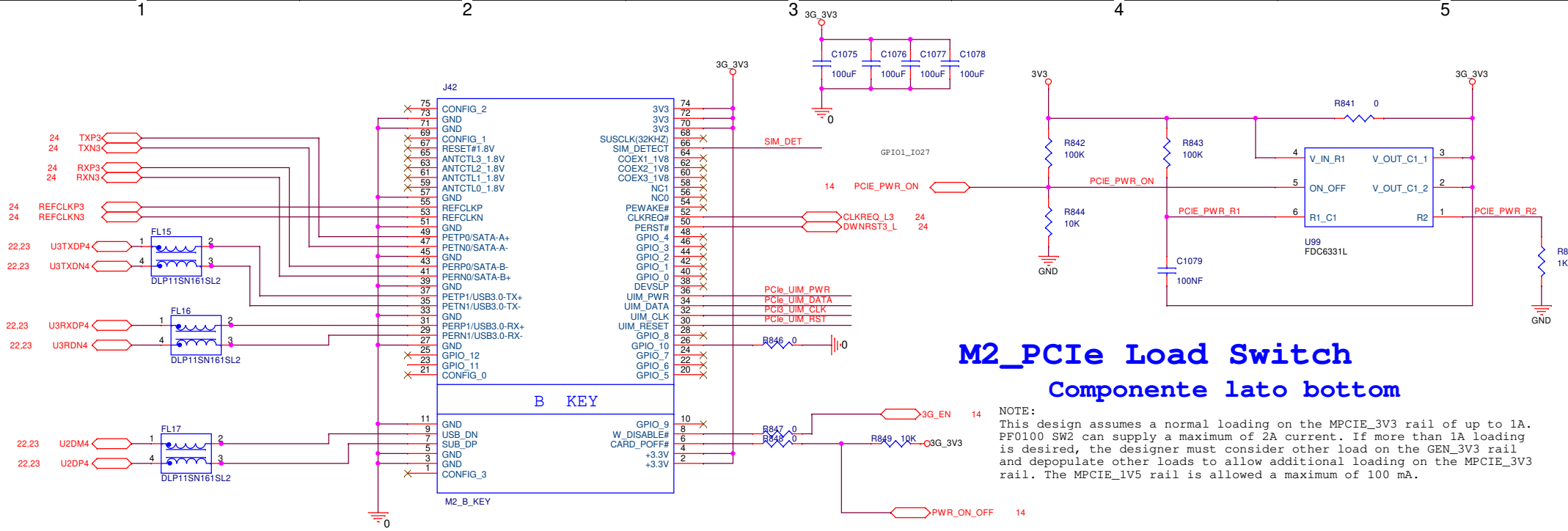
GPIO[1]	GPIO[0]	Functional Mode
0	0	505 mode, 5Port-5Lane Configuration
0	1	606 mode, 6Port-6Lane Configuration
1	0	508 mode, 5Port-8Lane Configuration
1	1	Reserved

M2 WLAN+BT PCIEx1 CONNECTOR



PROTO

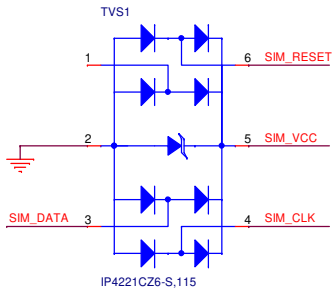
PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Friday, December 28, 2018	Last modify date: Saturday, September 28, 2019	Page title: M2.WLAN CONNECTOR
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 25 of 42 / REV. 0 / Format A3

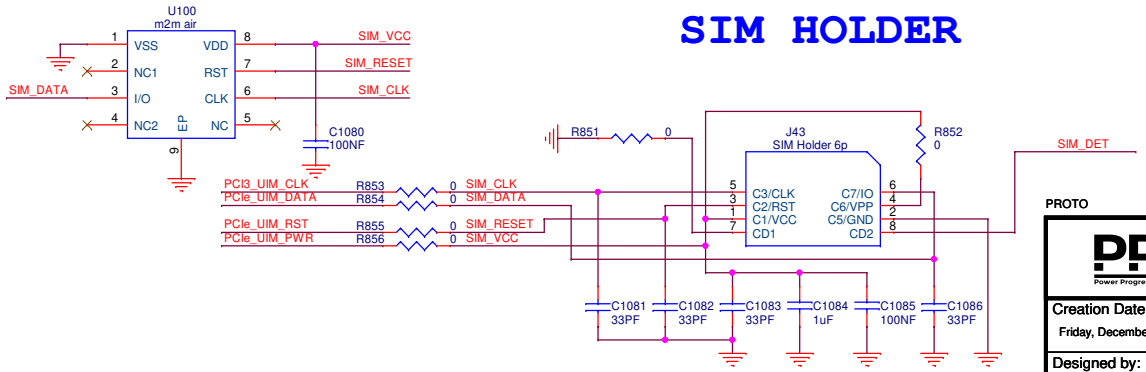


M2_PCIe Load Switch

Componente lato bottom

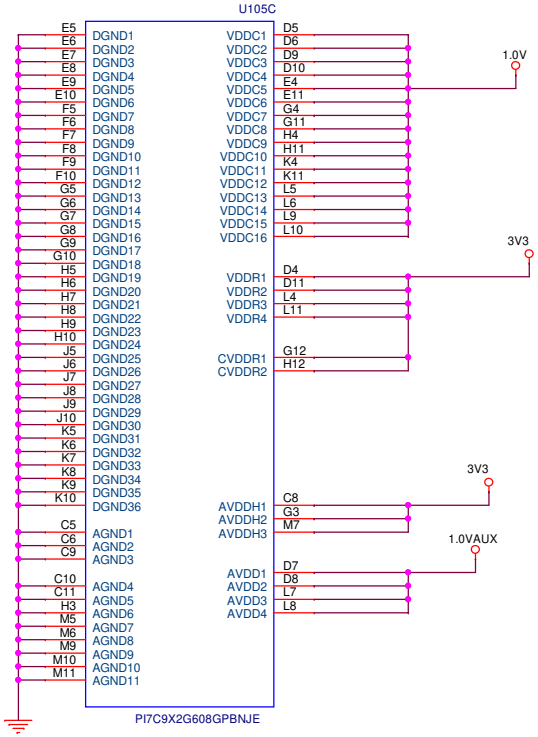
NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.



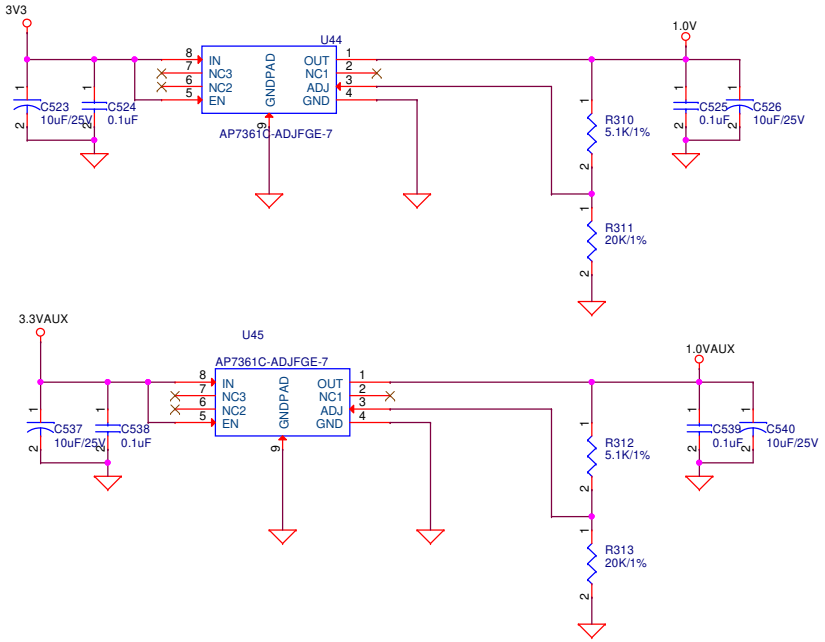


PROTO

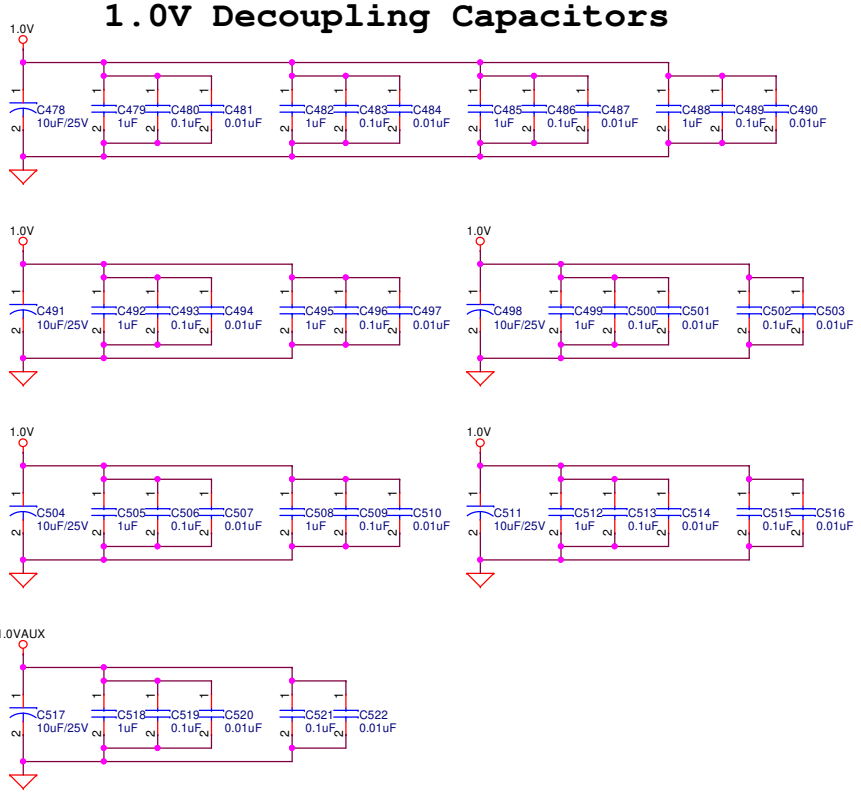
Power Progress Community	Project: ACB_0001_0	
Creation Date: Friday, December 28, 2018	Last modify date: Saturday, September 28, 2019	Page title: 3G/LTE MODEM
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 26 of 42 / REV. 0 / Format A3



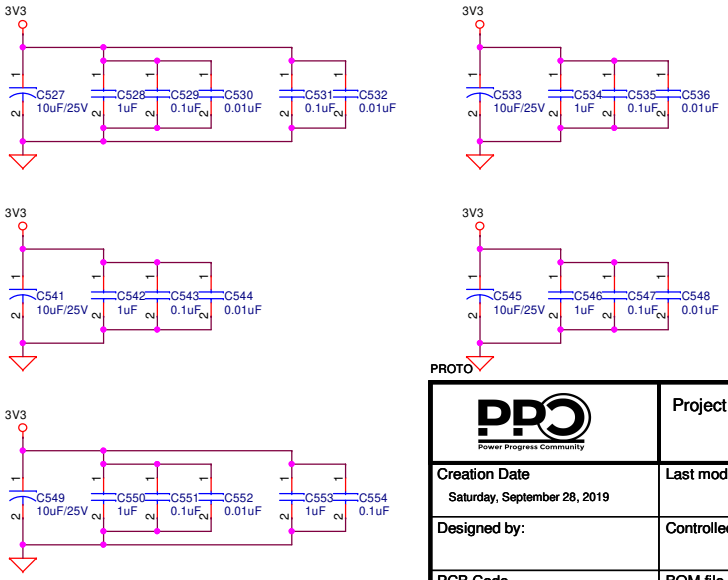
3.3V to 1.0V LDO



1.0V Decoupling Capacitors

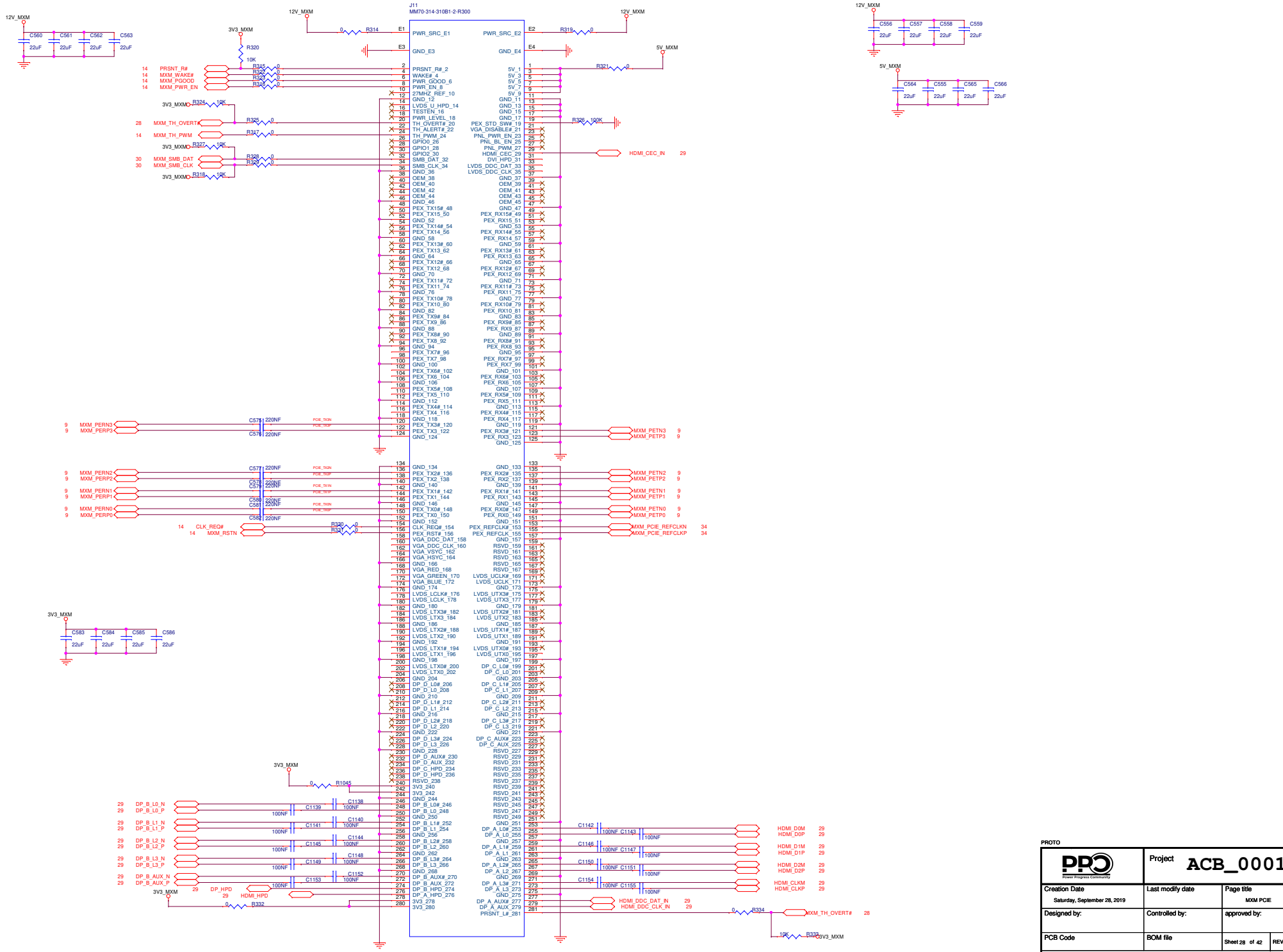


3.3V Decoupling Capacitors



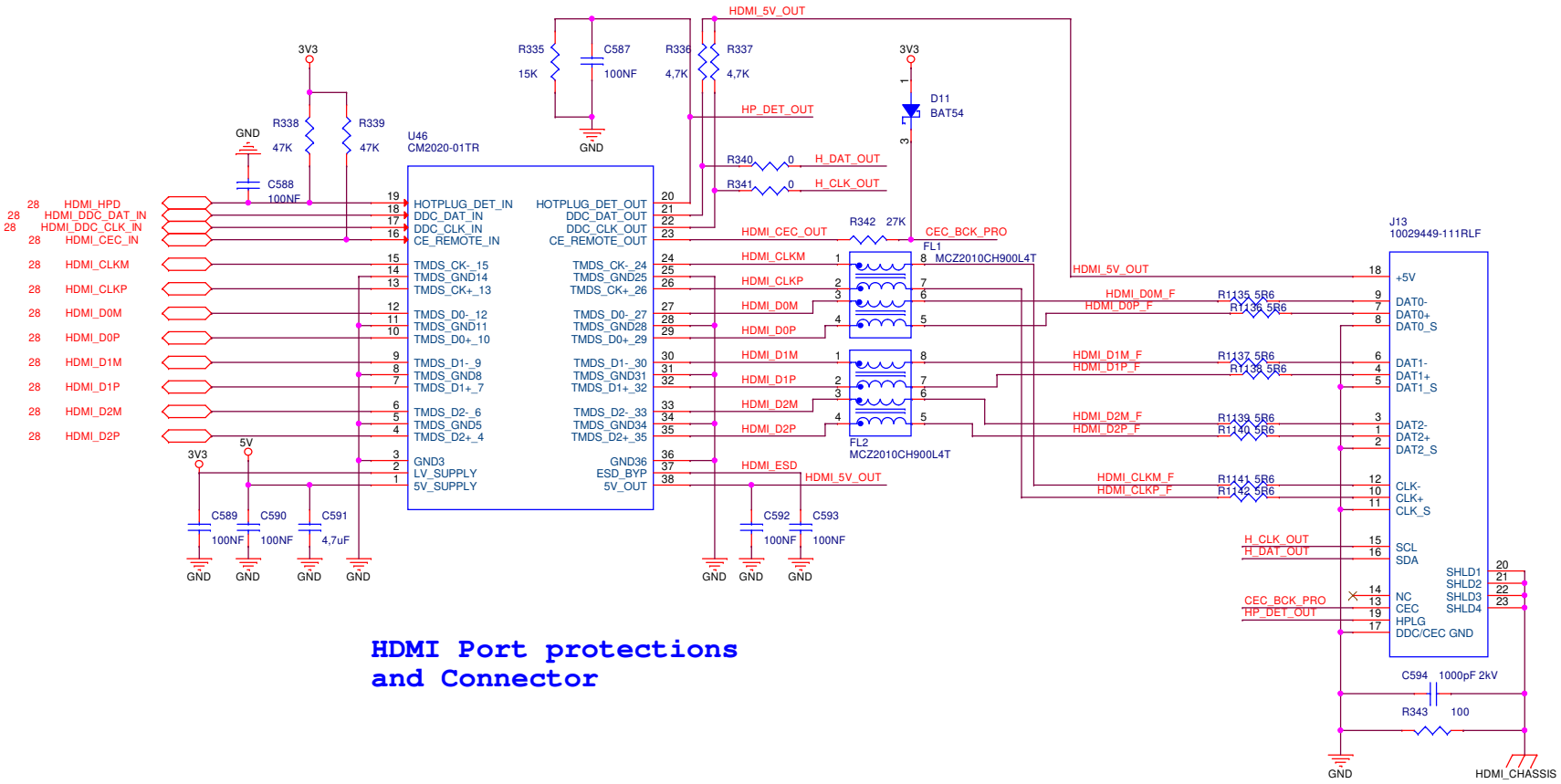
PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PCIE BRIDGE POWER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 27 of 42 / REV. 0 / Format A3

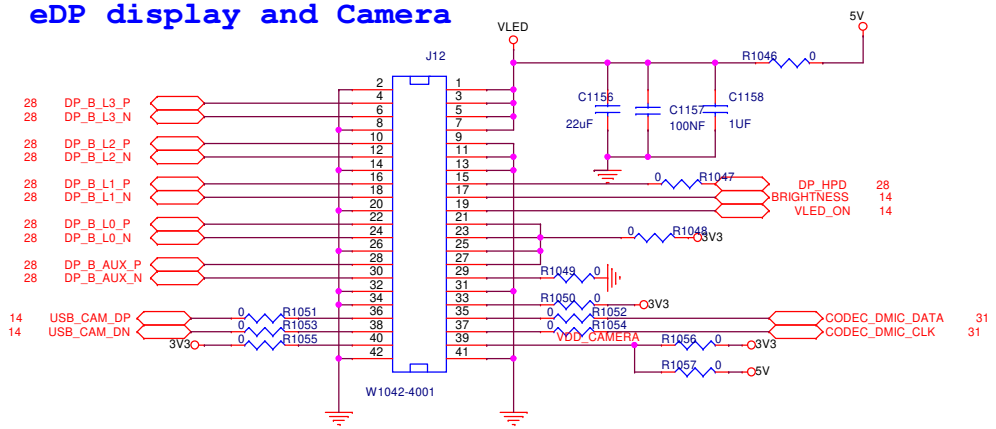


PROTO

Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: MXM PCIE
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 28 of 42 · REV. 0 · Format A2

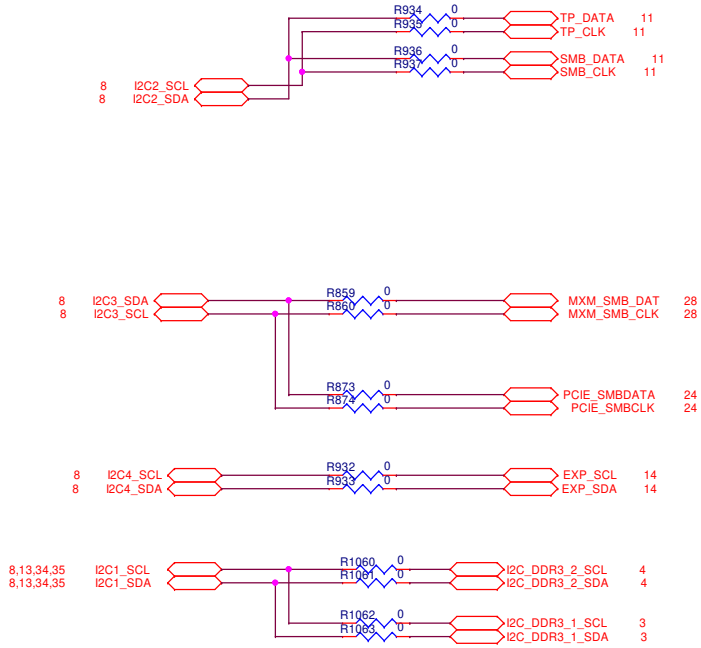


HDMI Port protections and Connector



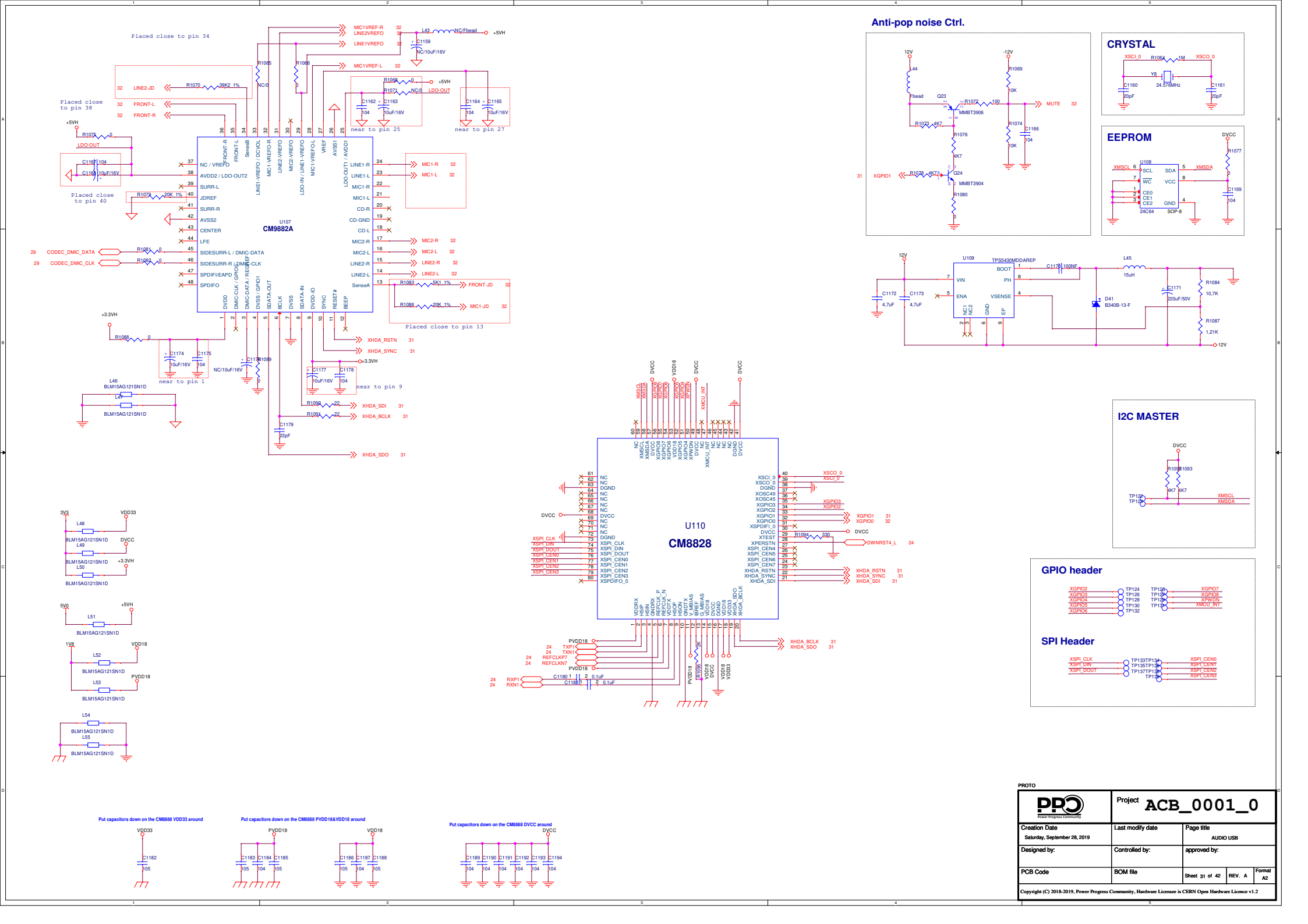
PROTO

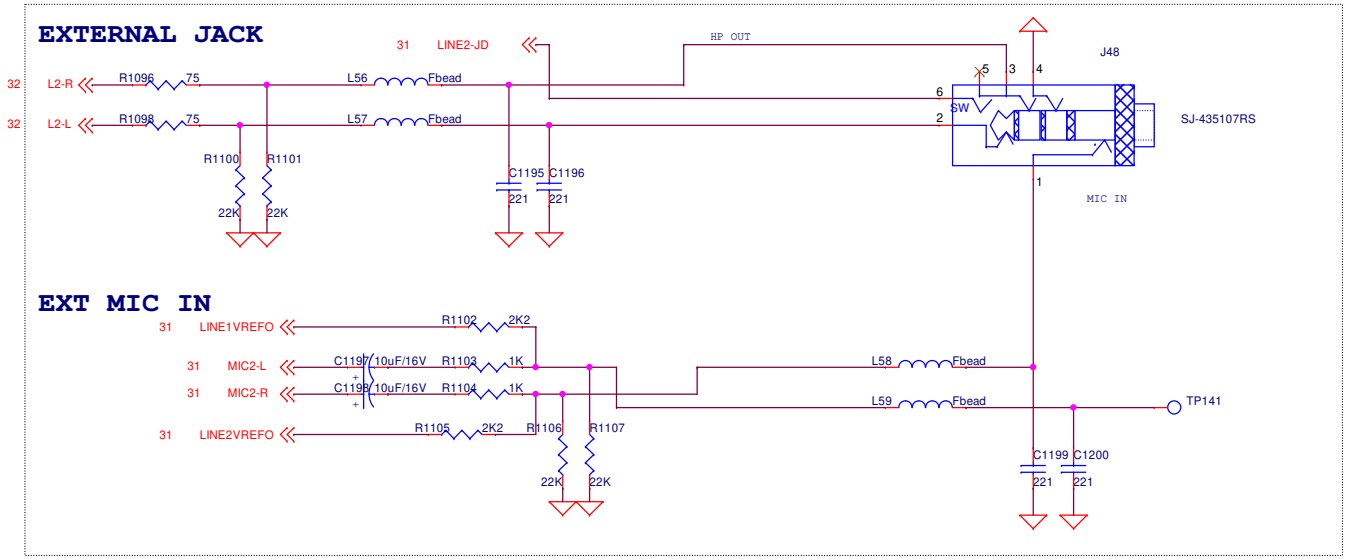
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: MXM VIDEO OUT
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 29 of 42 / REV. A / Format A3

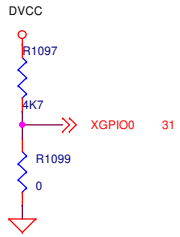


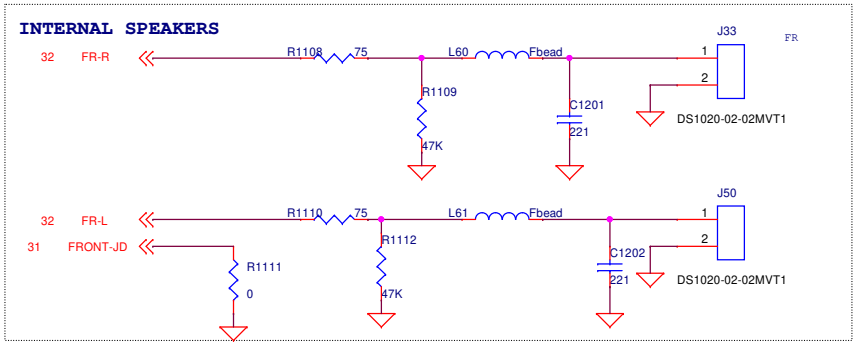
PROTO

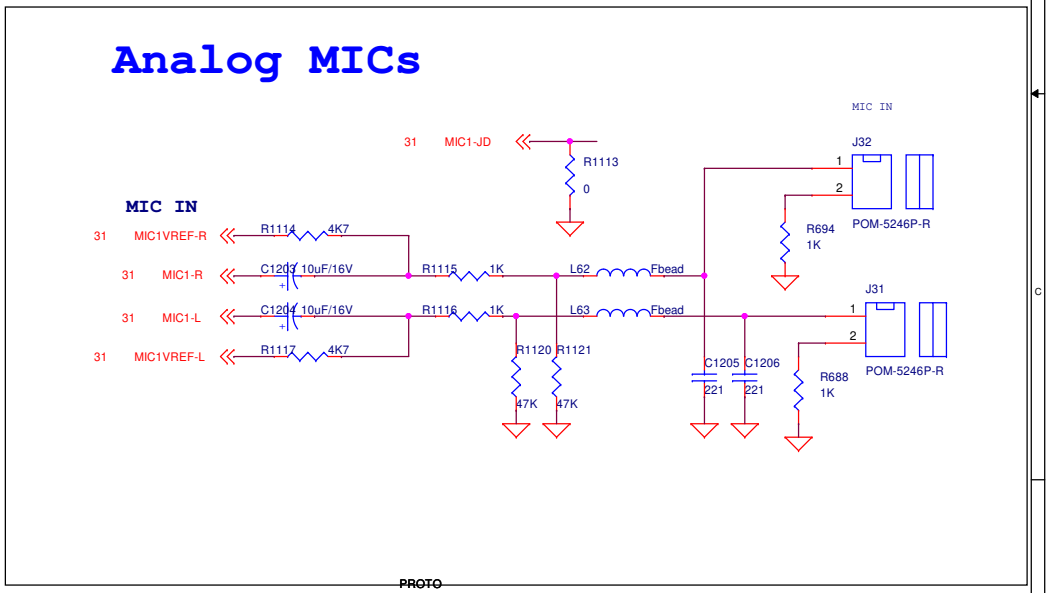
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: I2C WRAP
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 30 of 42 / REV. 0 / Format A3

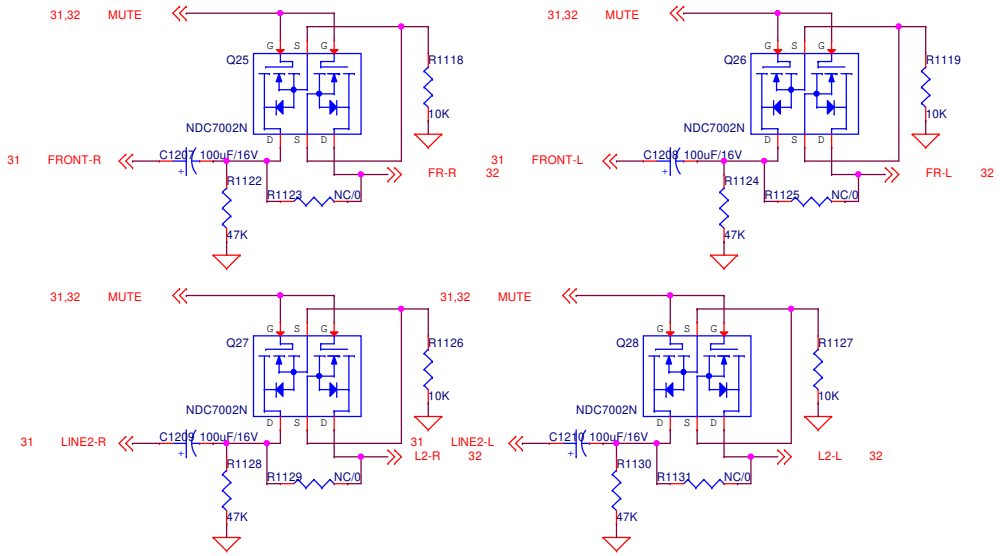

Anti-pop noise Ctrl.
CRYSTAL
EEPROM
I2C MASTER
GPIO header
SPI Header
U107
CM9882A
U110
CM8828
U109
TPS5430MDDAREP
Placed close to pin 34
Placed close to pin 38
Placed close to pin 40
Placed close to pin 13
near to pin 25
near to pin 27
near to pin 1
near to pin 9
Put capacitors down on the CM8888 VDD33 around
Put capacitors down on the CM8888 PVDD18&VDD18 around
Put capacitors down on the CM8888 DVCC around
PROTO
Project ACB_0001_0
Creation Date
Saturday, September 28, 2019
Last modify date
Page title
AUDIO USB
Designed by:
Controlled by:
approved by:
PCB Code
BOM file
Sheet 31 of 42
REV. A
Format A2
Copyright (C) 2018-2019, Power Progress Community, Hardware Licensee is CERN Open Hardware Licence v1.2







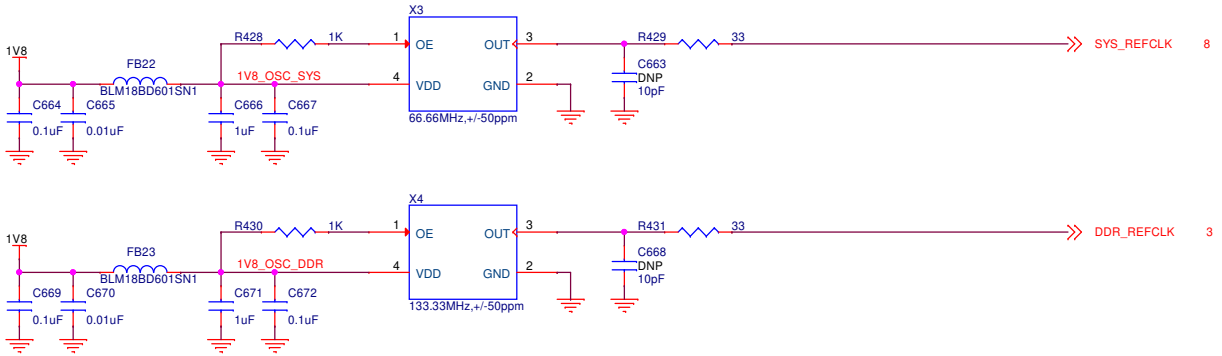




PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: AUDIO CONN
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 32 of 42 / REV. 0 / Format A3

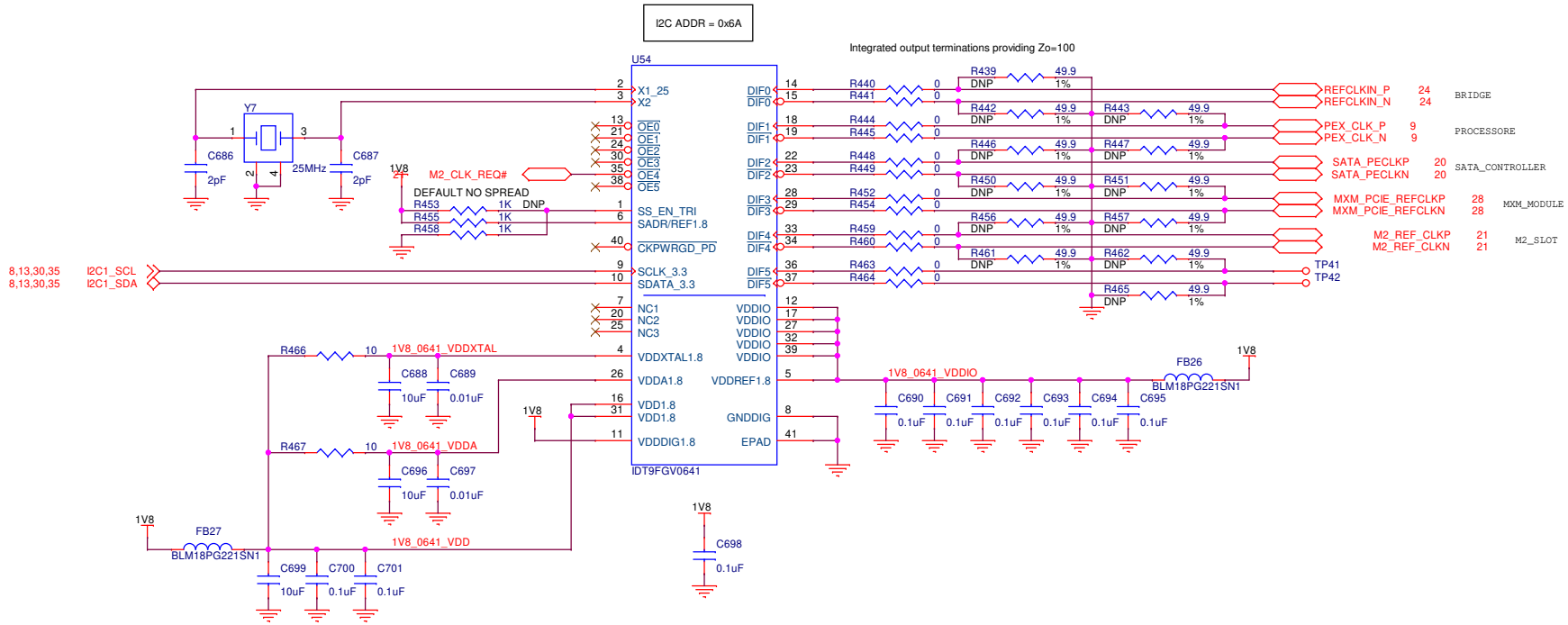
SYSTEM CLOCK GENERATORs



PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: CLOCK 1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 33 of 42 / REV. 0 / Format A3

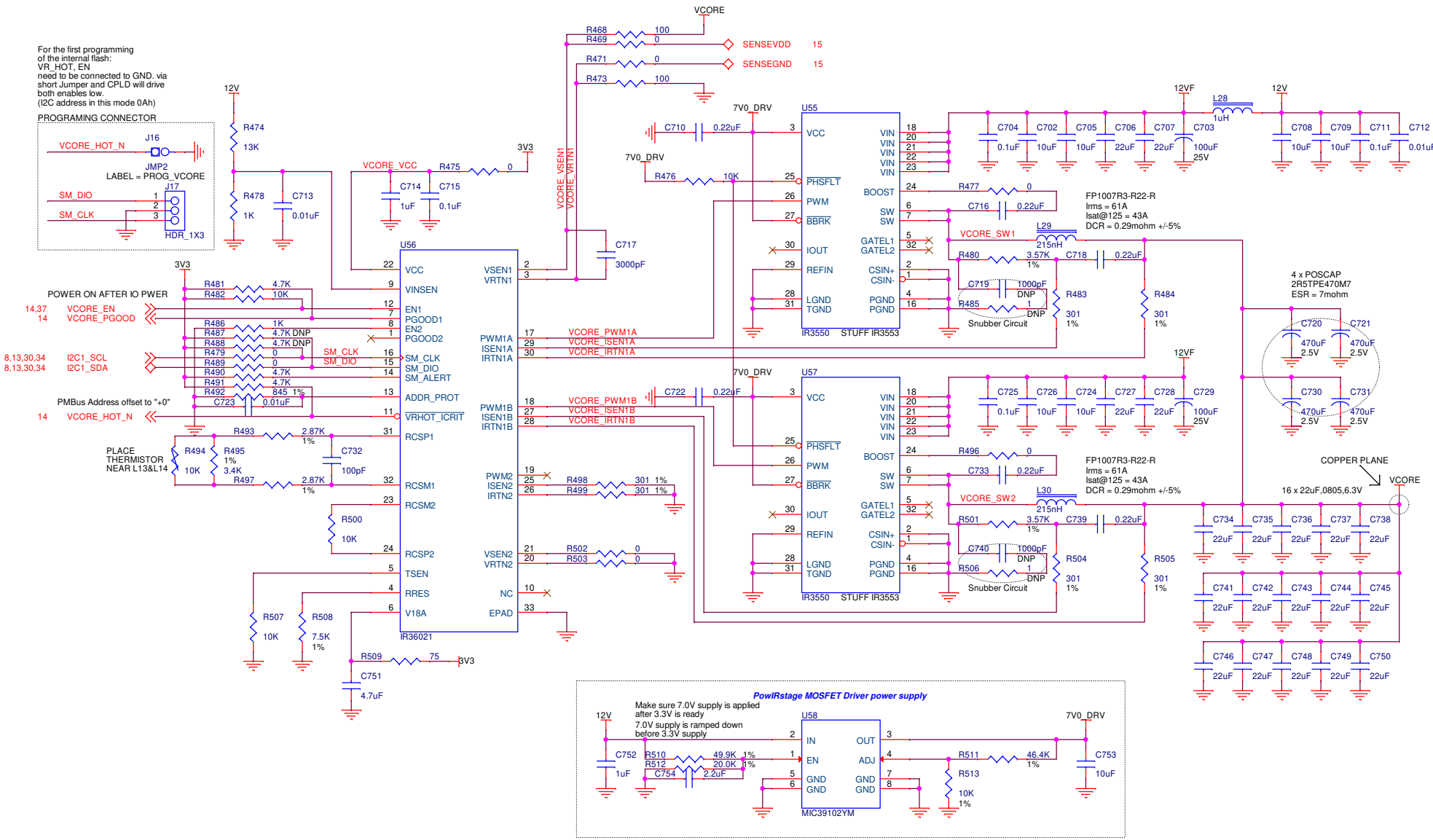
SYSTEM CLOCK GENERATORs (cont.)



PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: CLOCK 2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 34 of 42 / REV. 0 / Format A3

T2080 CORE POWER CONVERTOR

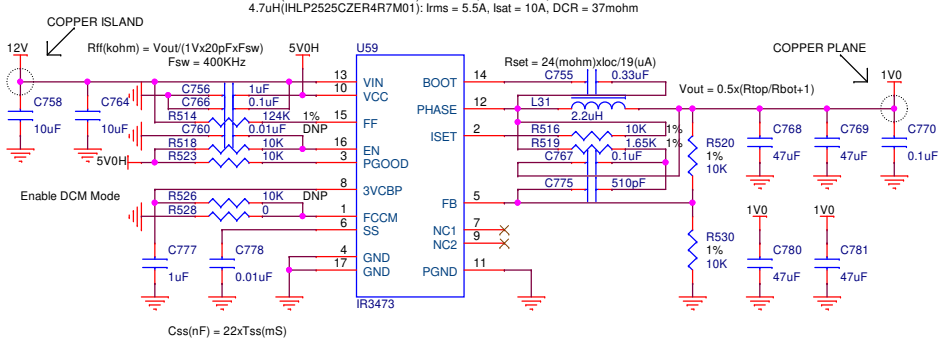


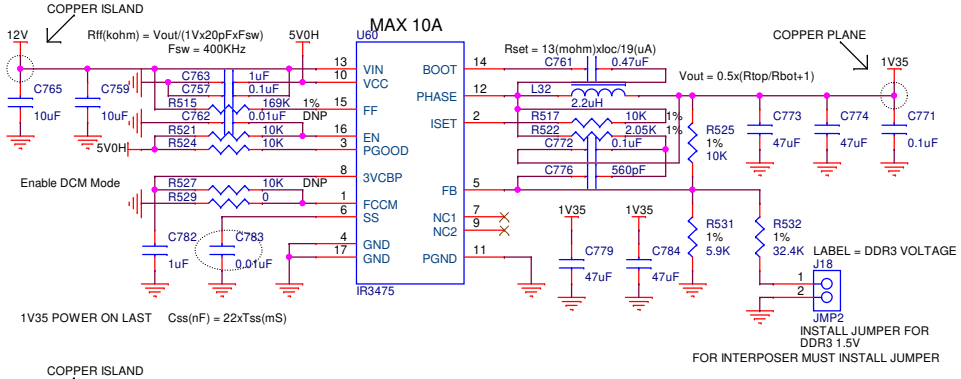
PROTO

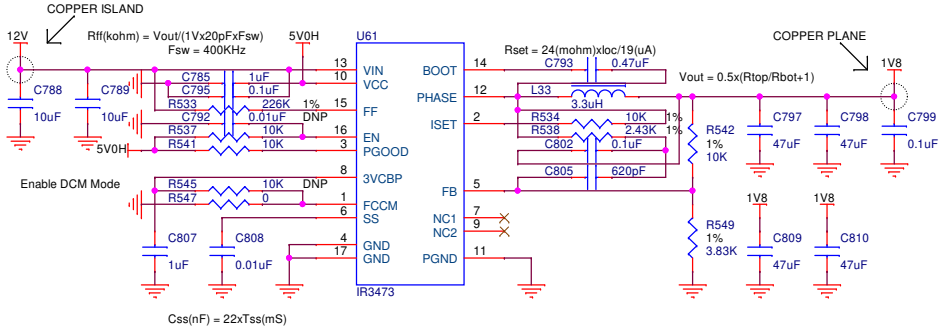
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: CORE PWR
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 35 of 42 / REV. 0 / Format A3

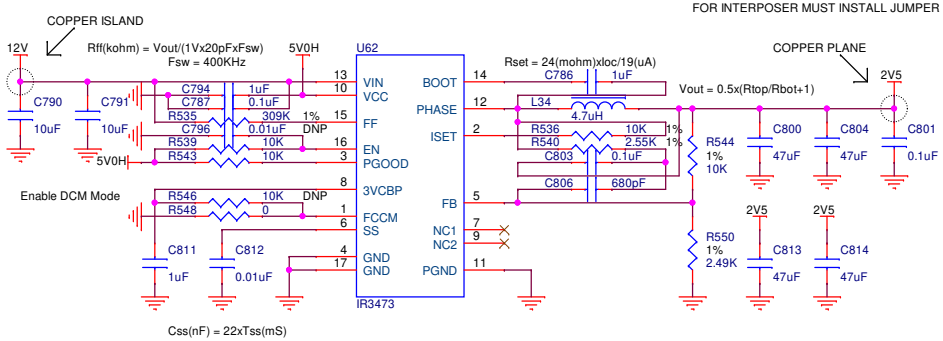
SYSTEM POWER CONVERTORs

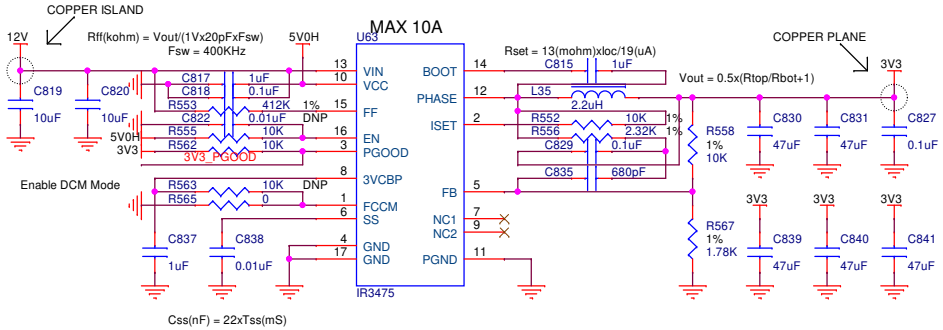
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

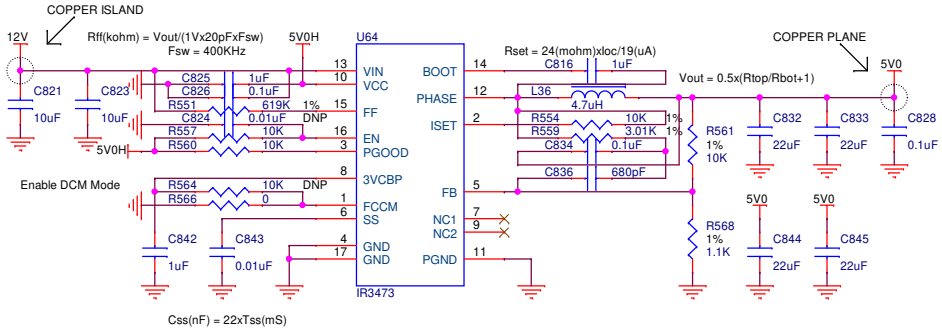




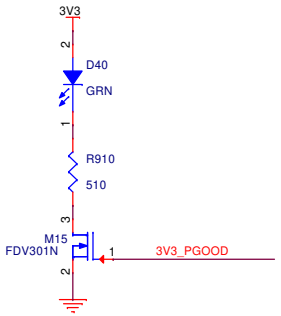








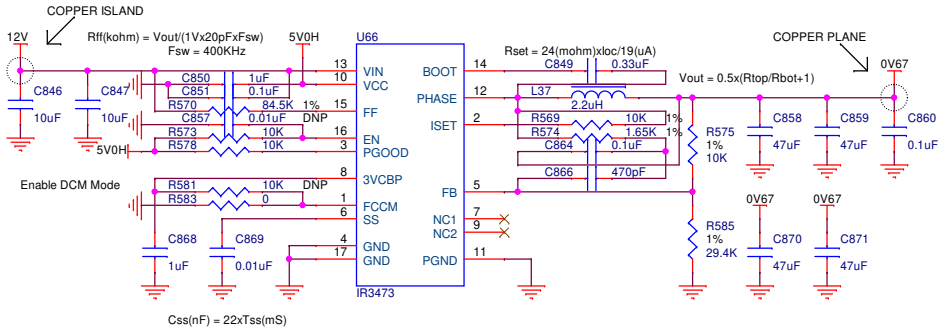
Caution: separate analog and power ground and make connection at GND plane

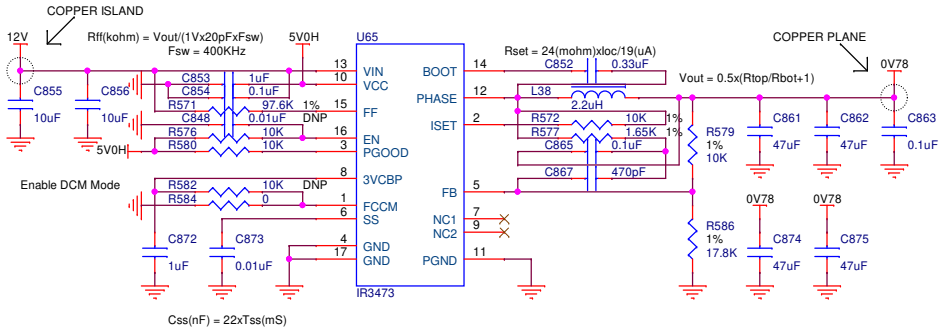


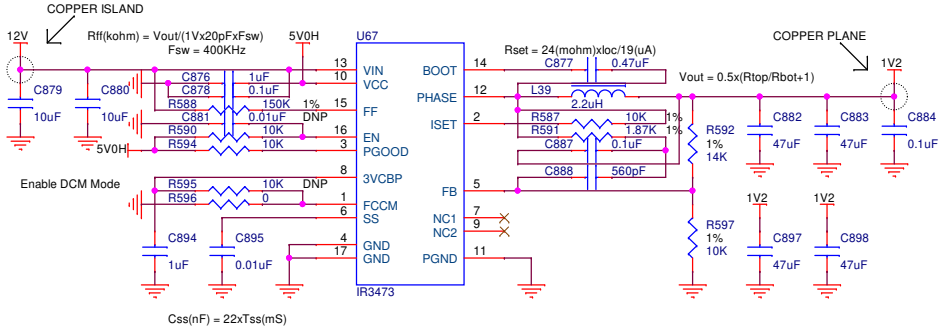
PROTO

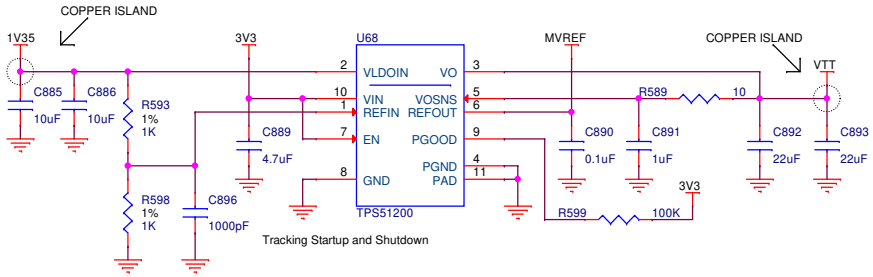
PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: OTHER PWR1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 36 of 42 / REV. 0 / Format A3

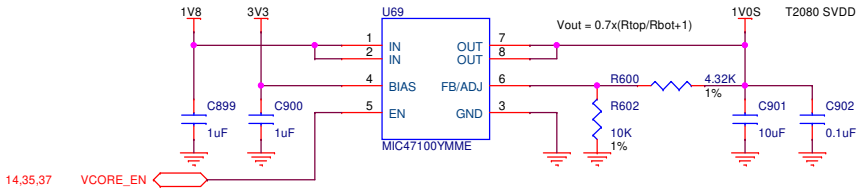
SYSTEM POWER CONVERTORs (cont.)

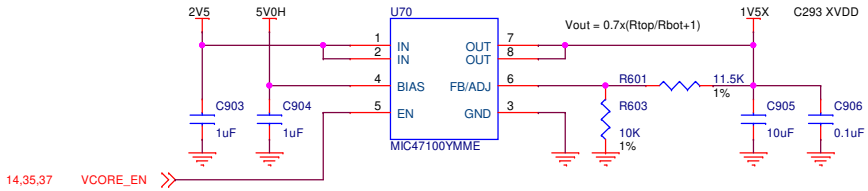


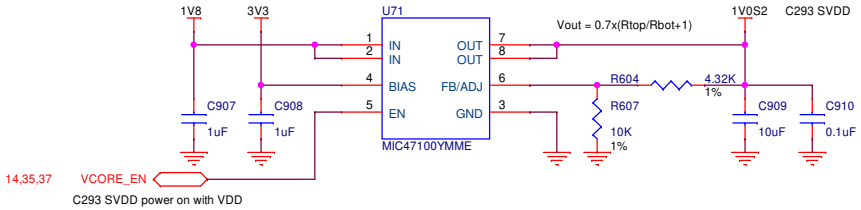


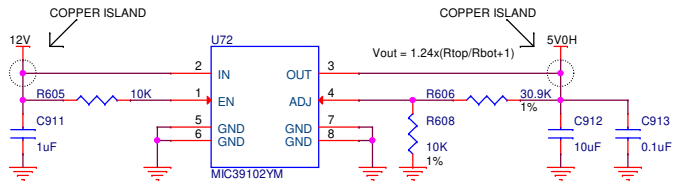












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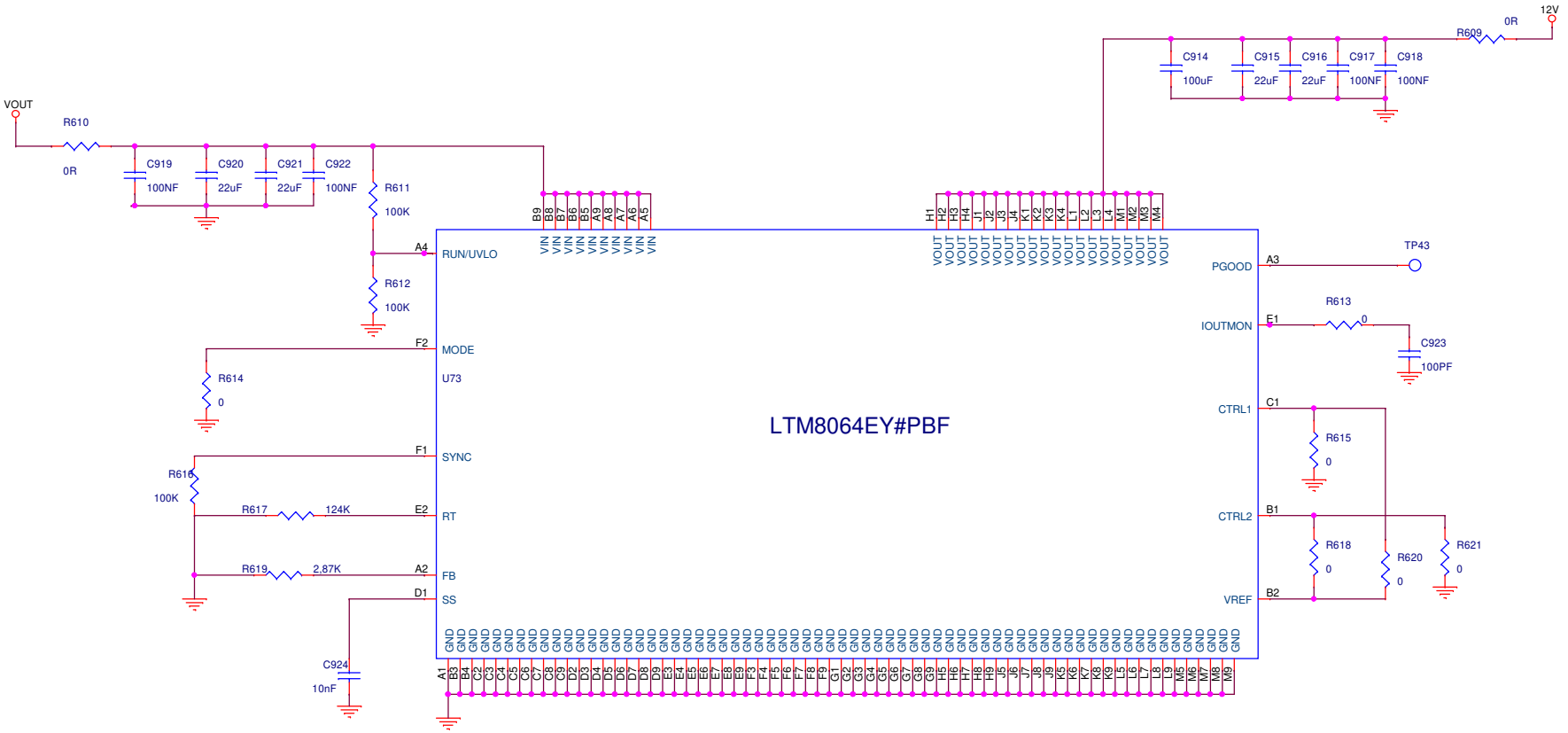
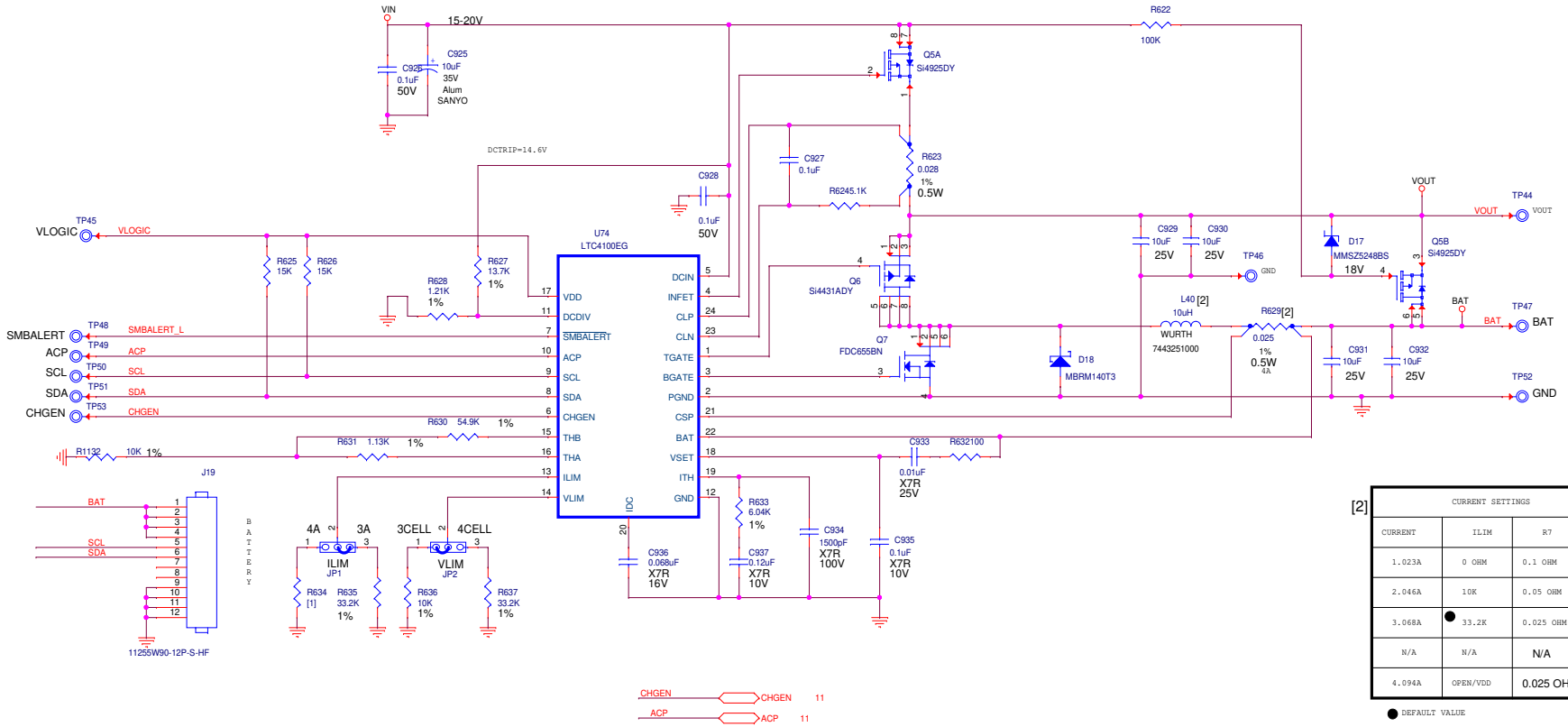
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: OTHER PWR2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 37 of 42 / REV. 0 / Format A3



PROTO

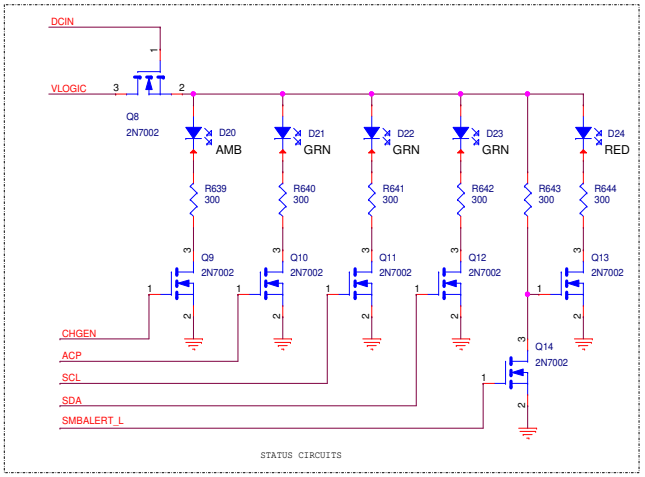
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: MAIN POWER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 38 of 42 / REV. 0 / Format A3

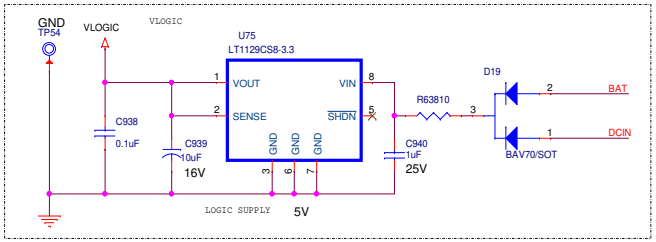


[2]

CURRENT SETTINGS				VOLTAGE SETTINGS	
CURRENT	ILIM	R7	L1	VOLTAGE	VLIM
1.023A	0 OHM	0.1 OHM	40uH	8.438V	0 OHM
2.046A	10K	0.05 OHM	20uH	12.646V	● 10K
3.068A	● 33.2K	0.025 OHM	10uH	16.870V	33.2K
N/A	N/A	N/A	N/A	21.062V	100K
4.094A	OPEN/VDD	0.025 OHM	10uH	32.758V	OPEN/VDD

● DEFAULT VALUE

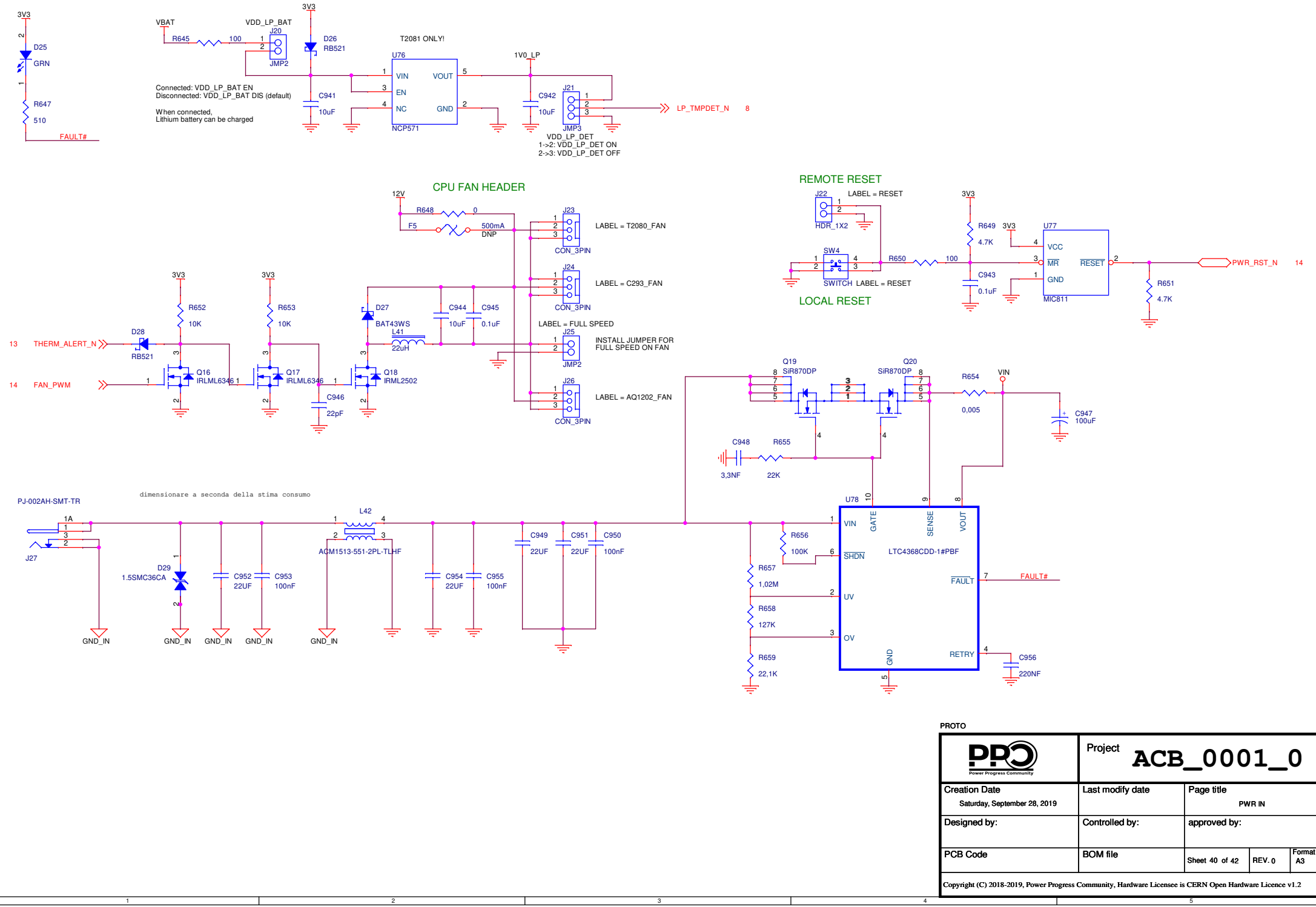




PROTO

PPC Power Progress Community	Project: ACB_0001_0		
Creation Date: Wednesday, August 08, 2018	Last modify date: Saturday, September 28, 2019	Page title: BATTERY CHARGE	
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 39 of 42	REV. 0 / Format: Custom

SYSTEM POWER INPUT



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PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Saturday, September 28, 2019	Last modify date	Page title: PWR IN
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PPC Power Progress Community	Project **T2080PCIe**			
Creation Date Saturday, September 28, 2019	Last modify date	Page title MECANICAL		
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CHANGE LIST

PROTO

Power Progress Community	Project **ACB_0001_0**	
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PCB Code	BOM file	Sheet 42 of 42 / REV. 0 / Format B