


Page Description

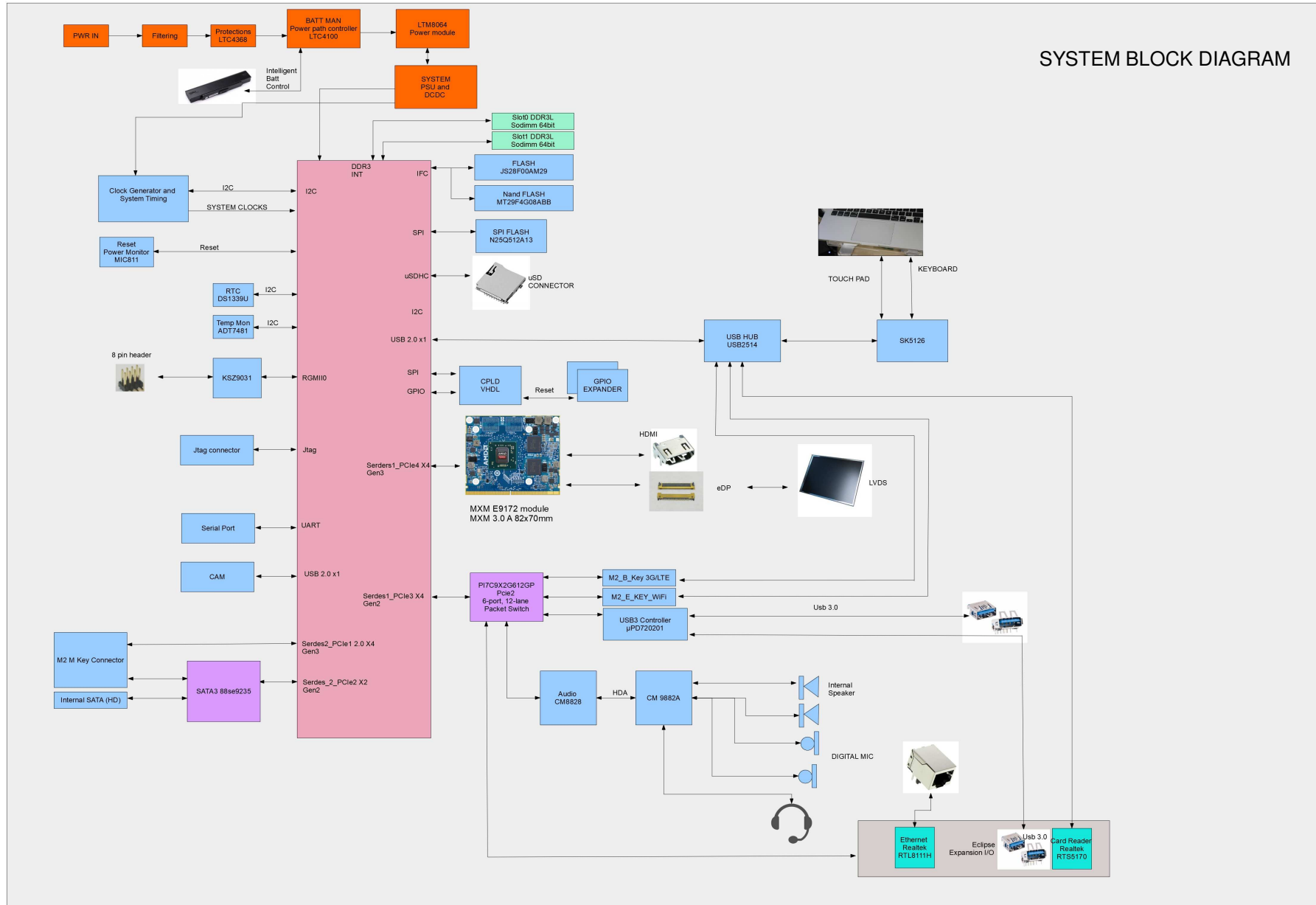
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4	T2080 SECOND BANK DDR3L INTERFACE
5	T2080 IFC INTERFACE
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Version Control		
Version	Date	Modifications
V0.1	2018/12	First release of Schematics
V0.2	2019/09	Second release of Schematics
V0.3	2020/04	Third release of Schematics
V0.4	2020/05	Fourth release of Schematics

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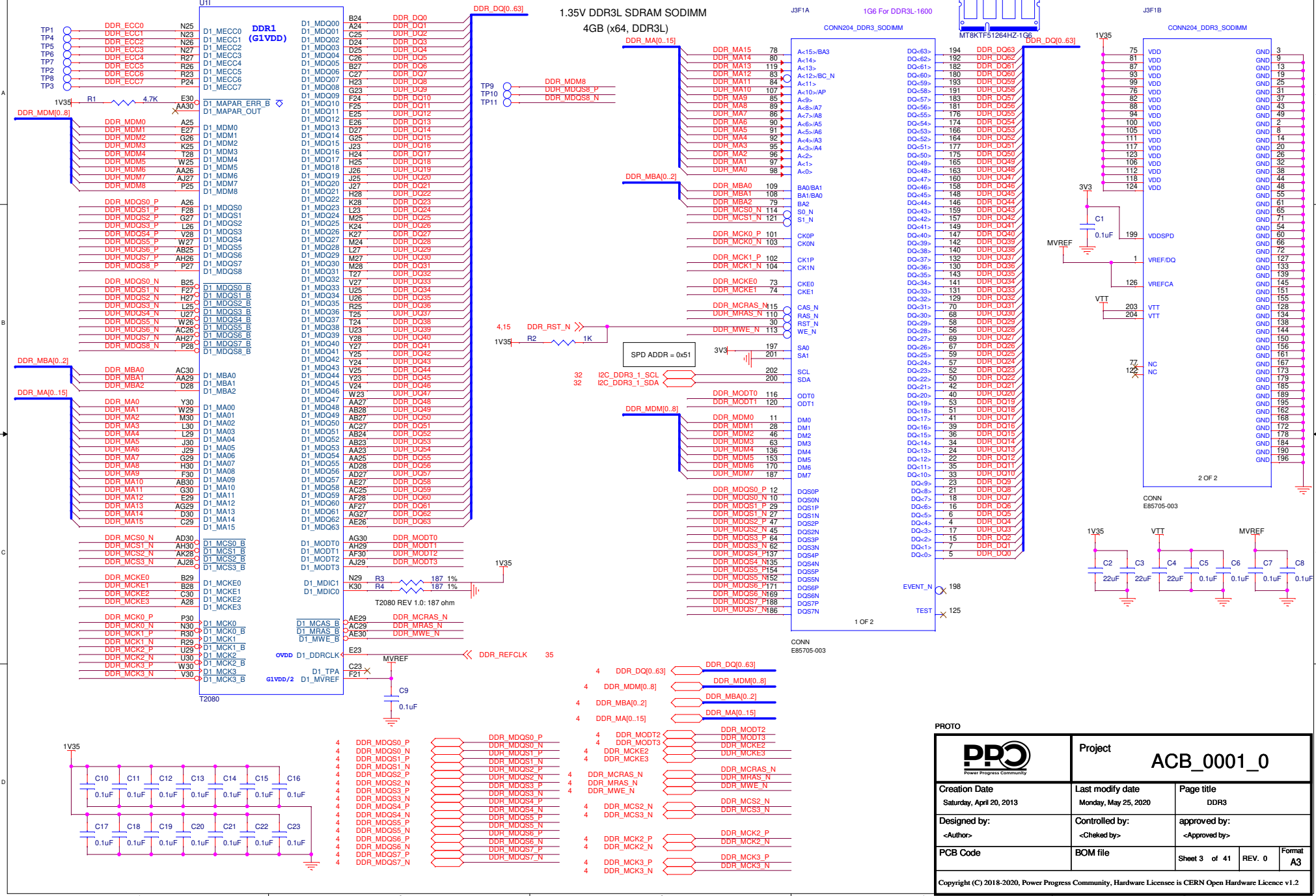
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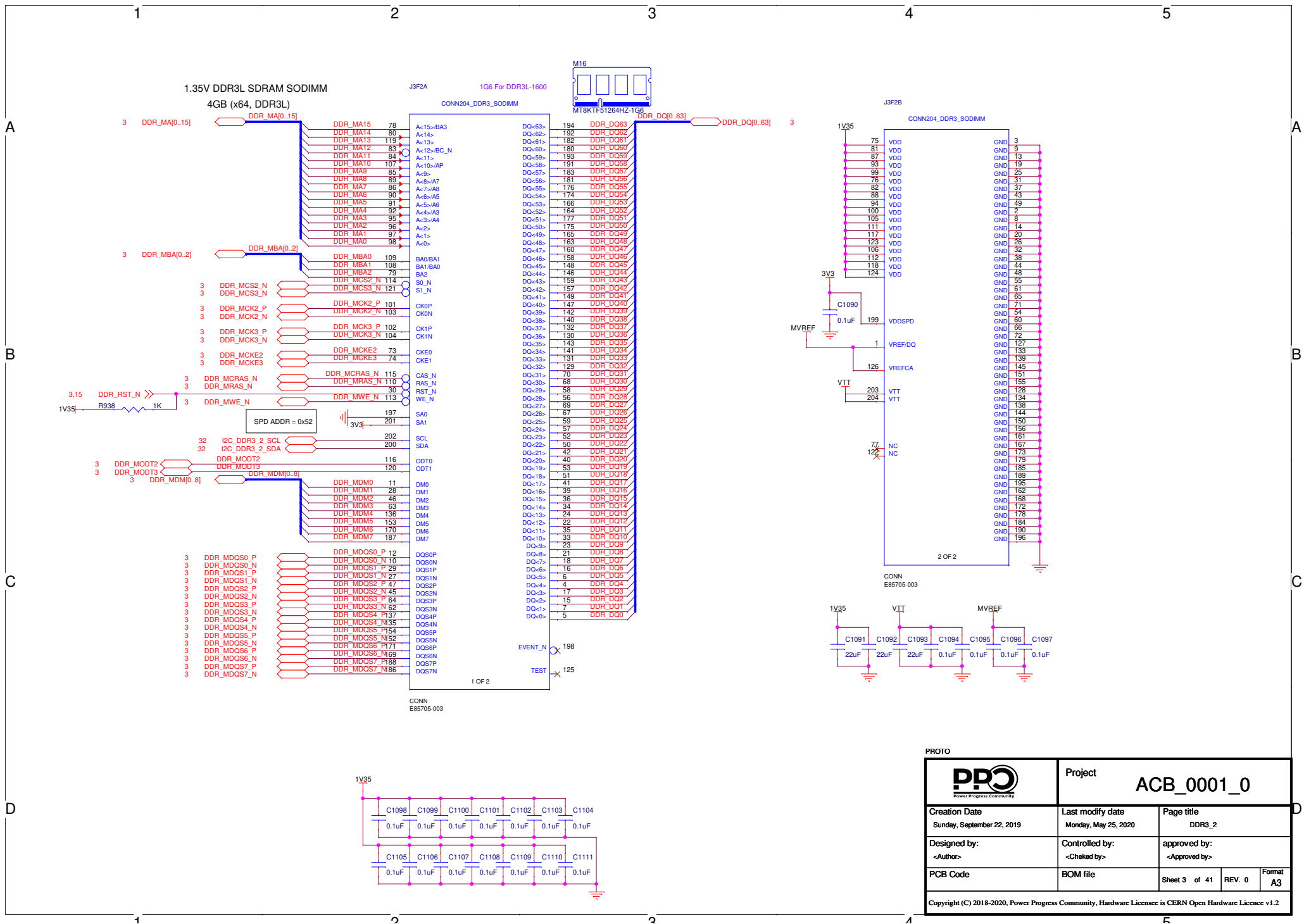
SYSTEM BLOCK DIAGRAM



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Author:	Check:	Approved:	Approved Date:
Proj Code:	Proj No:	Sheet:	Total:
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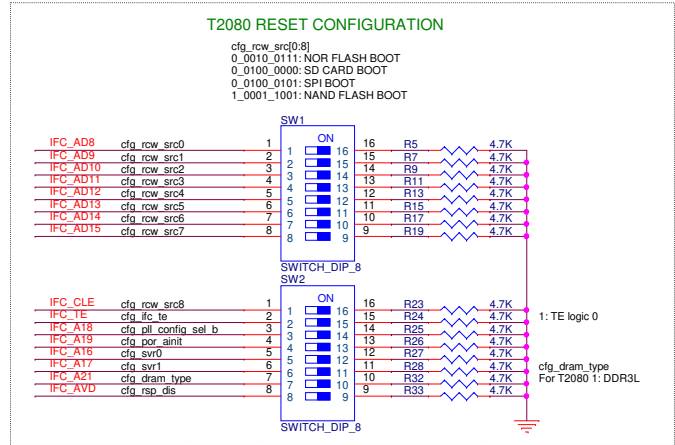
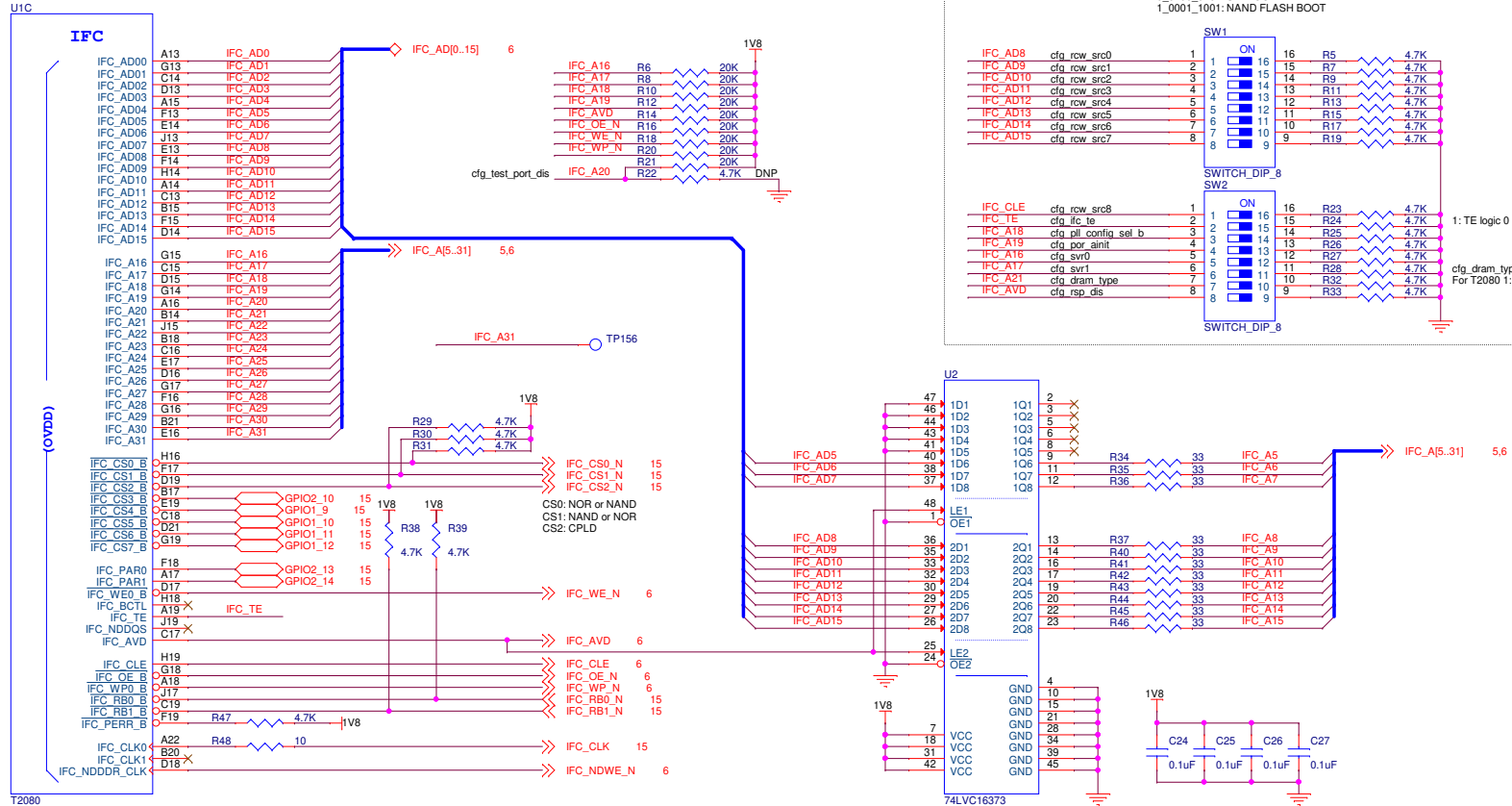
T2080 DDR3L MEMORY INTERFACE





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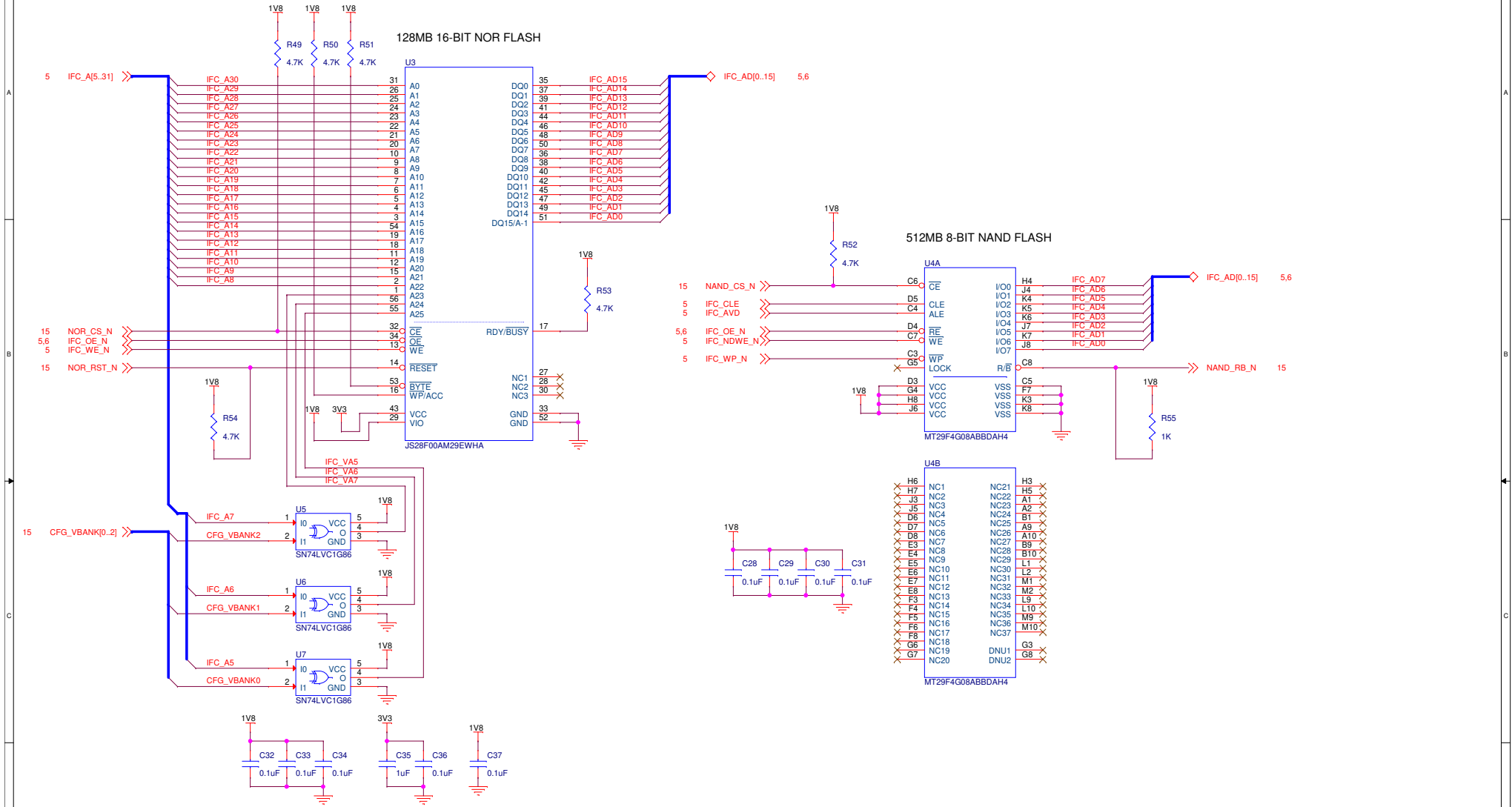
T2080 IFC INTERFACE



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PCB Code		BOM file	Sheet 4 of 41	REV. 0
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T2080 NOR and NAND FLASH INTERFACE

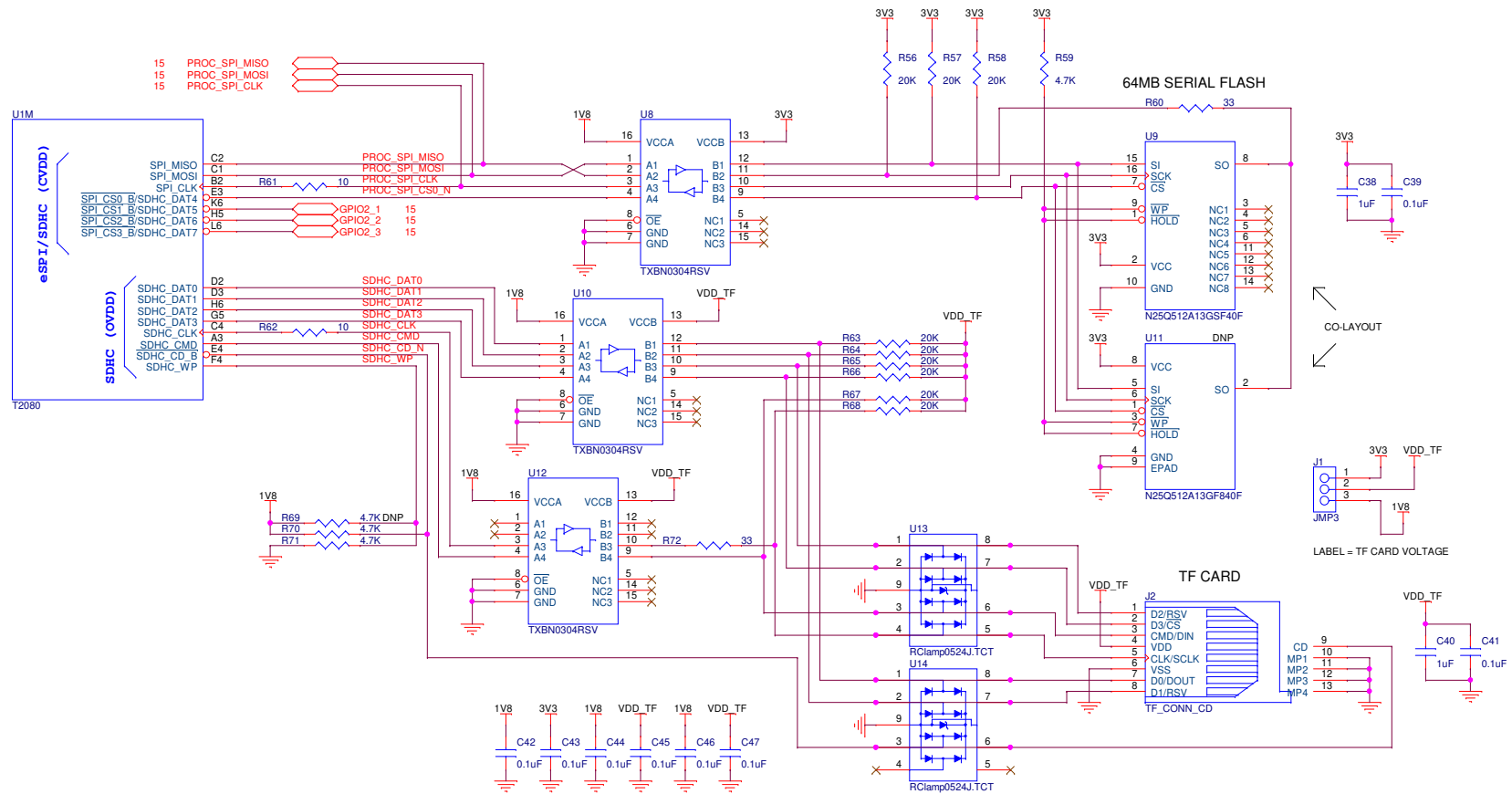


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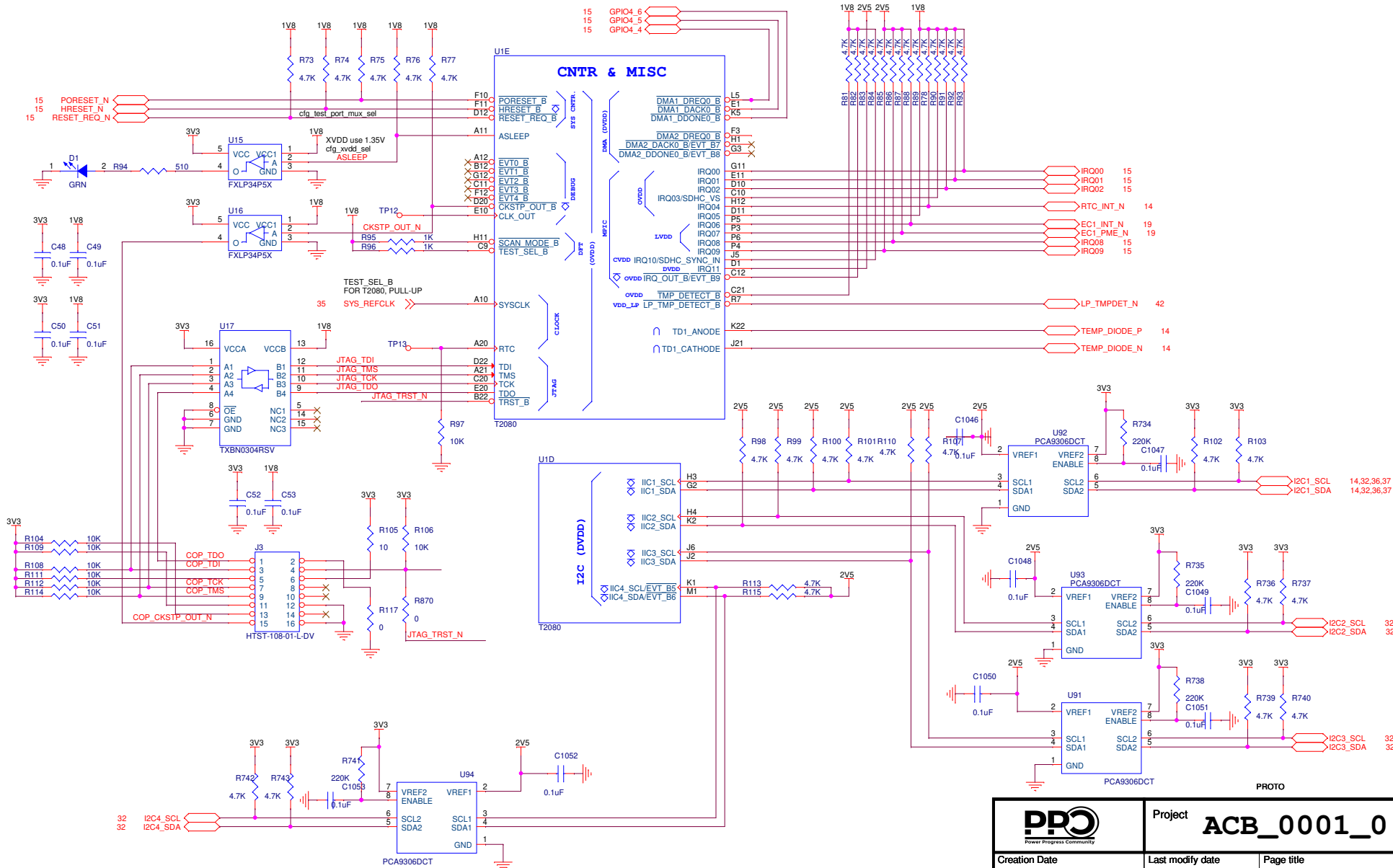
T2080 SPI FLASH and SDHC INTERFACE



PROTO

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T2080 SYSTEM LOGIC INTERFACE



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T2080 ETHERNET and SERDES INTERFACE

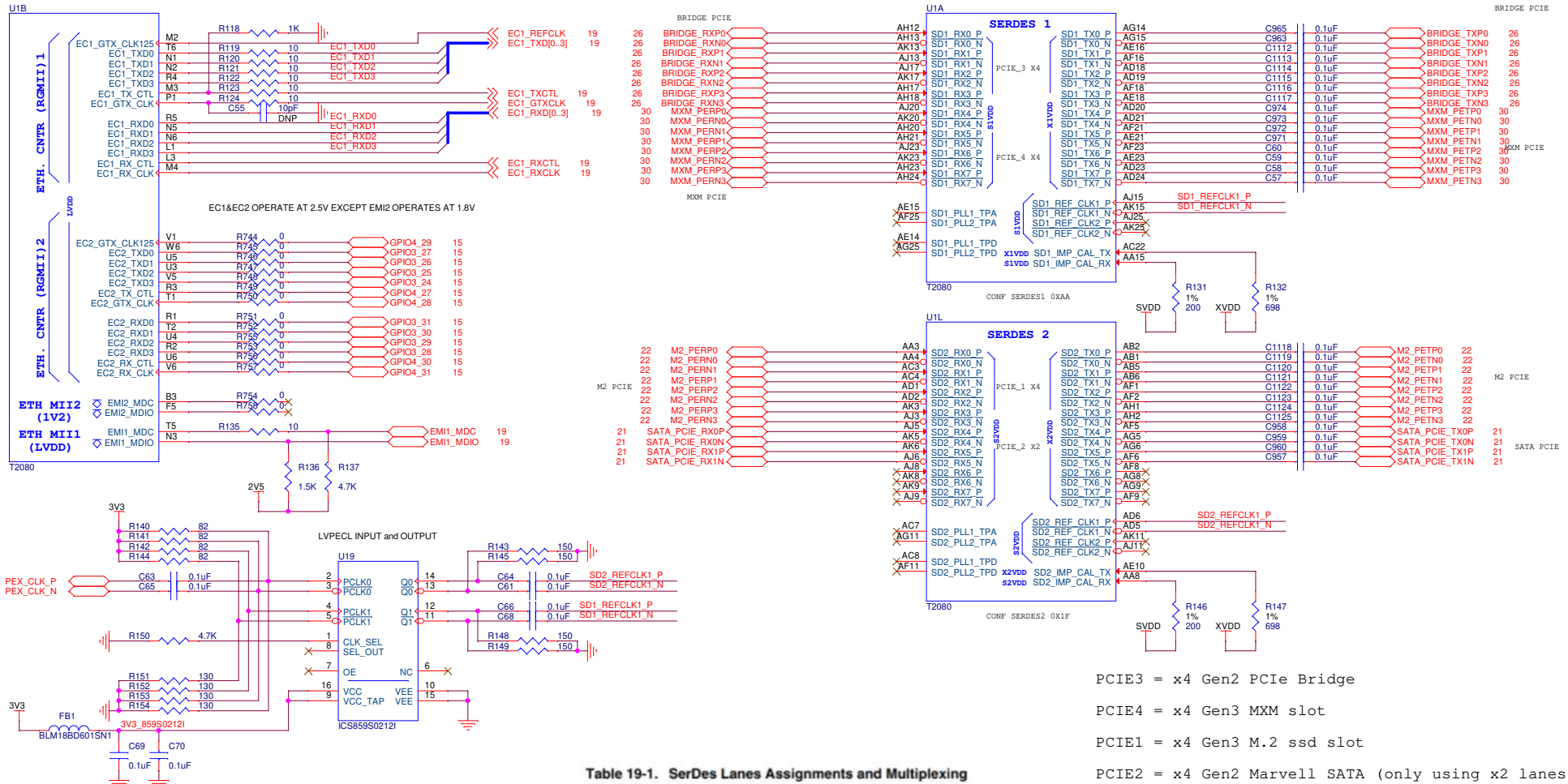



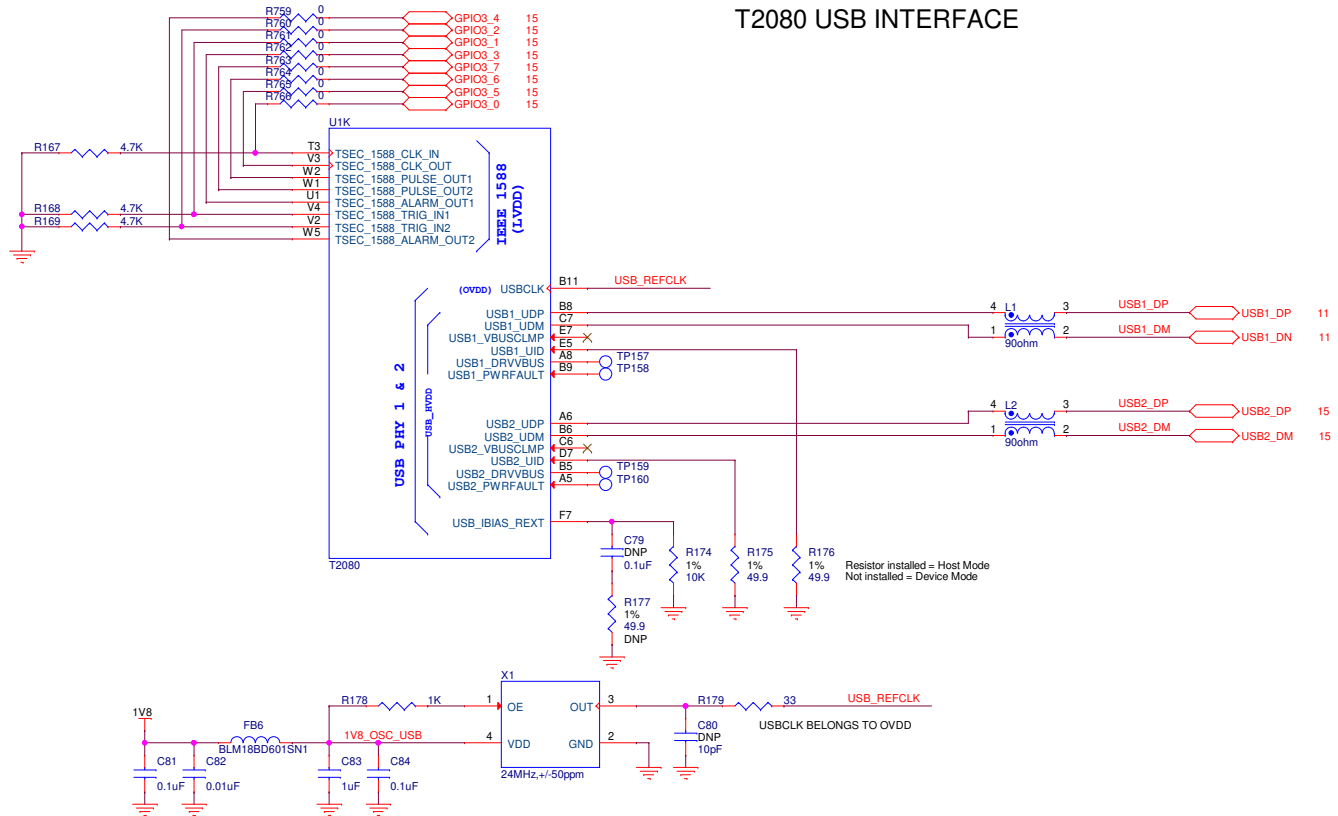
Table 19-1. SerDes Lanes Assignments and Multiplexing

SRDS_PARTCL_S1	SERDES1								SERDES2								Per Lane PLL Map
	A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H	
AA	PCIE3				PCIE4				1111	1F1	PCIE1				PCIE2	1111	2222


PROTO

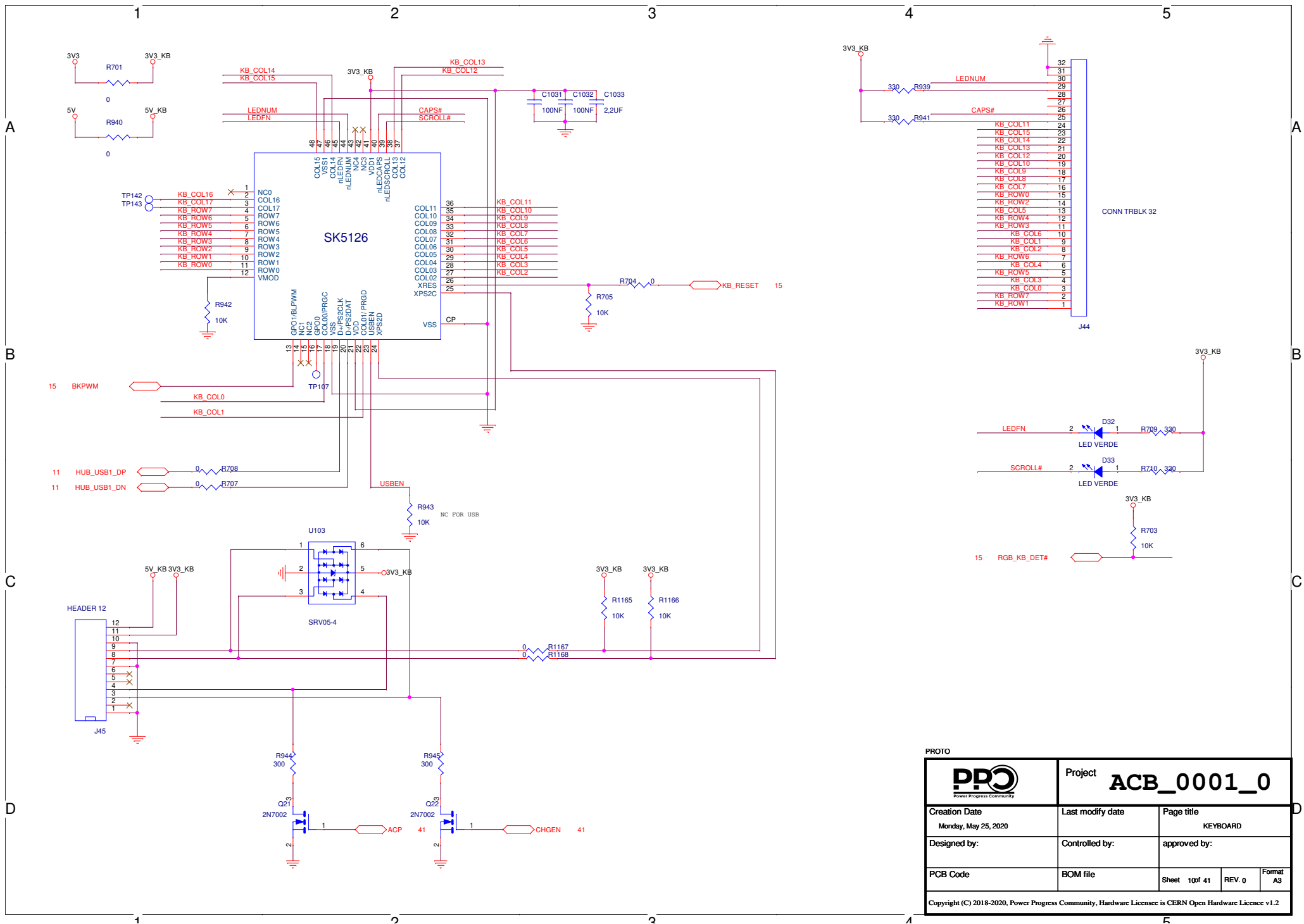
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T2080 USB INTERFACE



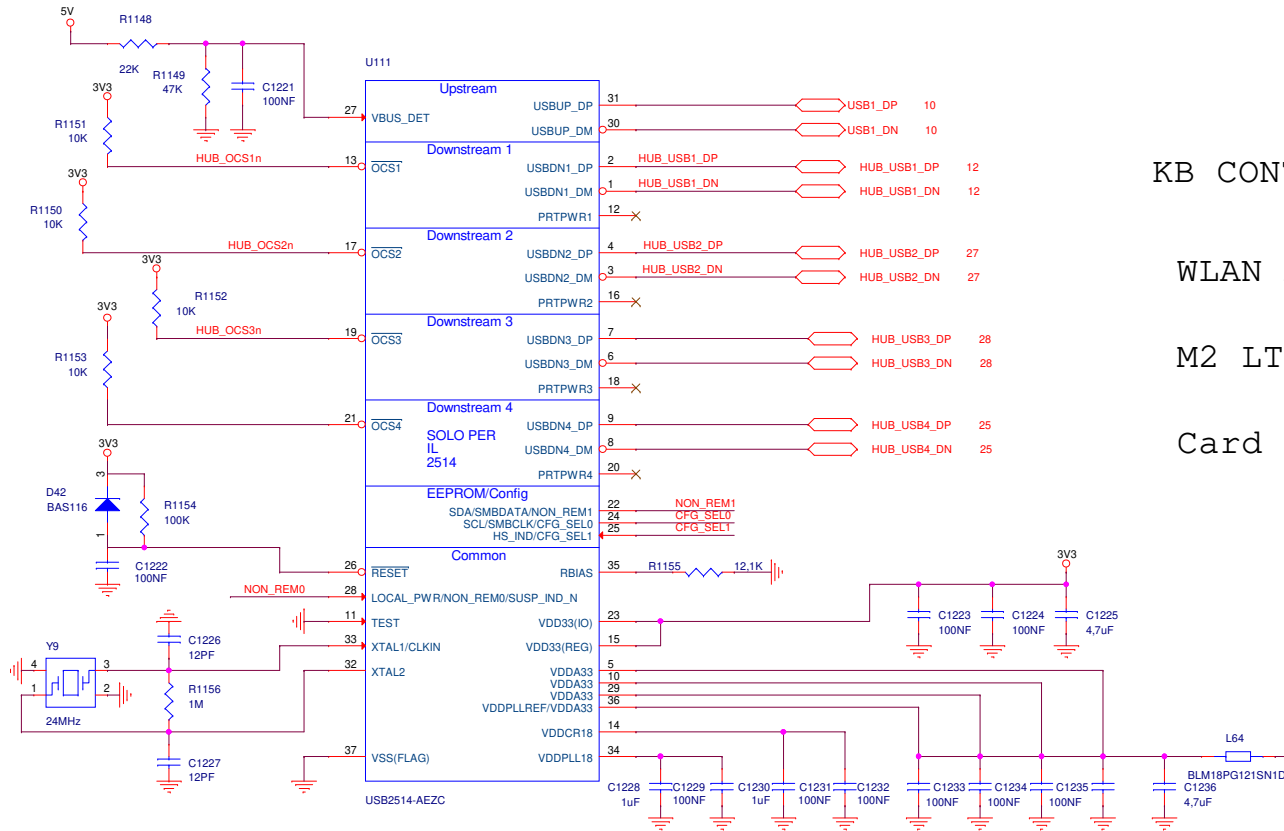
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HUB USB

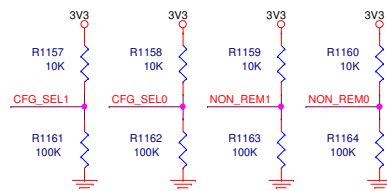


KB CONTROLLER


WLAN M2

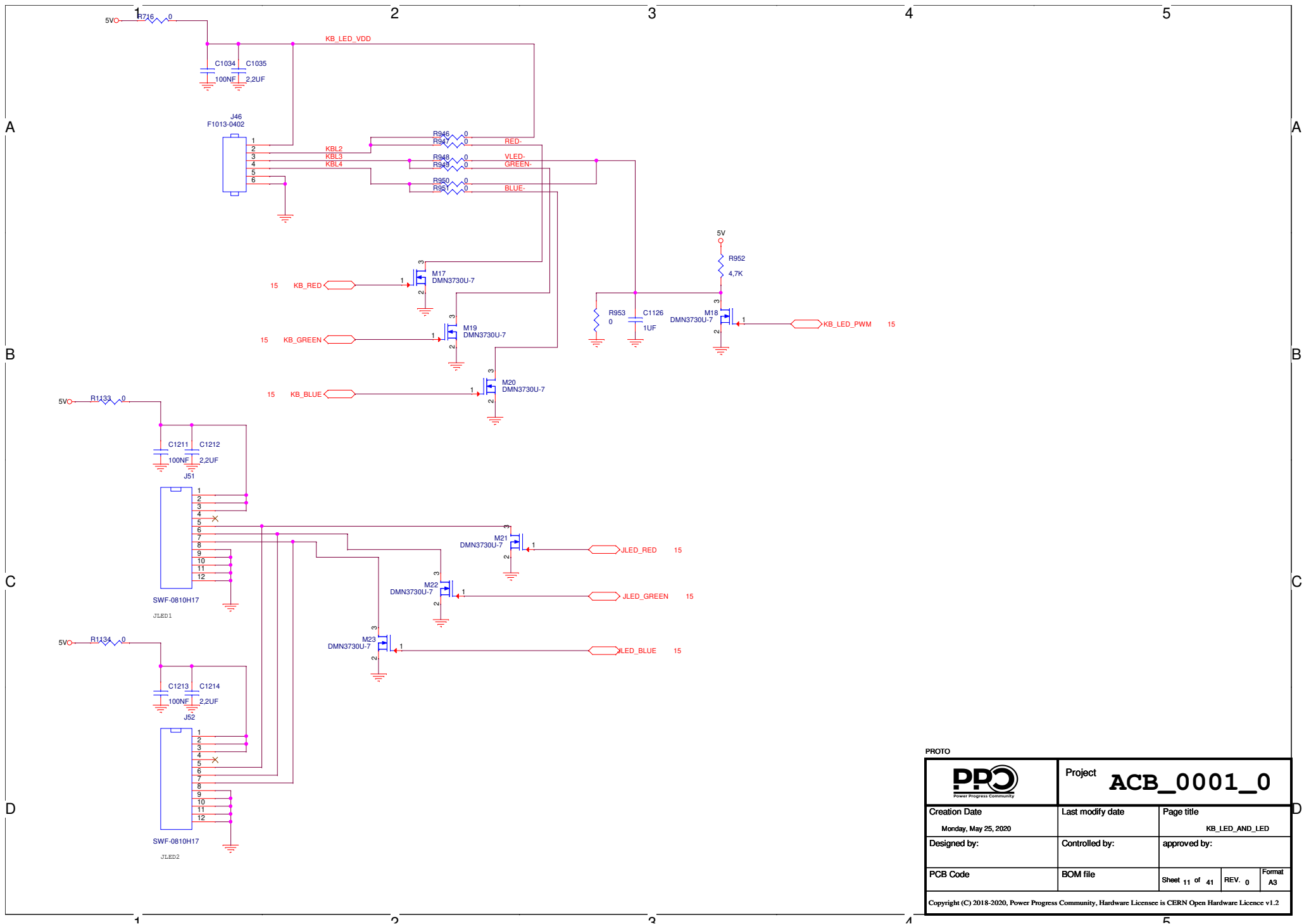
M2 LTE

Card Reader




PROTO

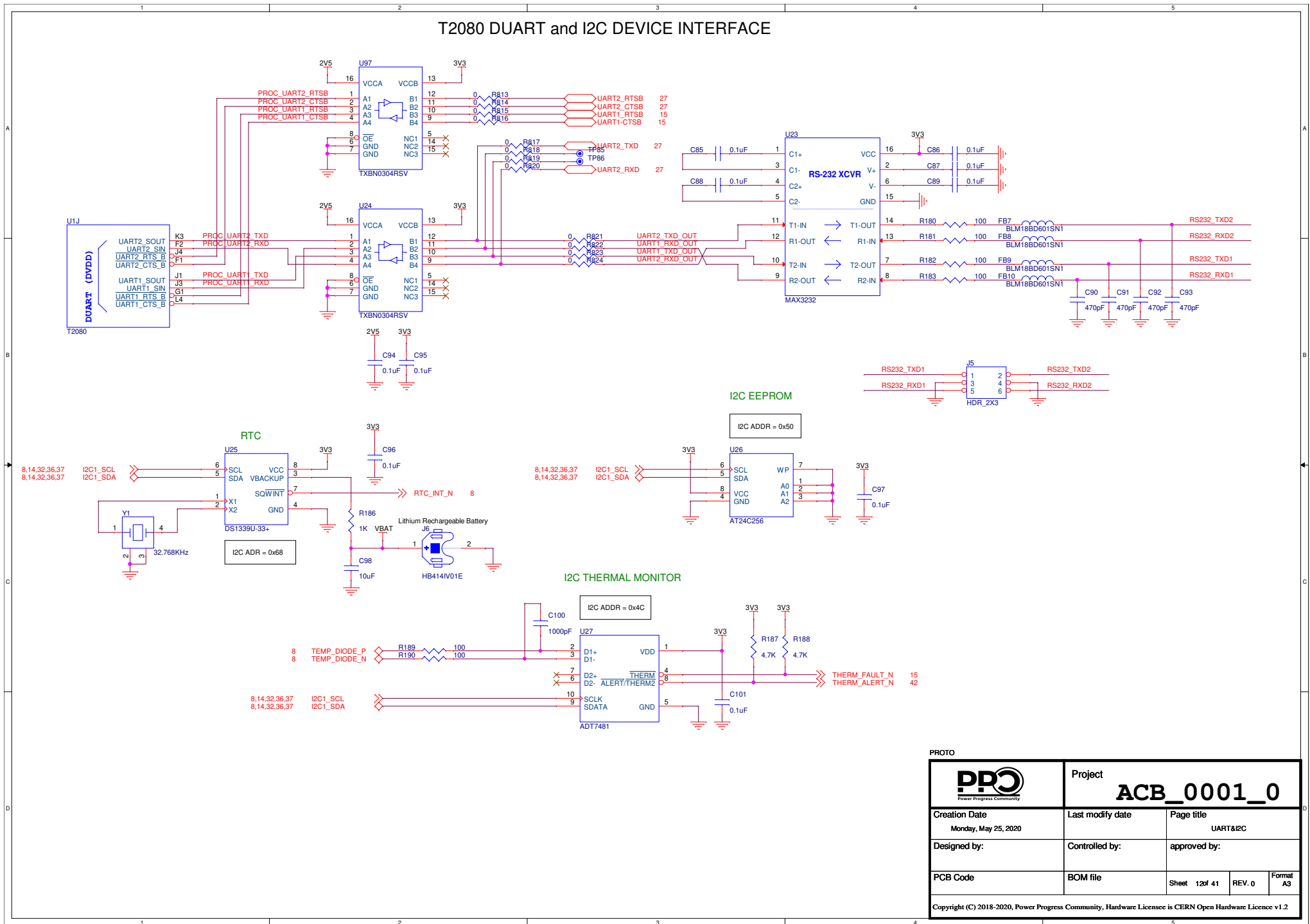
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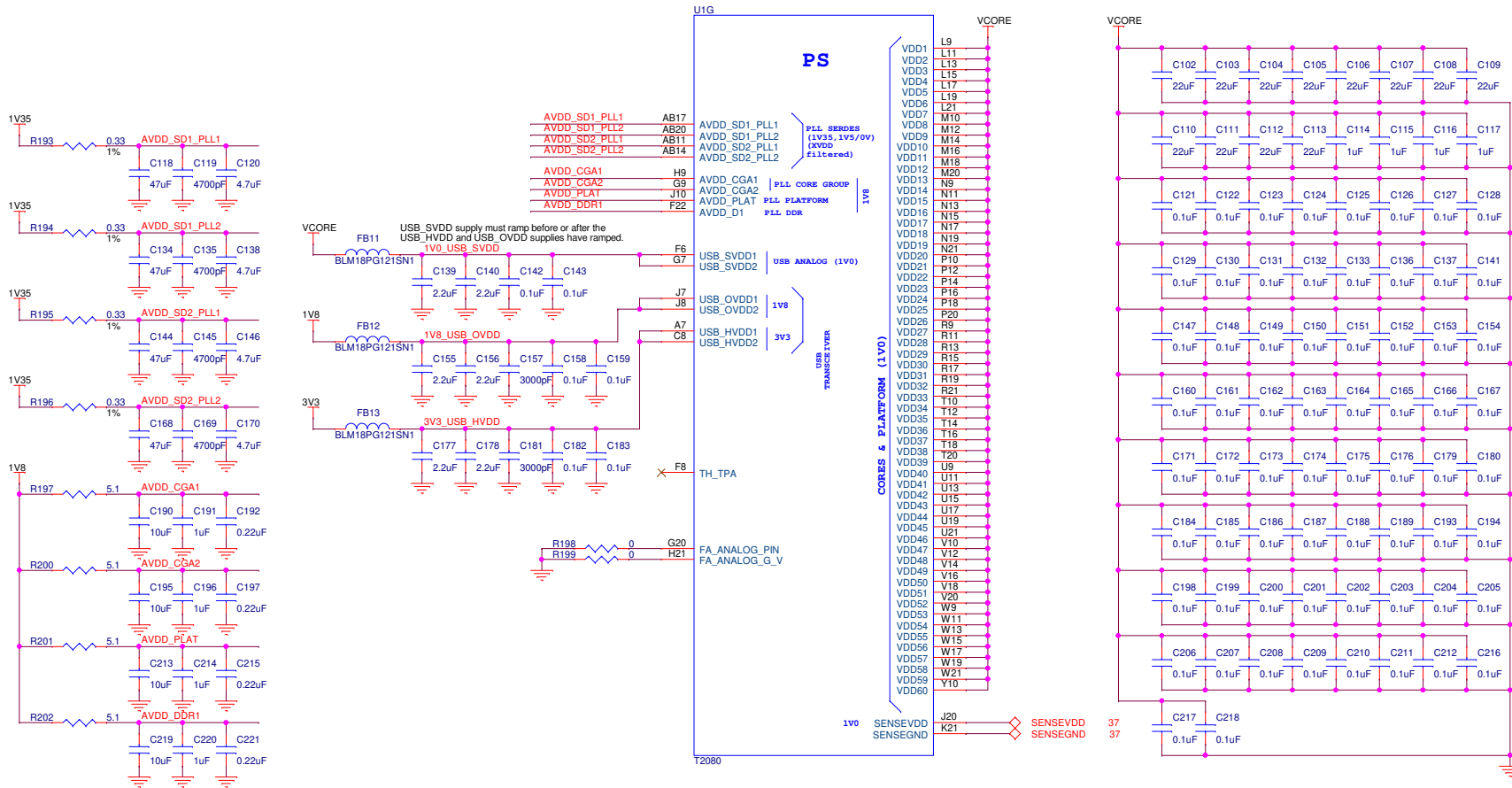
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PCB Code	BOM file	Sheet 11 of 41	REV. 0	Format A3
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T2080 DUART and I2C DEVICE INTERFACE



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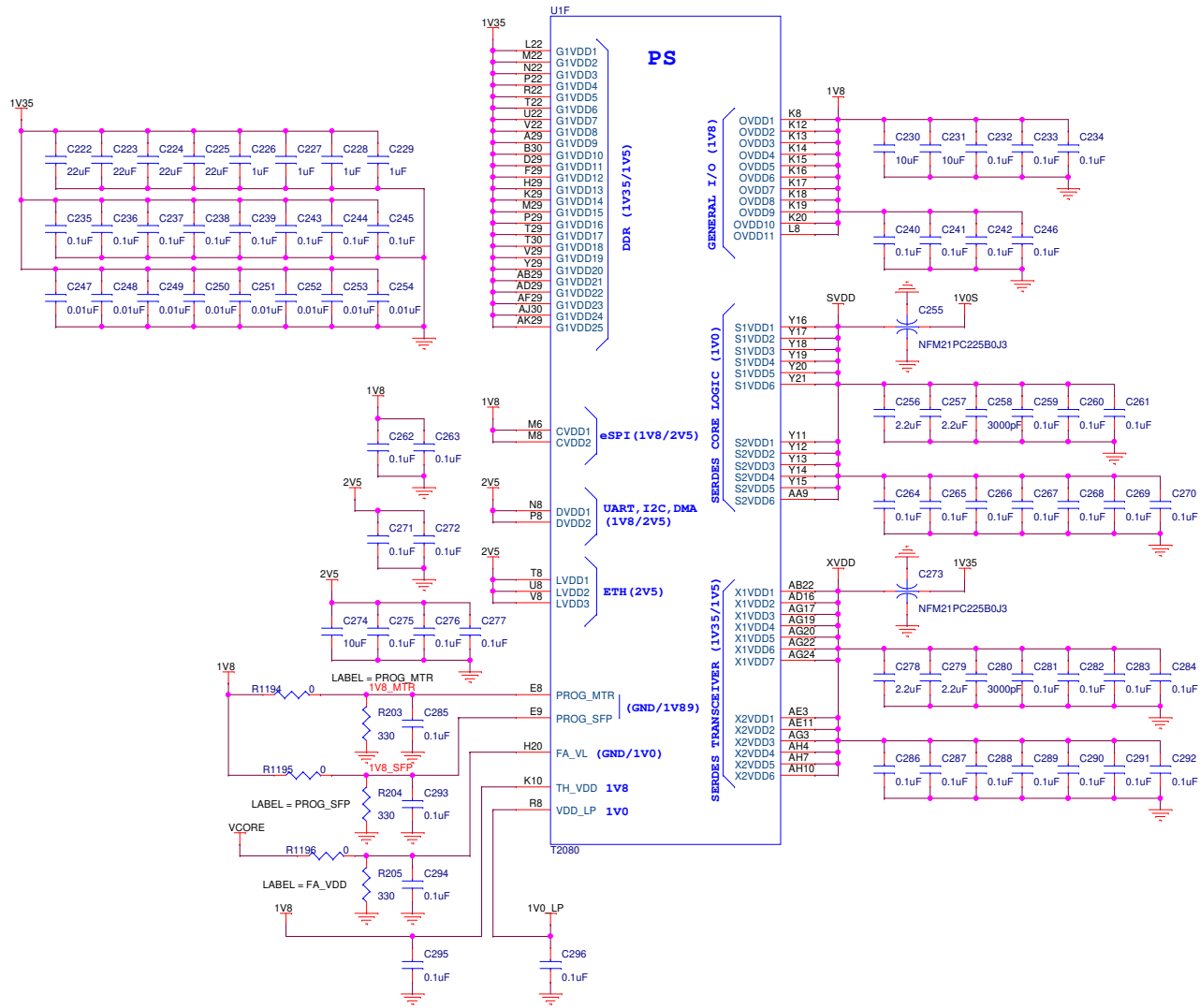
T2080 POWER SUPPLY




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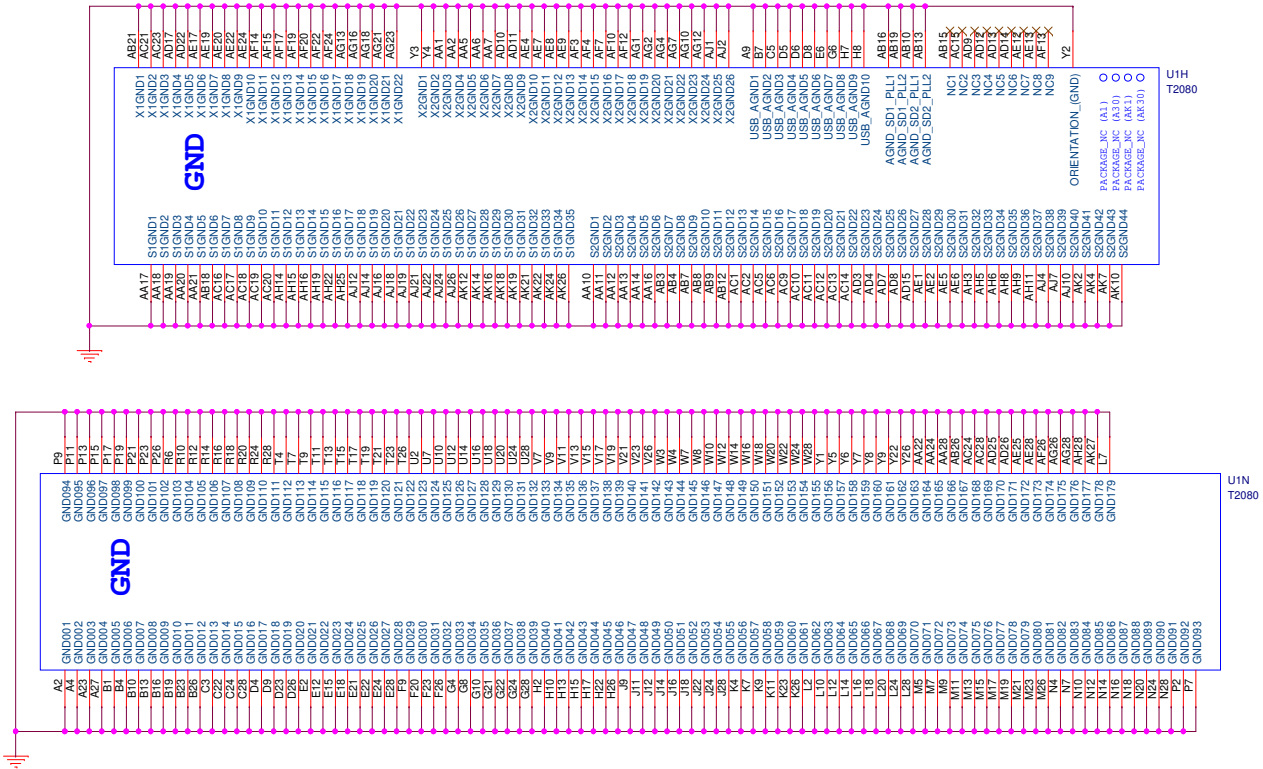
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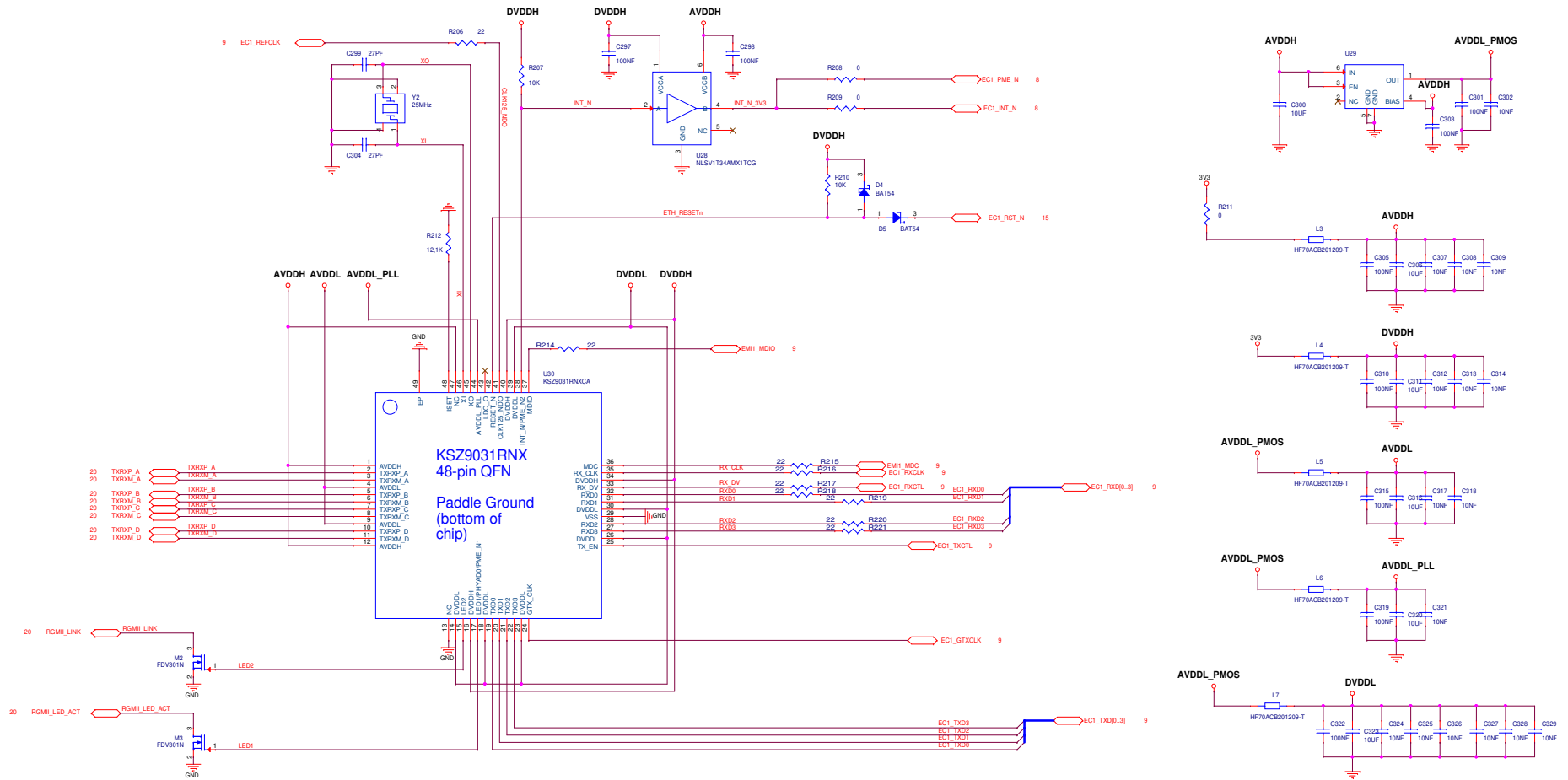
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T2080 GROUND

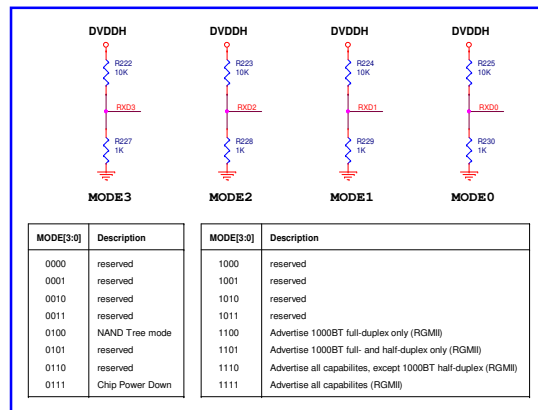


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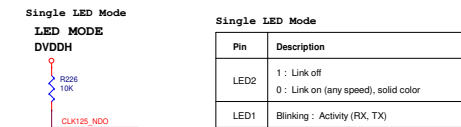
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Creation Date Monday, May 25, 2020	Last modify date	Page title PROC GND		
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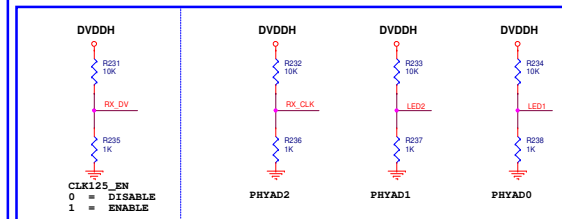
Strapping Pins



Strapping Pin

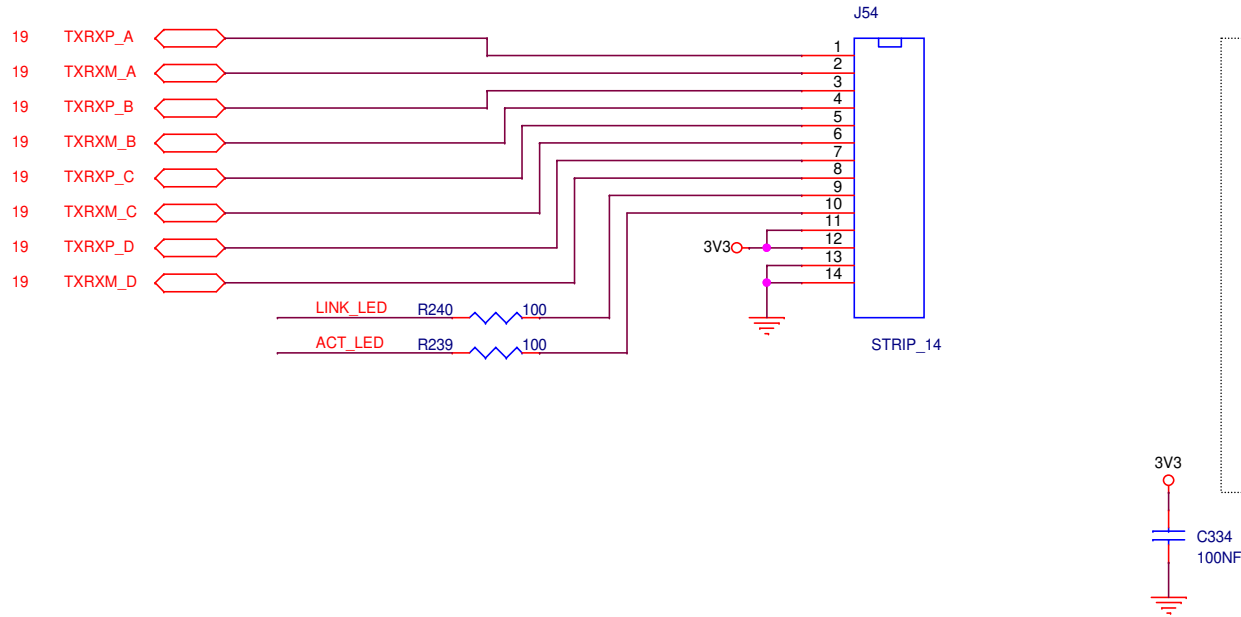


Strapping Pins

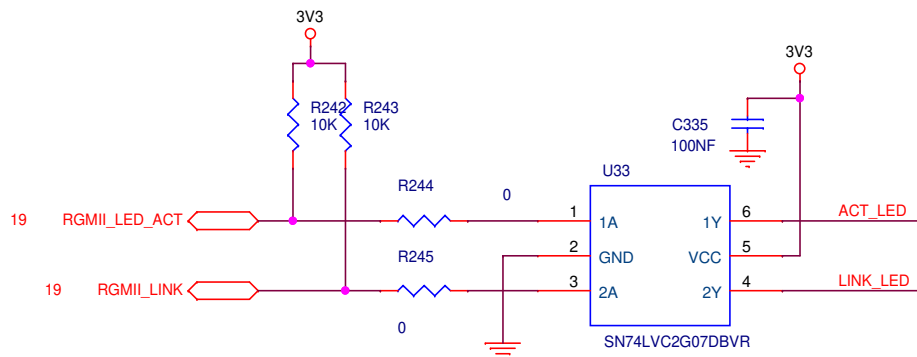


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PCB Code	BOM file	Sheet 17 of 41 REV. 0
		Format A2


Gigabit Ethernet



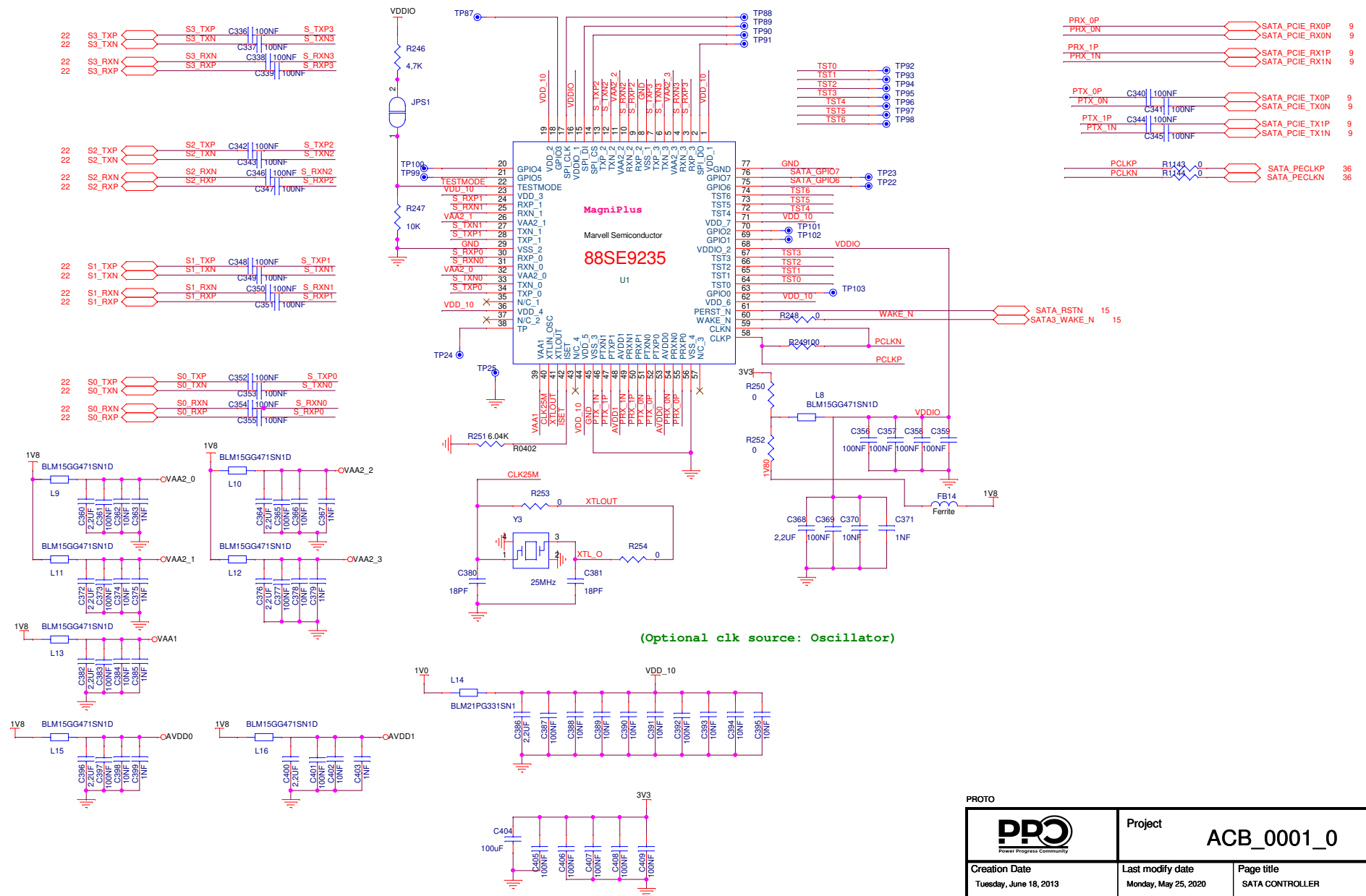
Led Ethernet Buffer



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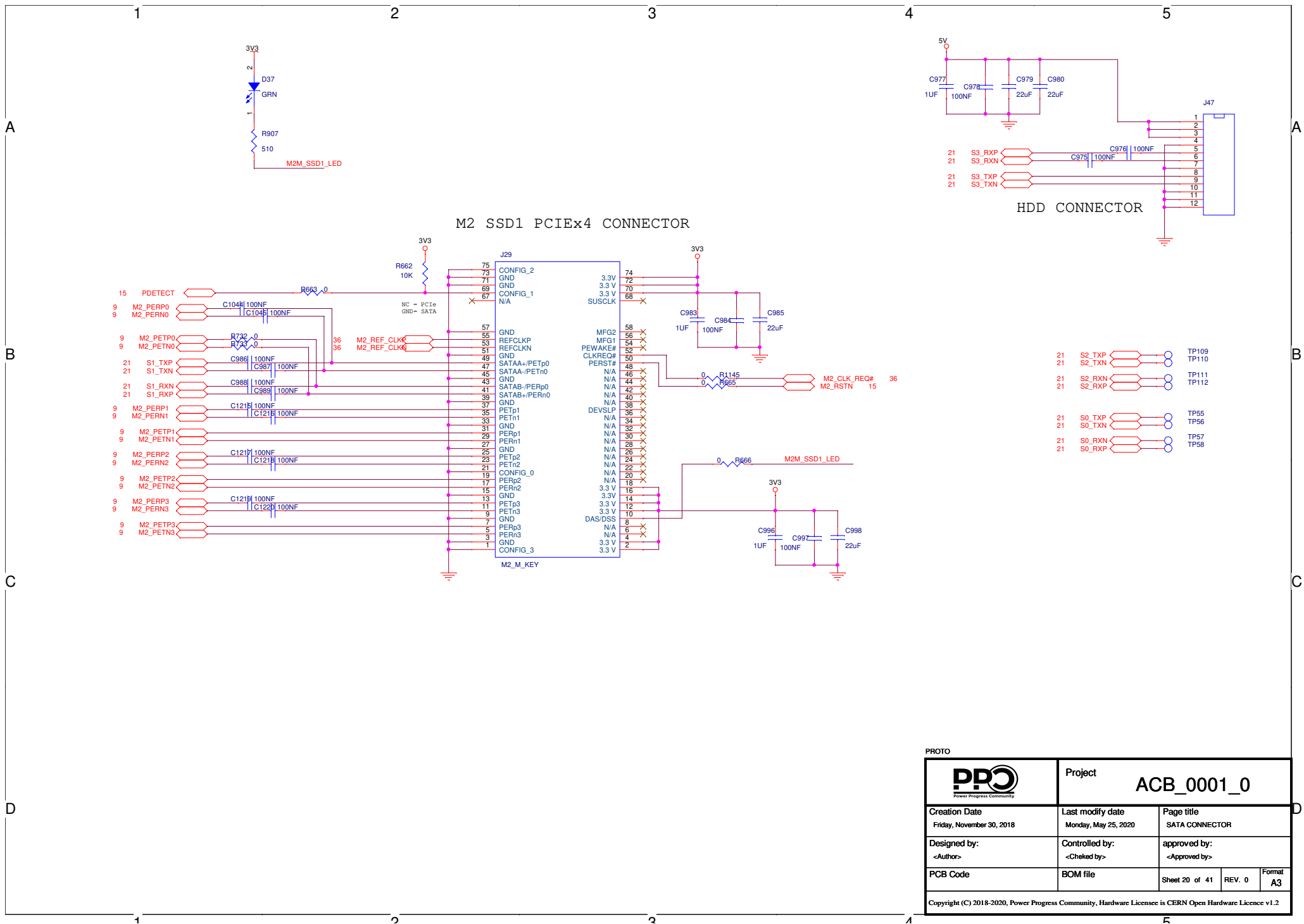
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		REV. 0
		Format A4
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MagniPlus -SATA Interface




(Optional clk source: Oscillator)

Creation Date		Last modify date	Page title
Tuesday, June 18, 2013		Monday, May 25, 2020	SATA CONTROLLER
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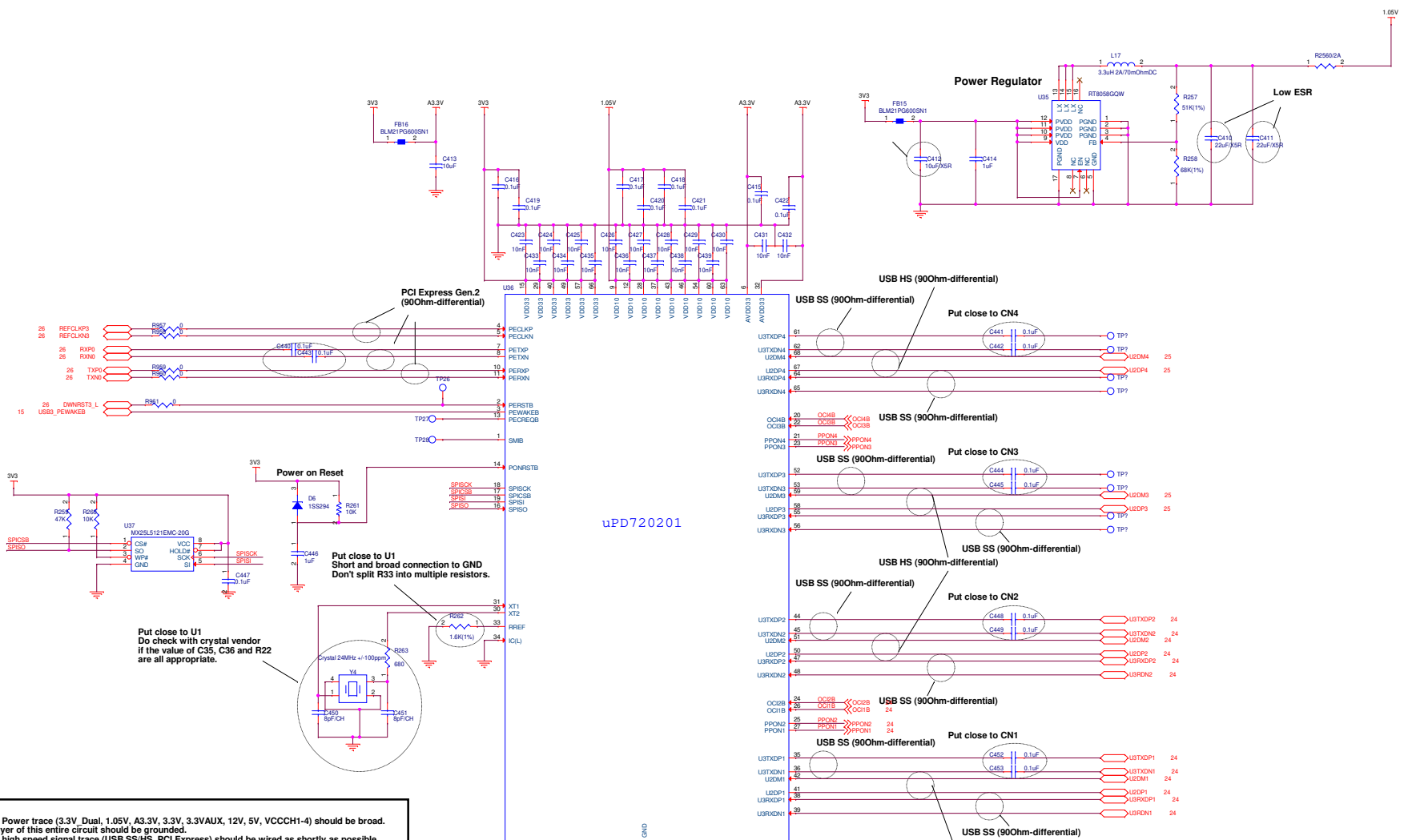



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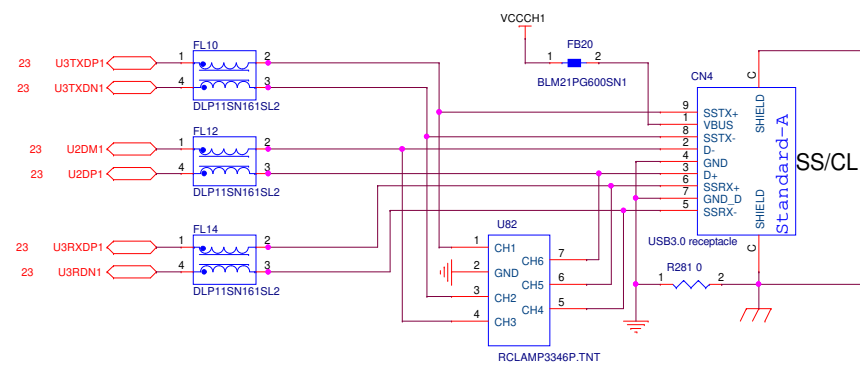
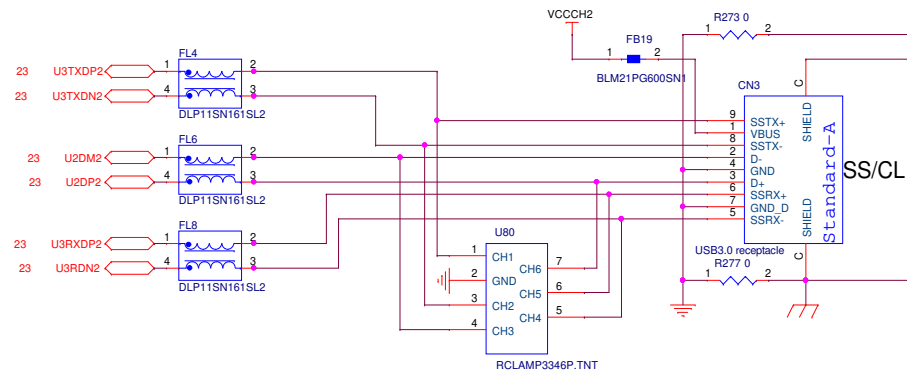
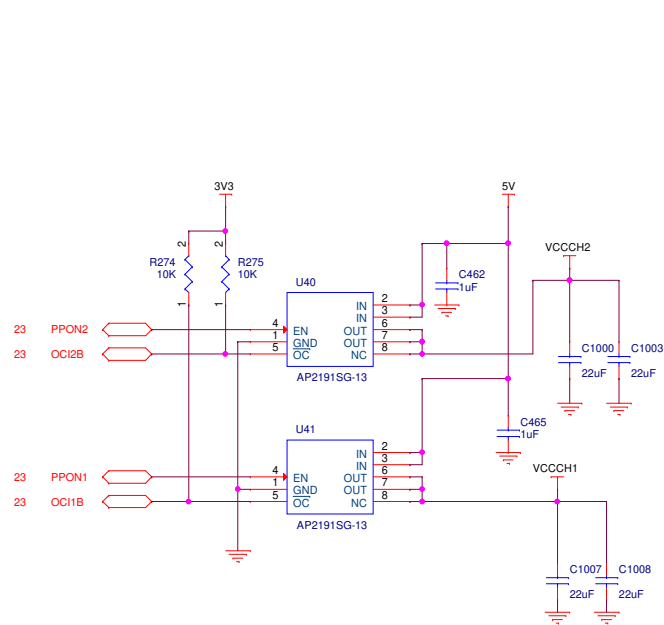
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PCB Code	BOM file	Sheet 20 of 41	REV. 0
Format A3			
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Note:


- Every Power trace (3.3V, Dual, 1.05V, A3.3V, 3.3V, 3.3VAUX, 12V, 5V, VCCCH1-4) should be broad.
- 2nd layer of this entire circuit should be grounded.
- Every high speed signal trace (USB SS/HS, PCI Express) should be wired as shortly as possible.
- Capacitors C100-116 should be located next to U1, and connected to GND tightly – by tracing shortly and broadly.
- For signal traces, routing priority is as follows;
 - USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
- At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
- Follow the basic of transmission trace pair when routing any signal trace.
 - > Remove any impairment or discontinuity.
 - > Keep same length by each other.
 - > Keep same width and spacing.
- The differential impedance of nominal value is as follows.
 - > USB 3.0 / 2.0 --- 90ohm
 - > PCI express Gen 1,(2,5GT/s) --- 100ohm PCI express Gen 2,(5GT/s) --- 85ohm
 PCB trace impedance would be a non-continues value by its design rules. The differential impedance adopt the nearest value that can be manufactured at PCB. For more information please refer to 'USB3.0 Board Design Guide' in design kit.



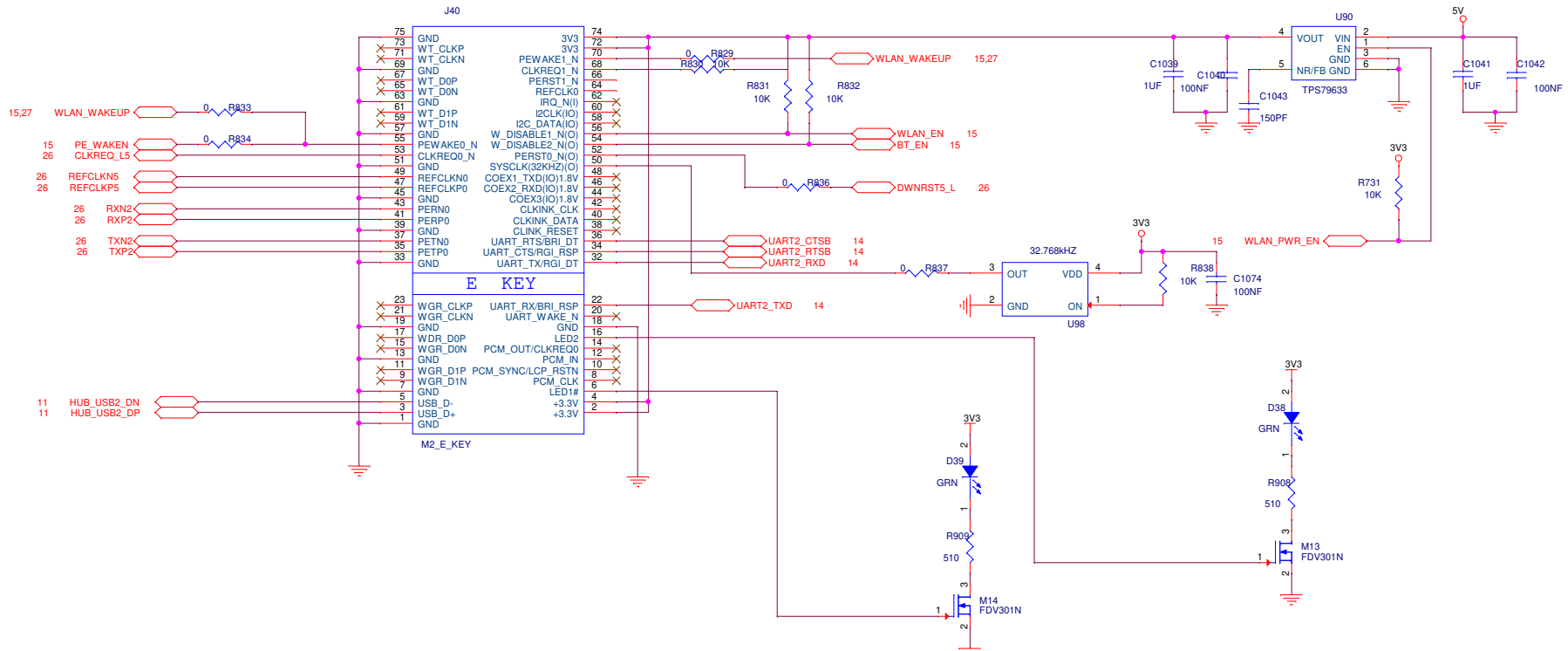
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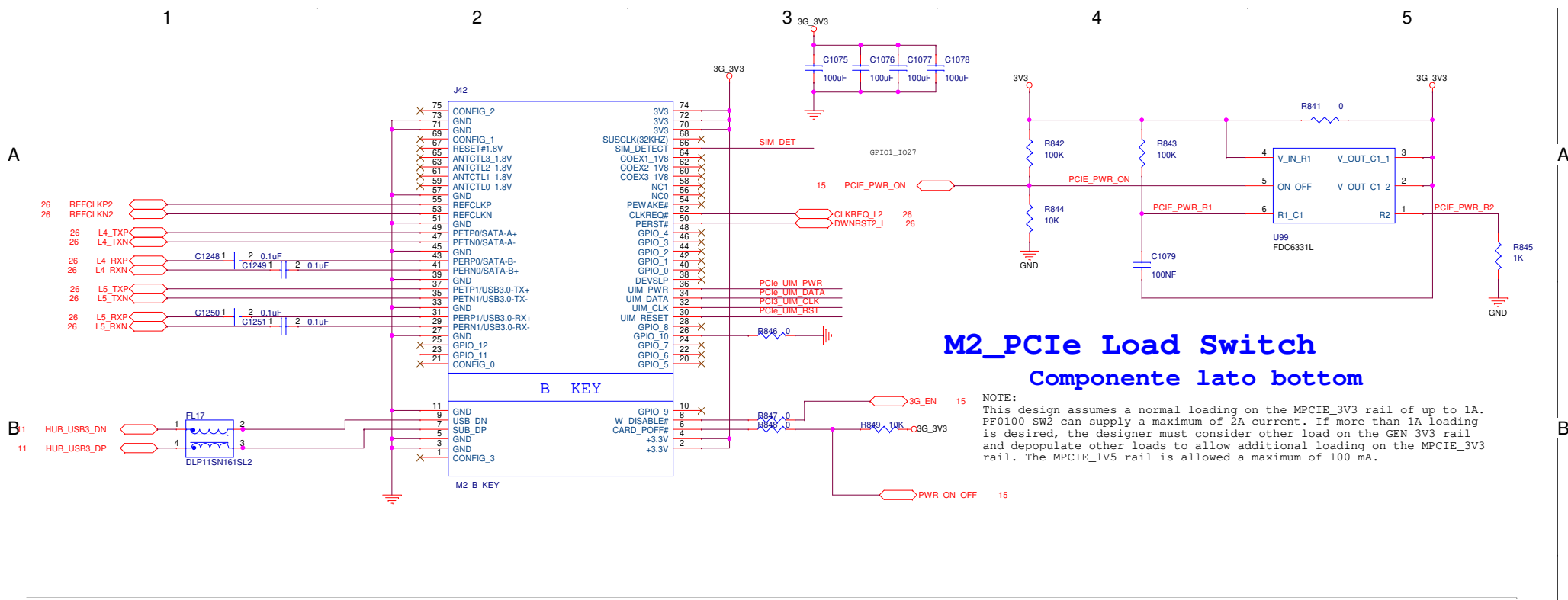
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M2 WLAN+BT PCIe x1 CONNECTOR

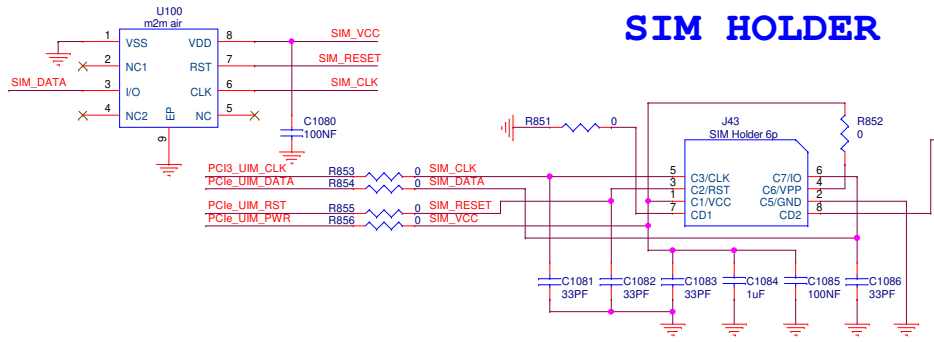
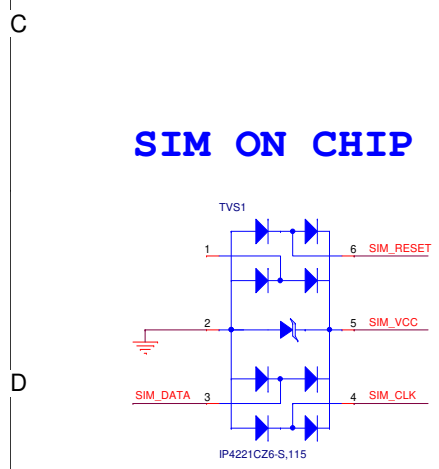


PPC Power Progress Community		Project ACB_0001_0	
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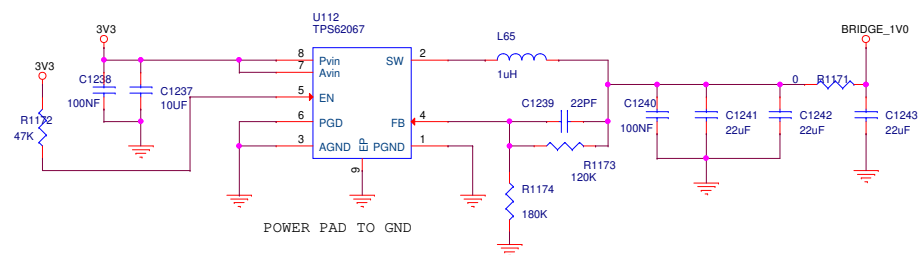
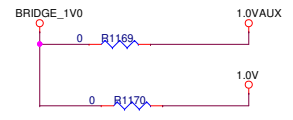
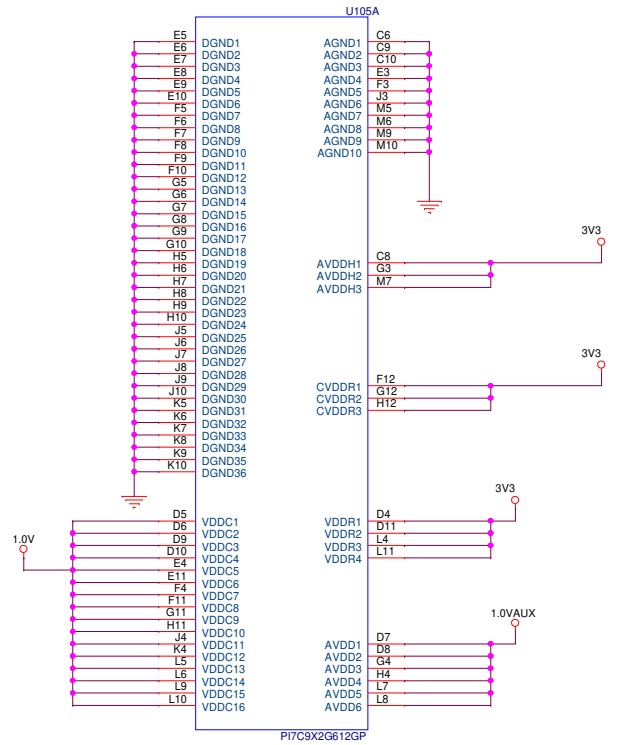


M2_PCIe Load Switch Componente lato bottom

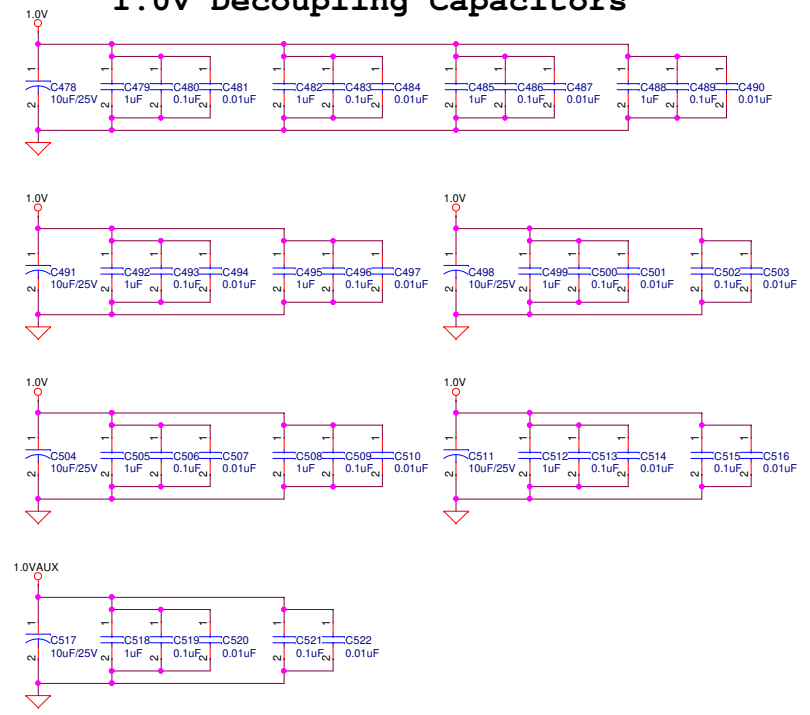
NOTE:
 This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.



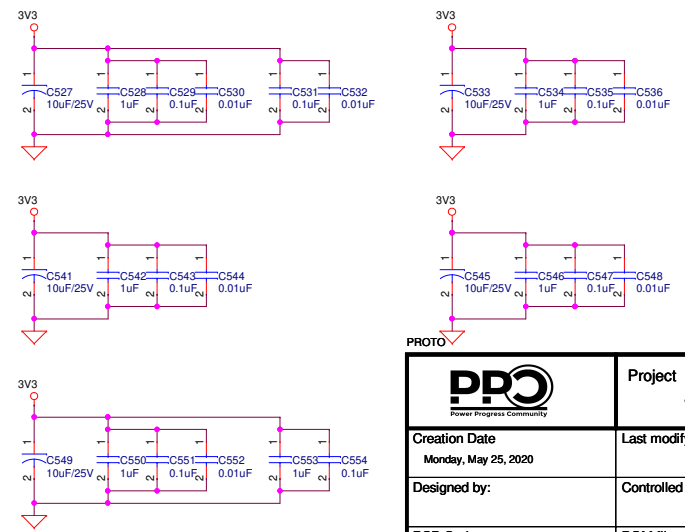
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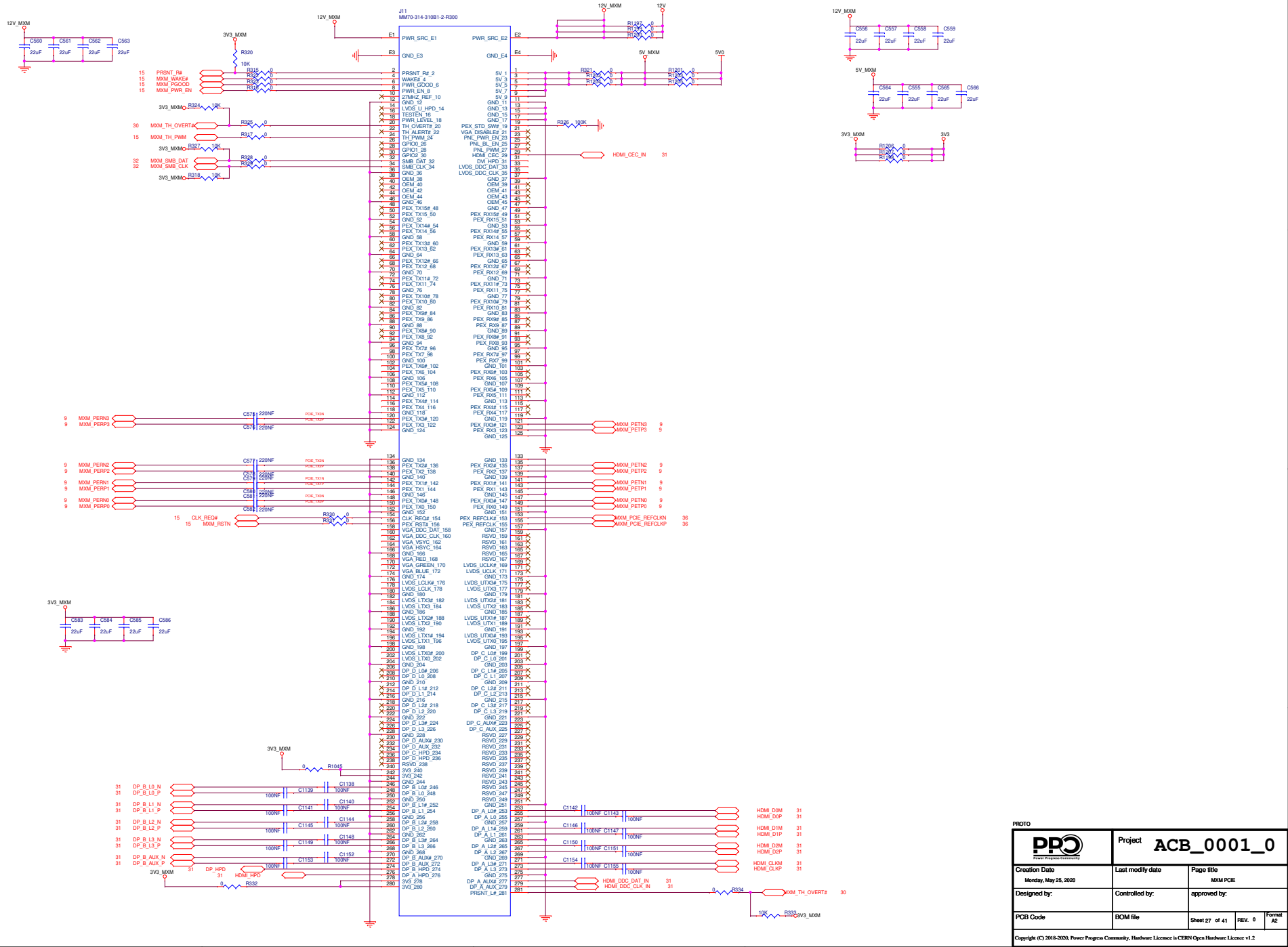
1.0V Decoupling Capacitors




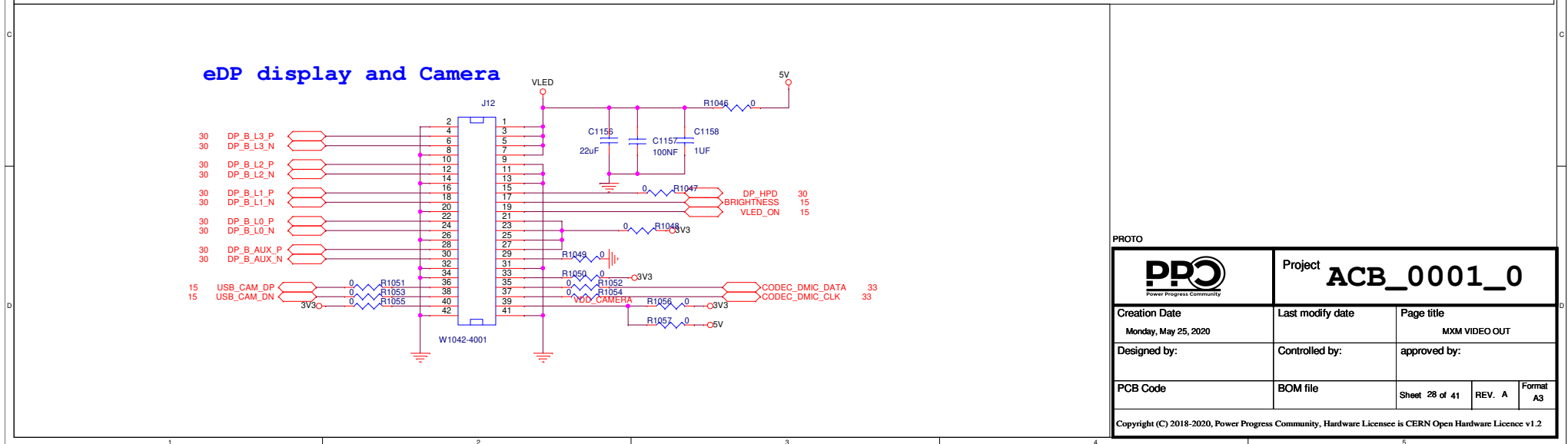
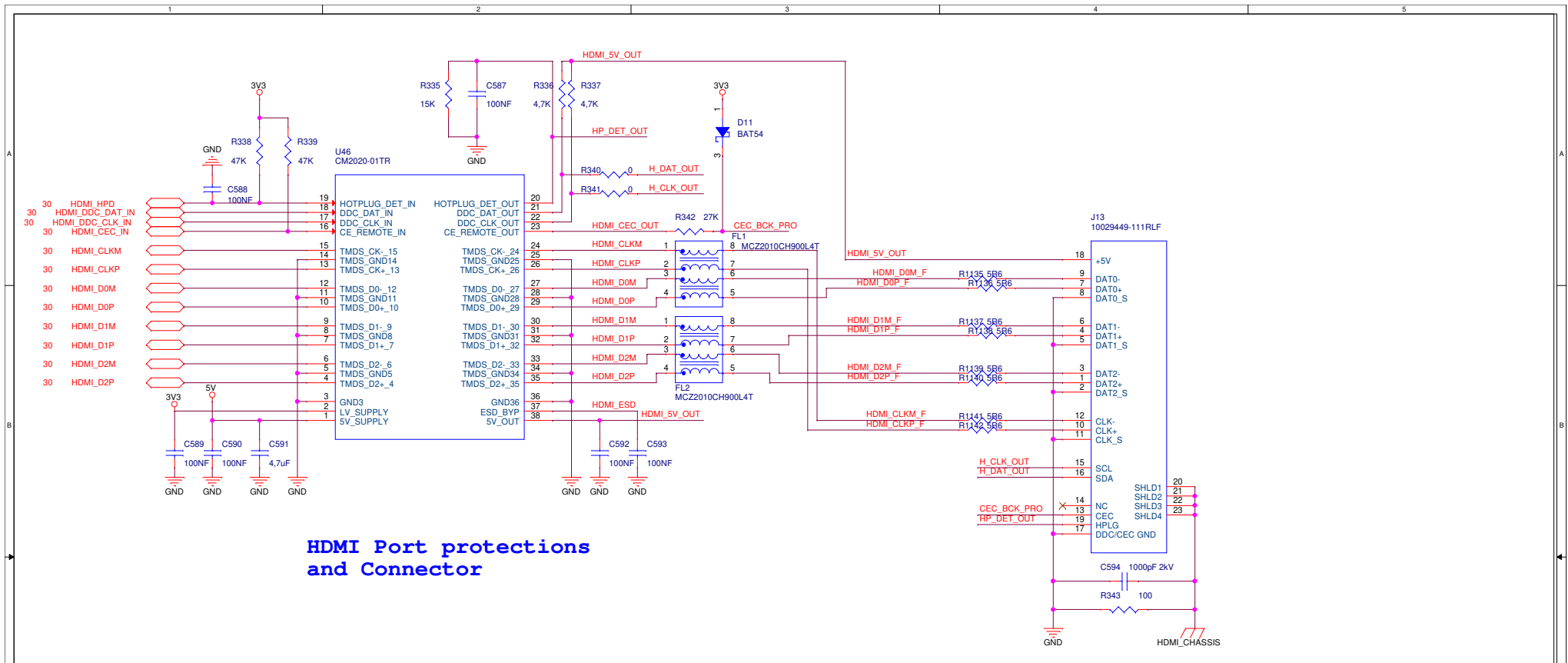
3.3V Decoupling Capacitors




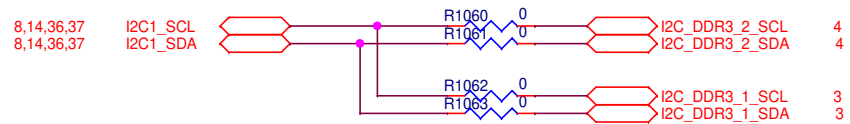
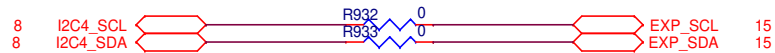
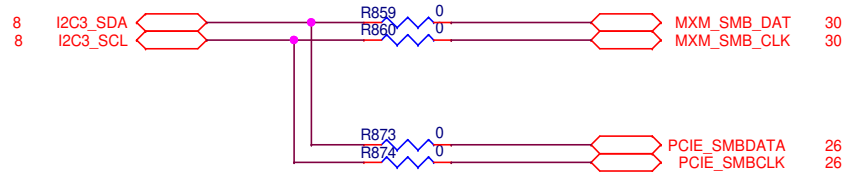
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PCB Code	BOM file	Sheet 27 of 41 REV. 0 Format A2
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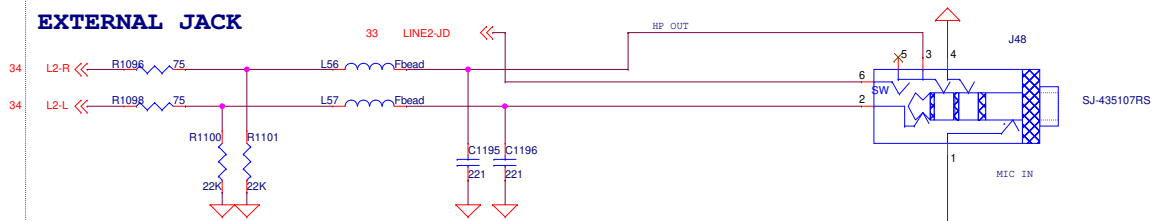
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		ACB_0001_0	
Creation Date	Last modify date	Page title	
Monday, May 25, 2020		MXM VIDEO OUT	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 28 of 41	REV. A Format A3
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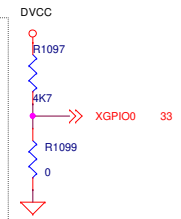
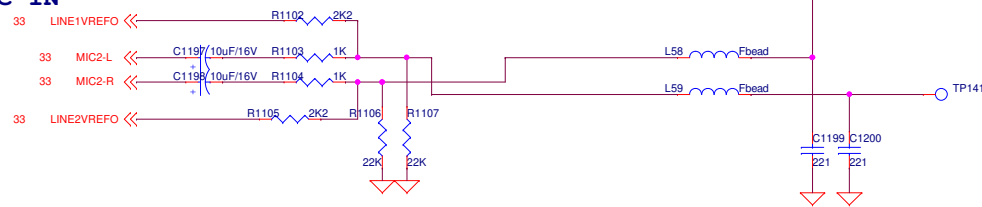
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Creation Date Monday, May 25, 2020		Last modify date	Page title I2C WRAP	
Designed by:		Controlled by:	approved by:	
PCB Code		BOM file	Sheet 29 of 41	REV. 0
			Format A4	
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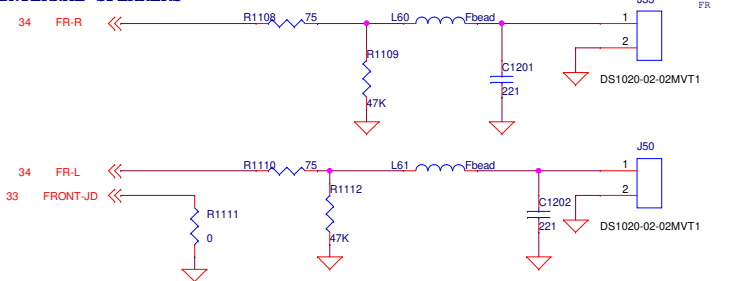
EXTERNAL JACK



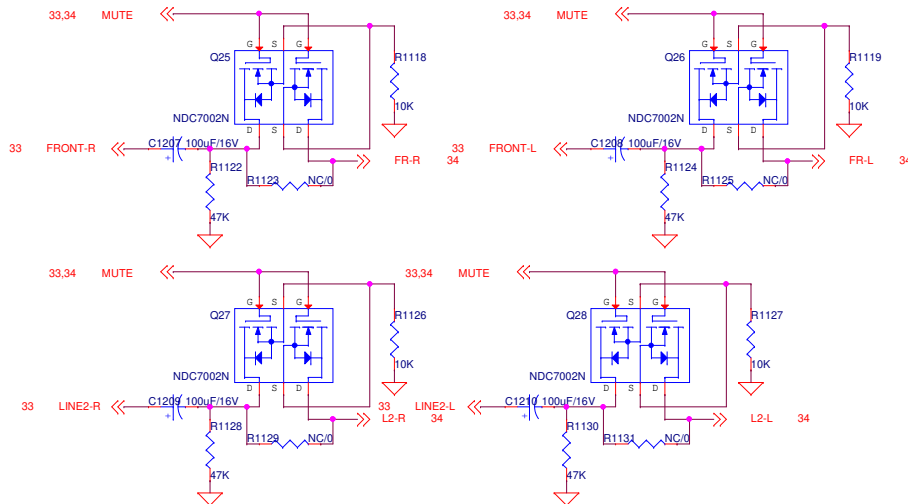
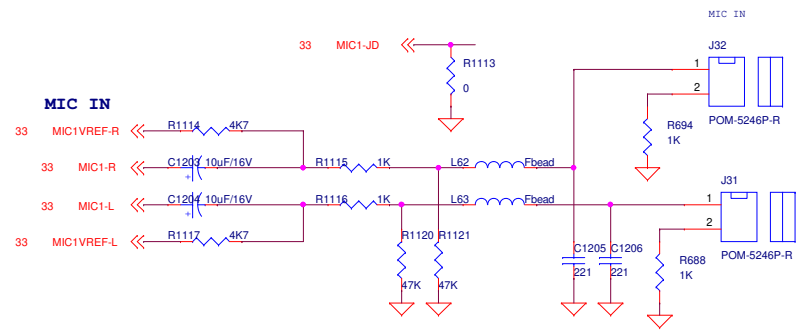
EXT MIC IN



INTERNAL SPEAKERS

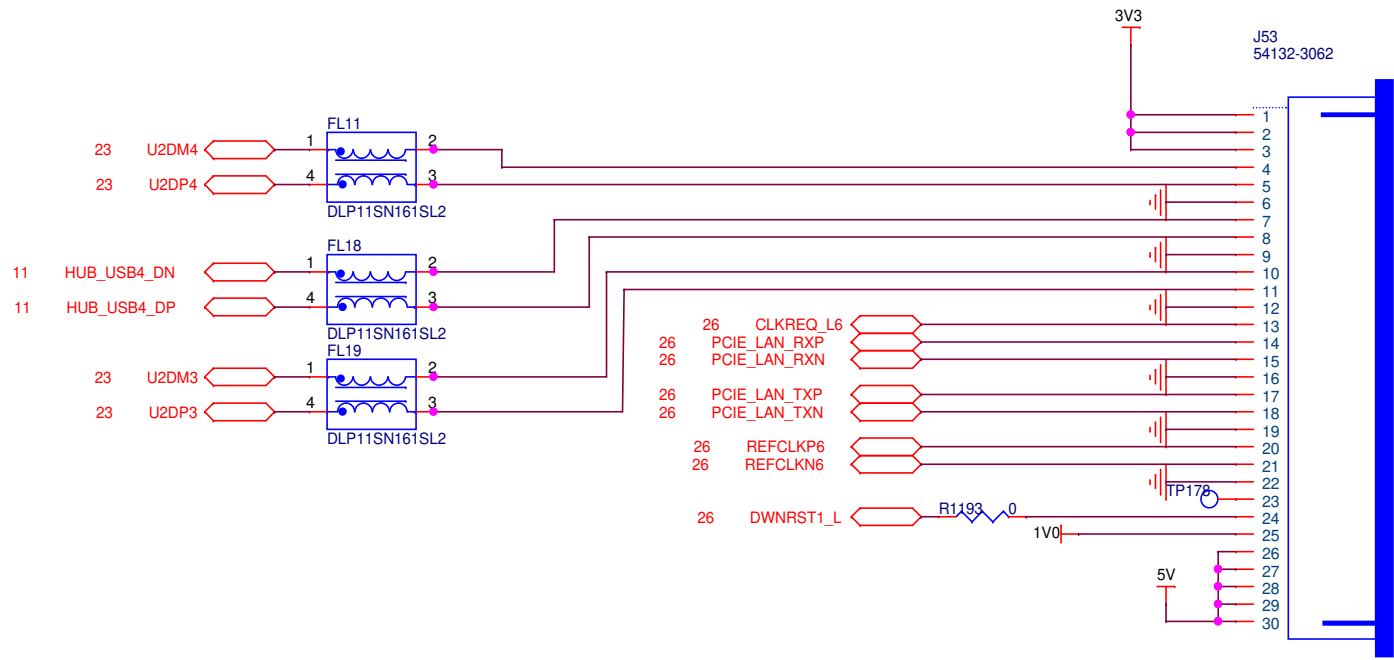


Analog MICs




PROTO

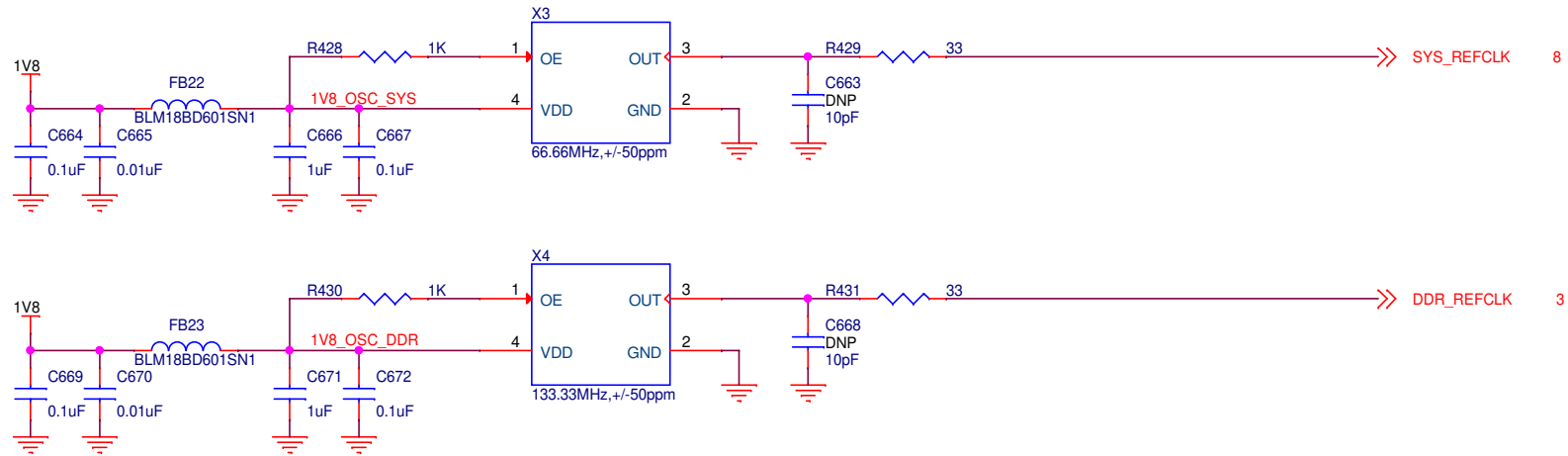
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Creation Date Monday, May 25, 2020	Last modify date	Page title AUDIO CONN	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 31 of 41	REV. 0 Format AS
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PROTO

		Project ACB_0001_0		
Creation Date Monday, May 25, 2020	Last modify date	Page title ETHERNET_CARD		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 31 of 41	REV. 0	Format A4
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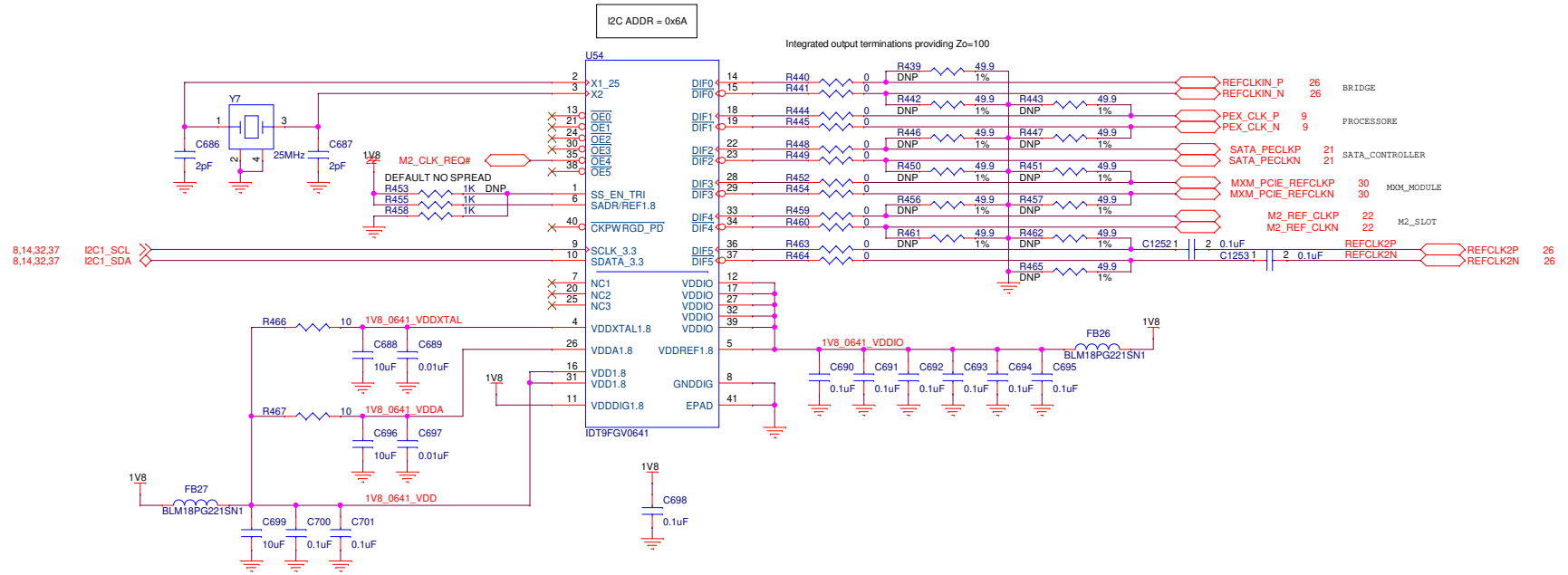
SYSTEM CLOCK GENERATORS




PROTO

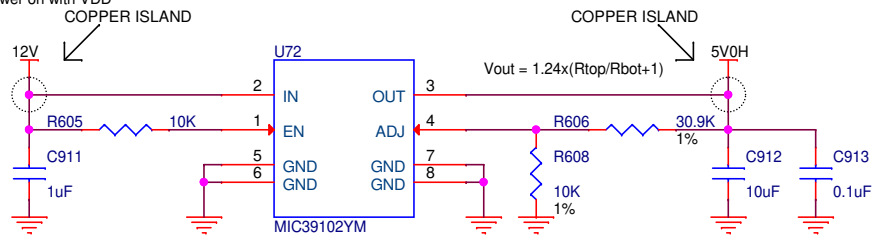
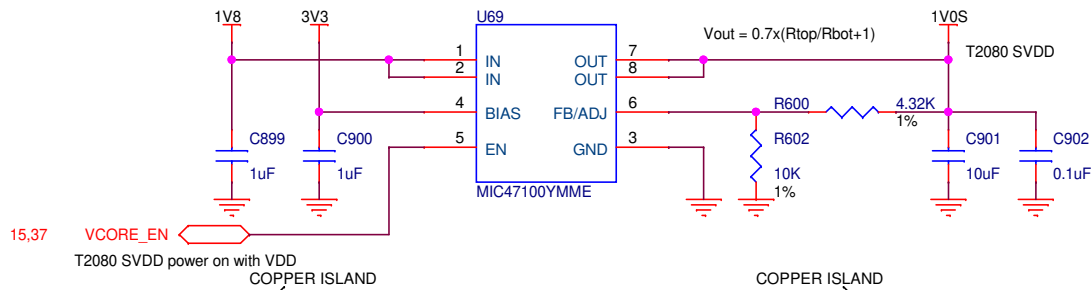
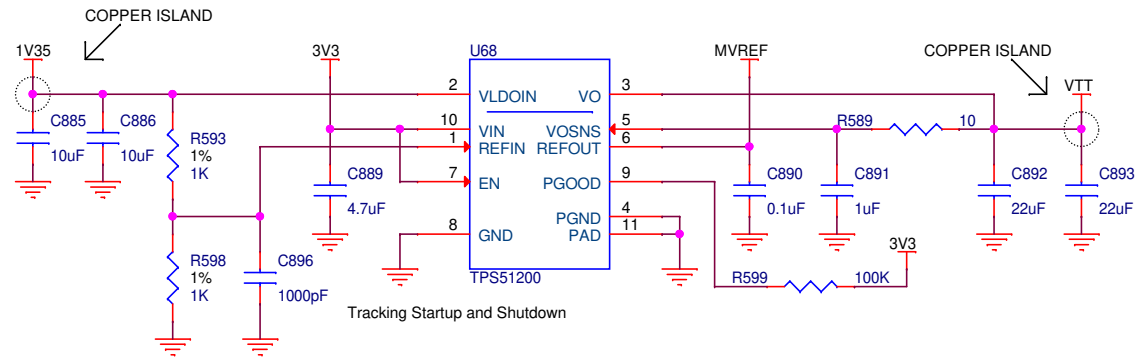
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Creation Date Monday, May 25, 2020	Last modify date	Page title CLOCK 1		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 32 of 41	REV. 0	Format A4
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SYSTEM CLOCK GENERATORS (cont.)




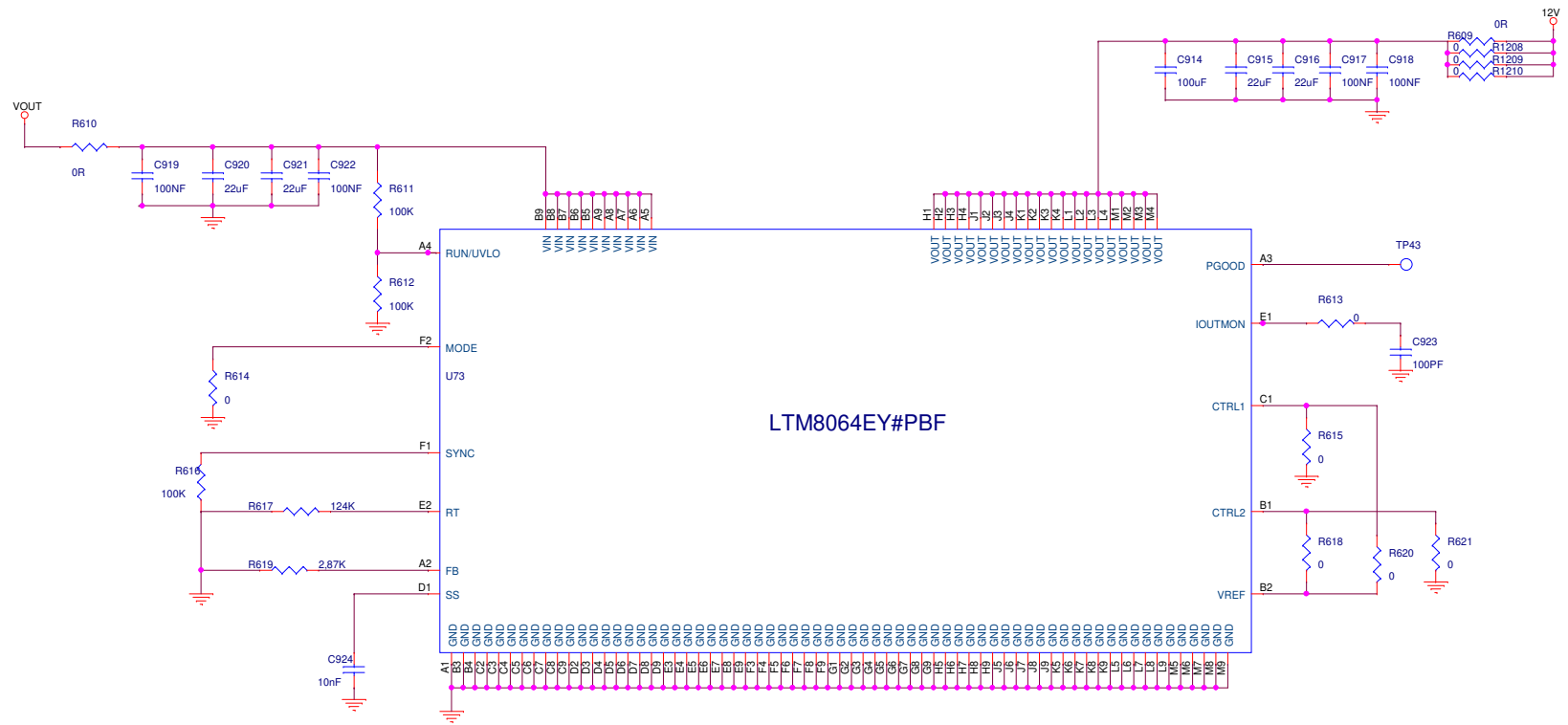
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Creation Date Monday, May 25, 2020	Last modify date	Page title CLOCK 2	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 33 of 41	REV. 0 Format A3
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SYSTEM POWER CONVERTORS (cont.)

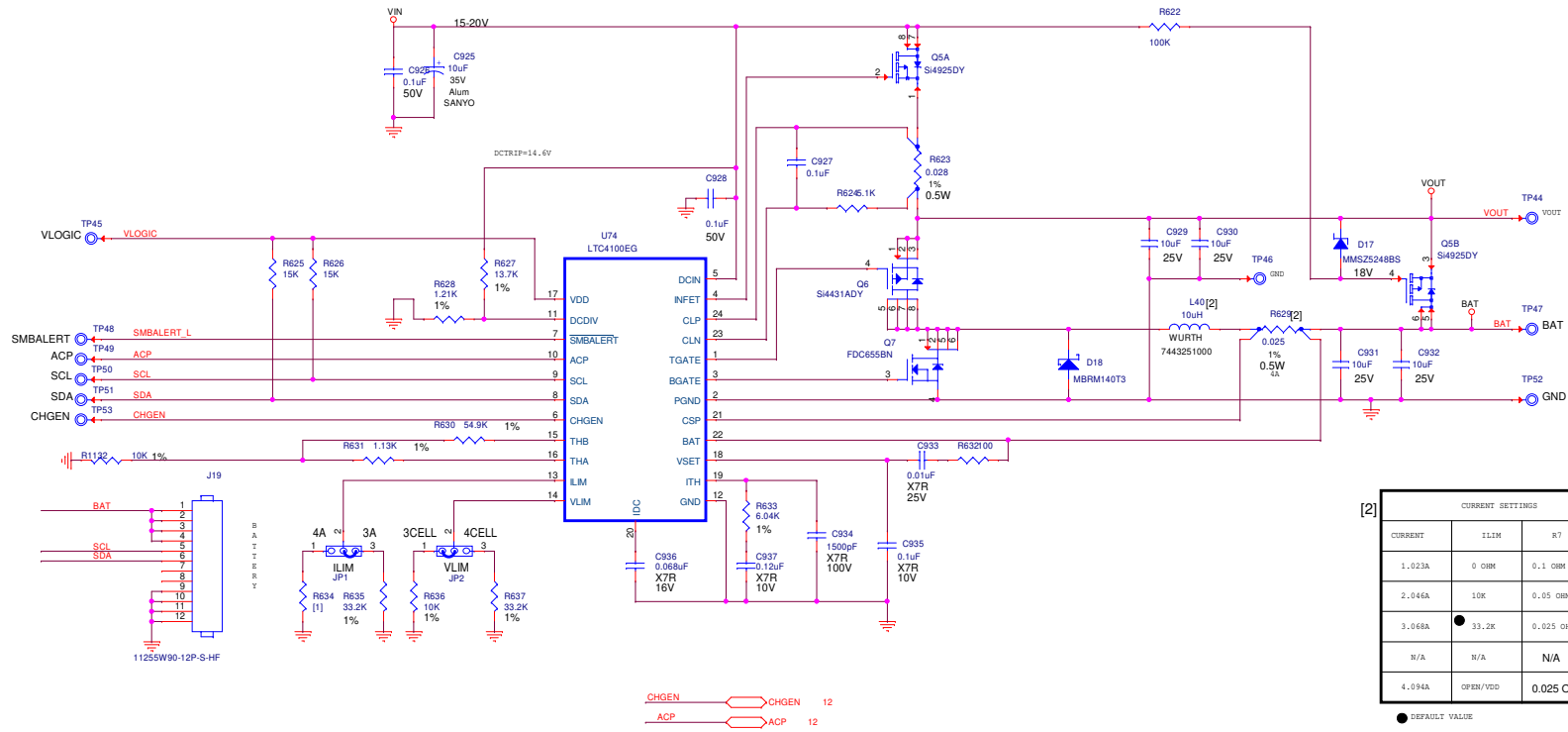


PROTO

		Project ACB_0001_0		
		Creation Date Monday, May 25, 2020	Last modify date	Page title OTHER PWR2
Designed by:		Controlled by:		approved by:
PCB Code	BOM file	Sheet 36 of 41	REV. 0	Format A4
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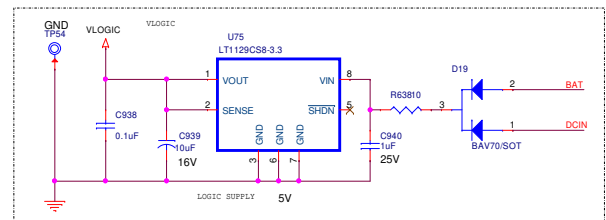
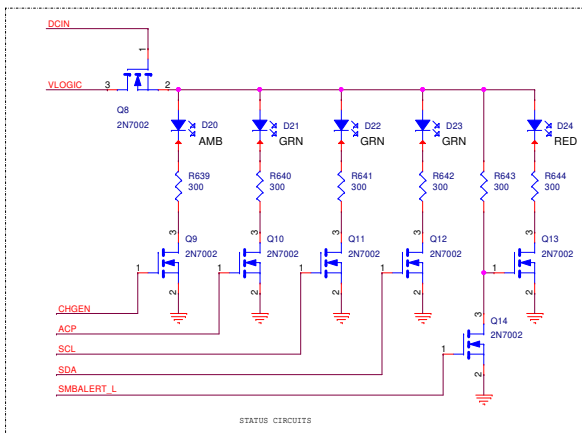


		Project ACB_0001_0	
Creation Date Monday, May 25, 2020	Last modify date	Page title MAIN POWER	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 37 of 41	REV. 0 Format A3
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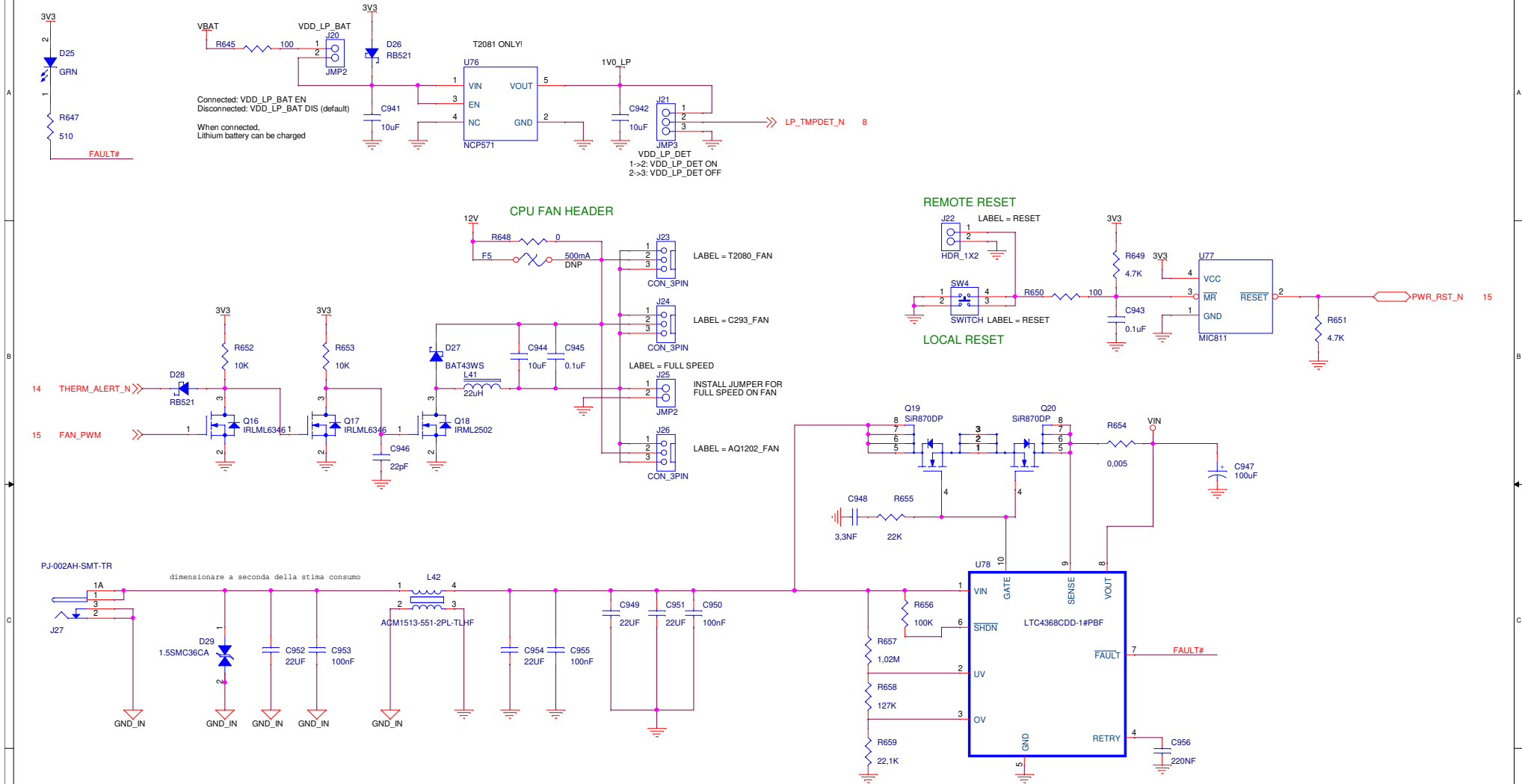
CURRENT SETTINGS				VOLTAGE SETTINGS	
CURRENT	I LIM	R7	LI	VOLTAGE	V LIM
1.023A	0 OHM	0.1 OHM	40uH	8.438V	0 OHM
2.046A	10K	0.05 OHM	20uH	12.646V	10K
3.069A	33.2K	0.025 OHM	10uH	16.870V	33.2K
N/A	N/A	N/A	N/A	21.062V	100K
4.094A	OPEN/VDD	0.025 OHM	10uH	32.758V	OPEN/VDD

● DEFAULT VALUE




PROTO					
		Project ACB_0001_0			
		Creation Date Wednesday, August 08, 2018	Last modify date Monday, May 25, 2020	Page title BATTERY CHARGE	
Designed by: -<Author>		Controlled by: -<Checked by>		approved by: -<Approved by>	
PCB Code		BOM file		Sheet 38 of 41	REV. 0
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SYSTEM POWER INPUT




		Project ACB_0001_0	
Creation Date Monday, May 25, 2020	Last modify date	Page title PWR IN	
Designed by:	Controlled by:	approved by:	
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PROTO

		Project ACB_0001_0		
Creation Date Monday, May 25, 2020	Last modify date	Page title MECANICAL		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet of	REV. 0	Format B
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CHANGE LIST

PROTO

		Project ACB_0001_0		
Creation Date Monday, May 25, 2020	Last modify date	Page title CHANGE LIST		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 41 of 41	REV. 0	Format B
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