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4	T2080 SECOND BANK DDR3L INTERFACE
5	T2080 IFC INTERFACE
6	T2080 NOR and NAND FLASH INTERFACE
7	T2080 SPI FLASH and SDHC INTERFACE
8	T2080 SYSTEM LOGIC INTERFACE
9	T2080 ETHERNET and SERDES INTERFACE
10	T2080 USB INTERFACE
11	USB_HUB
12	KEYBOARD INTERFACE
13	KB_LED_AND_LED
14	T2080 DUART and I2C DEVICE INTERFACE
15	CPLD WRAPPER AND IO EXPANDER
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18	T2080 GROUND
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20	ETHERNET PORT CONNECTOR
21	SATA3 CONTROLLER
22	SATA3 CONNECTORS
23	USB3 CONTROLLER
24	USB3 CONTROLLER CONNECTORS
25	ETHERNET CARD
26	PCIE BRIDGE
27	PCIE CONNECTORS
28	3G LTE MODEM
29	PCIE BRIDGE POWER
30	MXM PCIE
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32	I2C WRAPPER
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38	SYSTEM POWER CONVERTORs
39	SYSTEM POWER CONVERTORs (cont.)
40	MAIN POWER
41	BATTERY CHARGER
42	SYSTEM POWER INPUT
43	MECHANICALs
44	CHANGE LIST

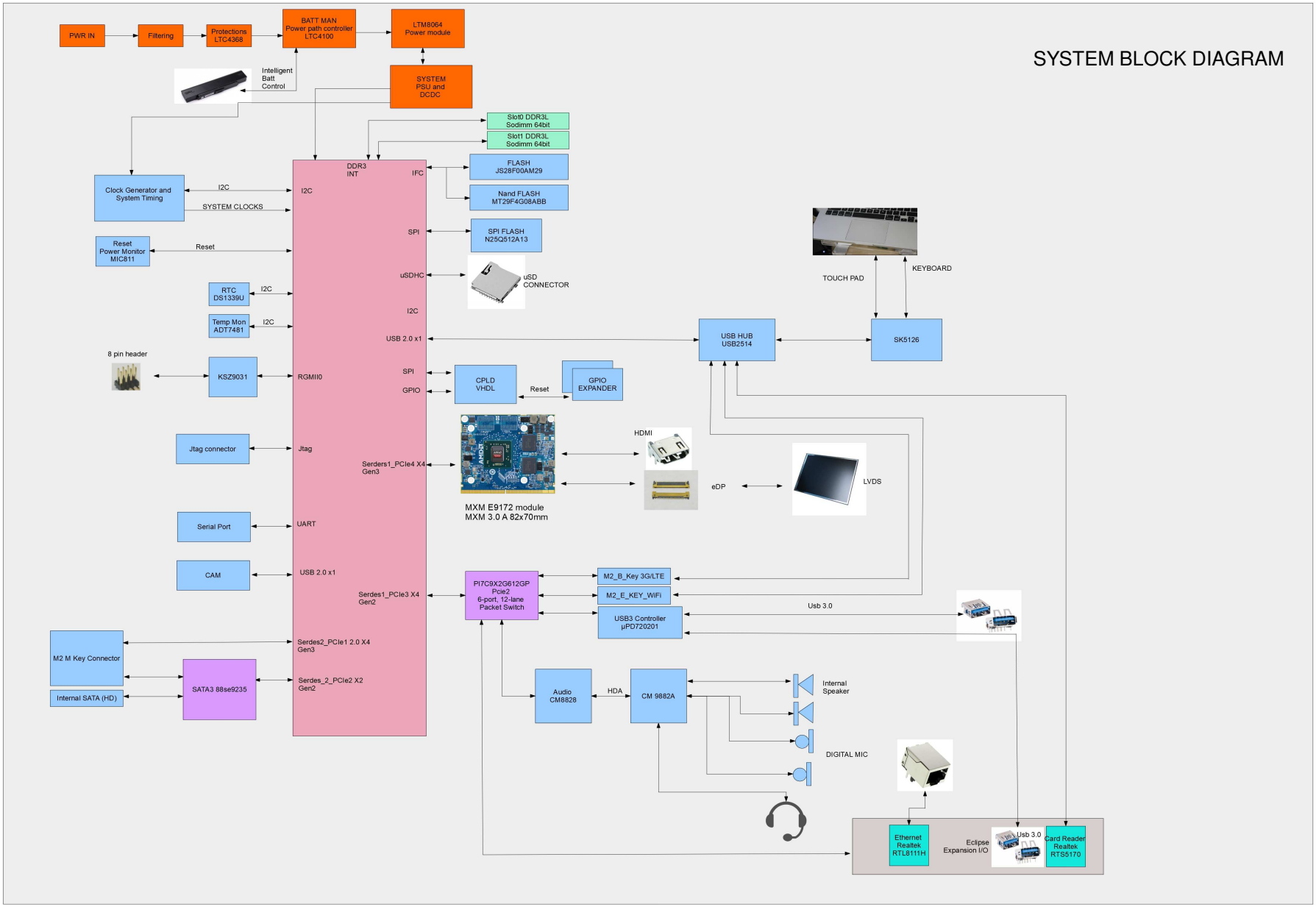
Version Control

Version	Date	Modifications
V0.1	2018/12	First release of Schematics
V0.2	2019/09	Second release of Schematics
V0.3	2020/04	Third release of Schematics
V0.4	2020/05	Fourth release of Schematics
V0.5	2020/06	Fifth release of Schematics

<Variant Name>

PPC Power Progress Community	Project **ACB_0001_0**		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: PAGE LISTING	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 1 of 44 / REV. 0	Format B

SYSTEM BLOCK DIAGRAM



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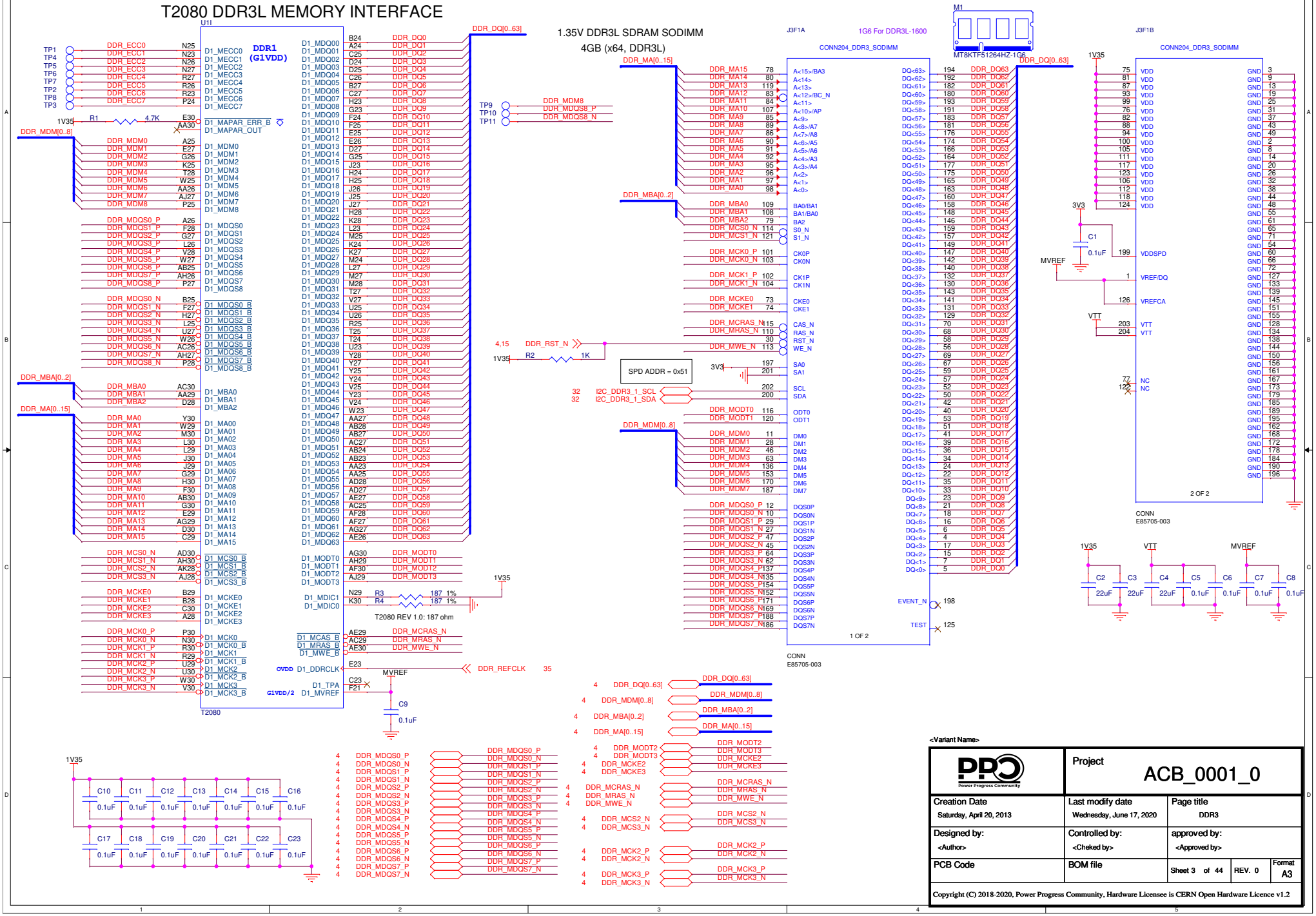
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: BLOCKDIAGRAM
Designed by:	Controlled by:	approved by:
PCB Code	MCM file	Sheet: 2 of 26 Rev: A Size: A4

T2080 DDR3L MEMORY INTERFACE



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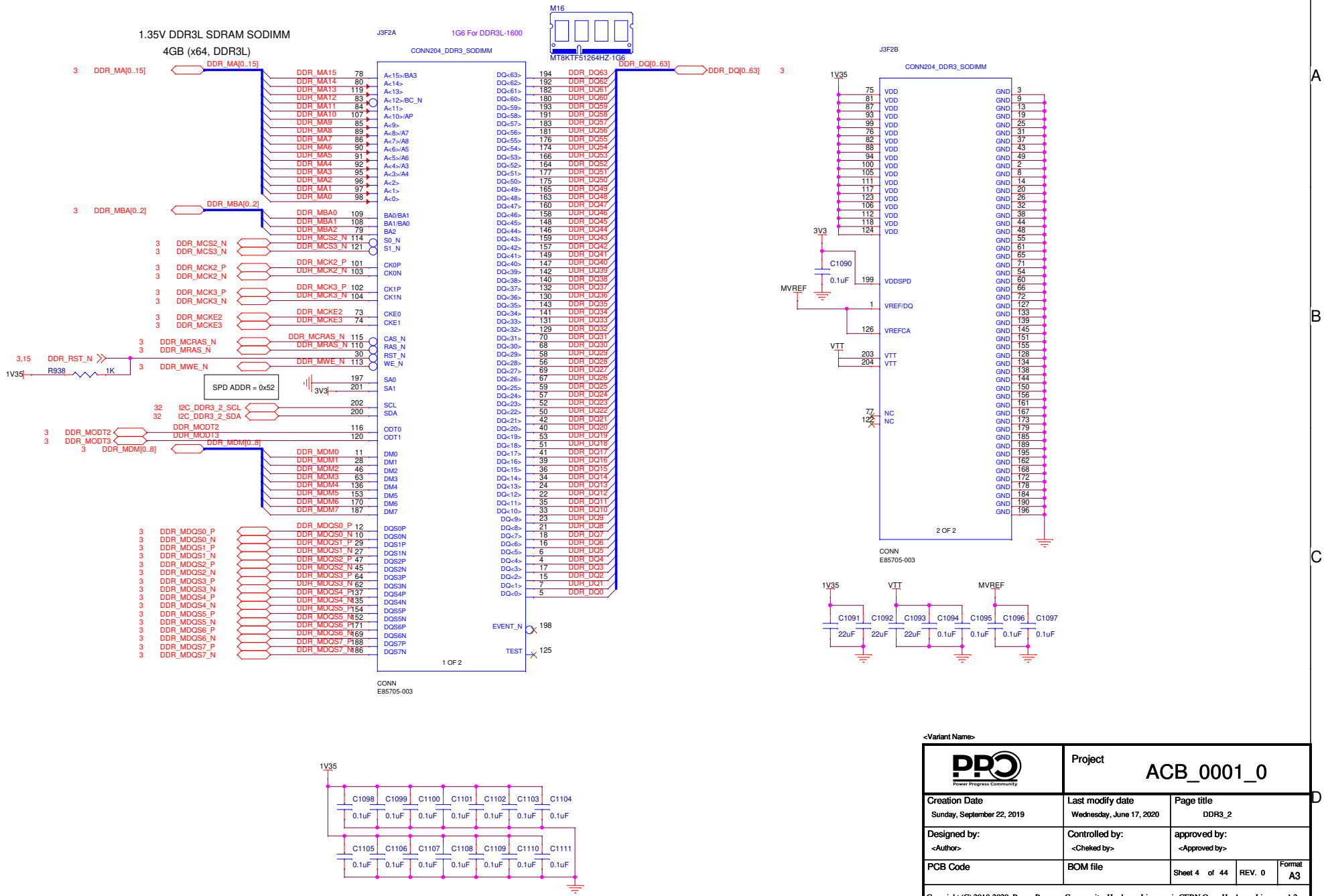
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 3 of 44 / REV. 0 / Format A3



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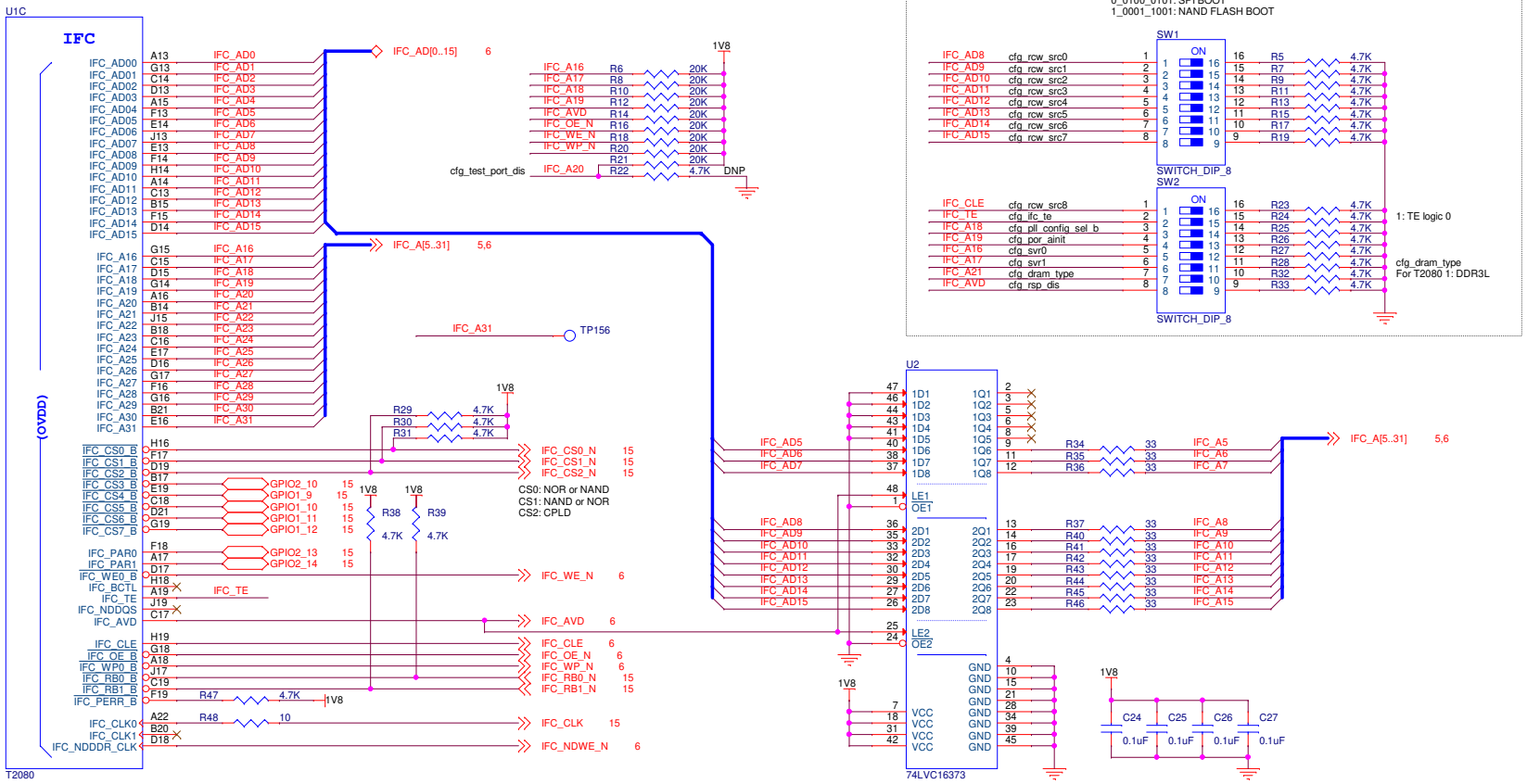
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 4 of 44 / REV. 0	Format A3

T2080 IFC INTERFACE

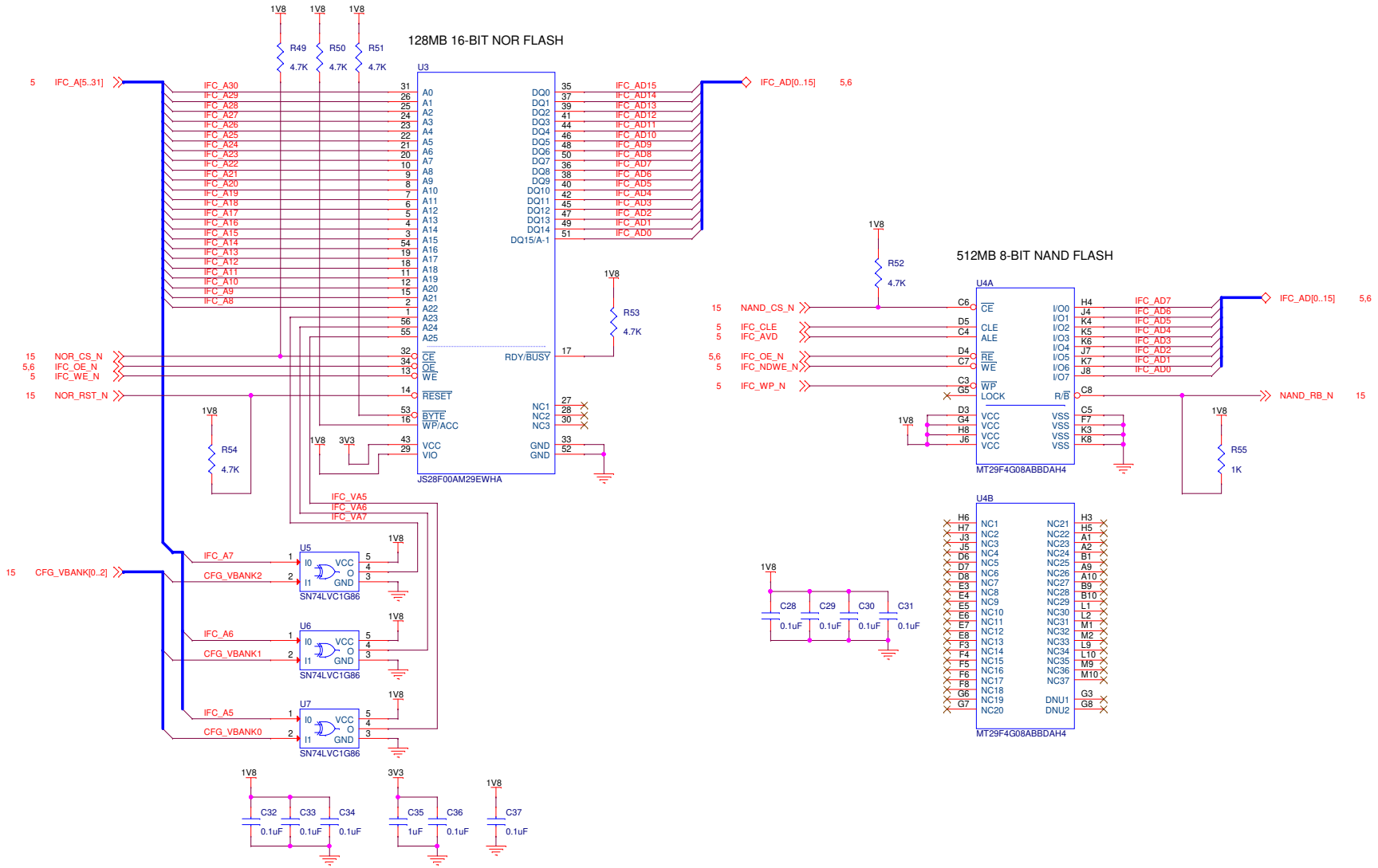


<Variant Name>

Project
ACB_0001_0

Creation Date	Last modify date	Page title
Wednesday, June 17, 2020		IFC
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 5 of 44 / REV. 0 / Format A3

T2080 NOR and NAND FLASH INTERFACE



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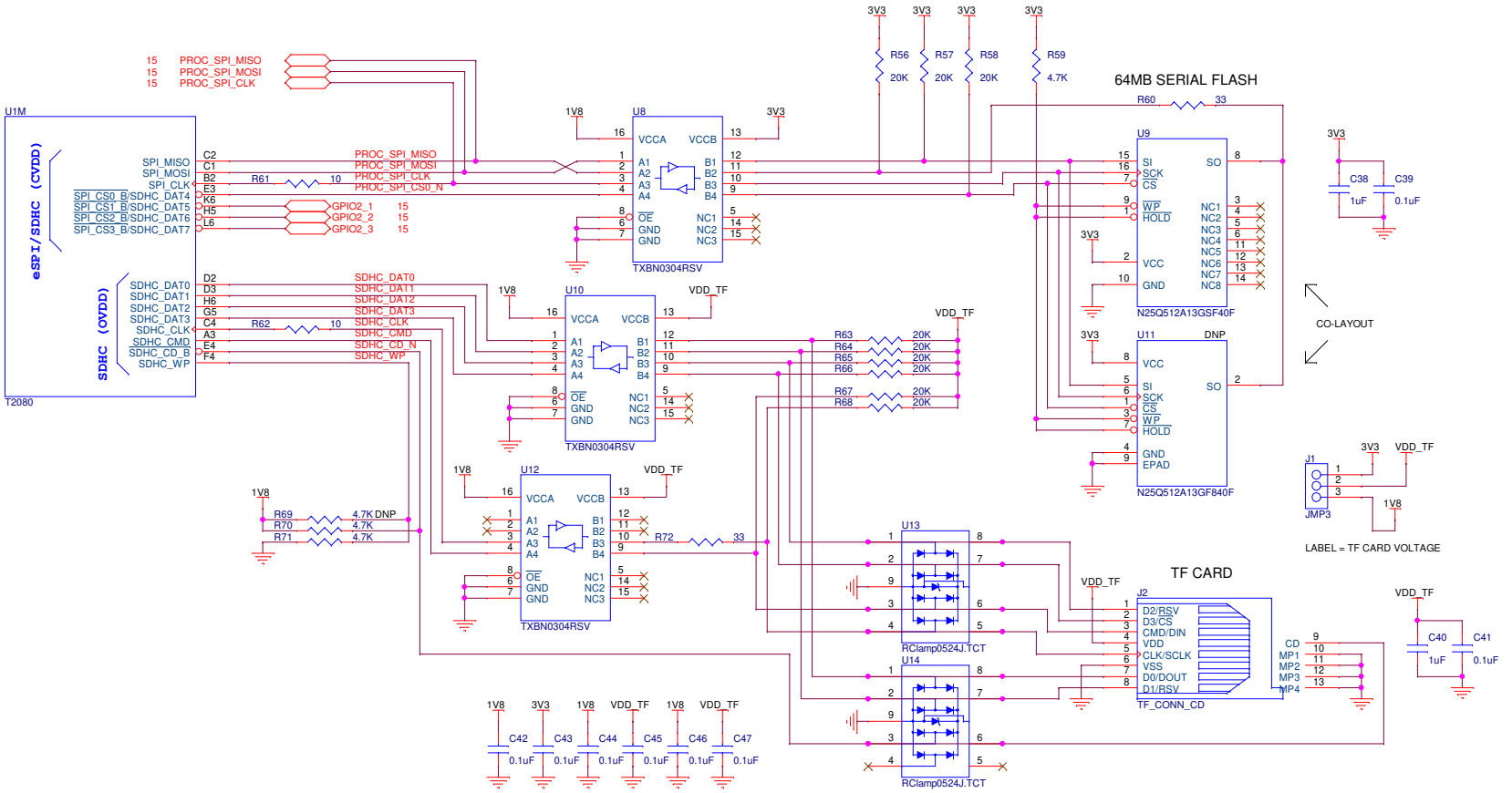
Project: ACB_0001_0		
Creation Date: Wednesday, June 17, 2020	Last modify date:	Page title: FLASH
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 6 of 44 / REV. 0 / Format A3

T2080 SPI FLASH and SDHC INTERFACE



<Variant Name>

Project **ACB_0001_0**		
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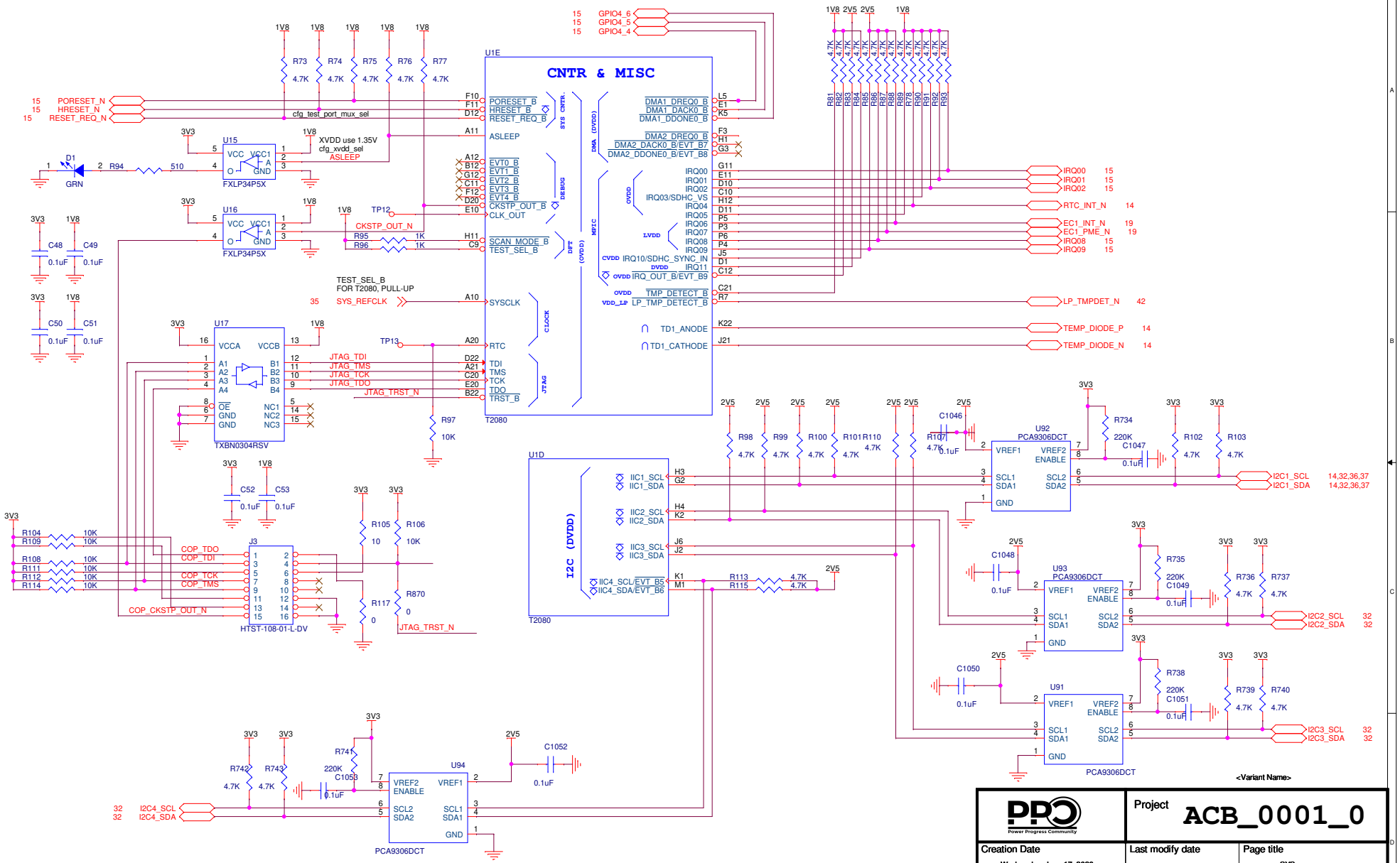
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 7 of 44 / REV. 0 / Format A3

T2080 SYSTEM LOGIC INTERFACE



T2080 ETHERNET and SERDES INTERFACE

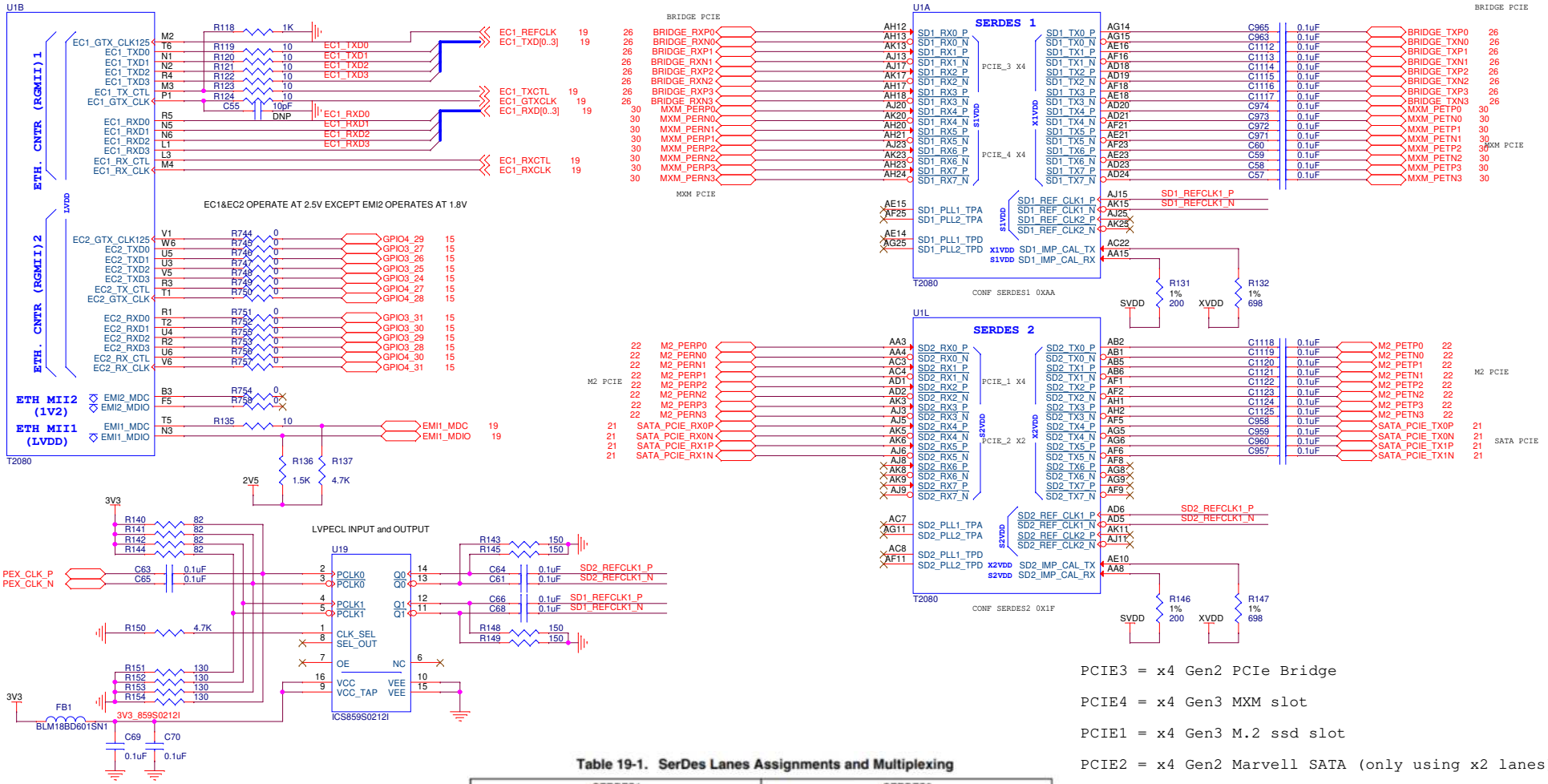


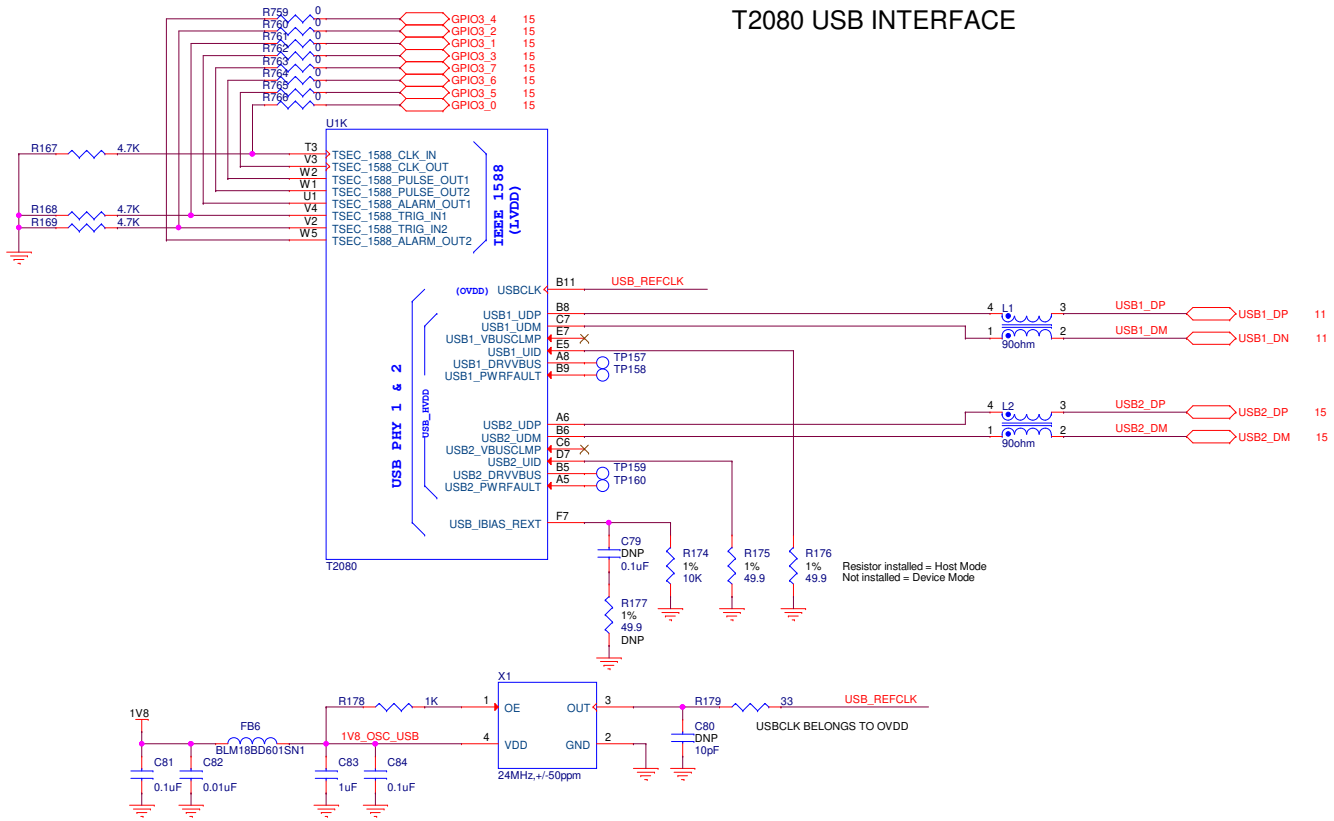
Table 19-1. SerDes Lanes Assignments and Multiplexing

	SERDES1									SERDES2								
SRDS_PRTCL_S1	A	B	C	D	E	F	G	H	Per Lane PLL Mapping	SRDS_PRTCL_S2	A	B	C	D	E	F	G	H	Per Lane PLL Mapping
AA	PCIe3				PCIe4				1111 1111	1F[1]	PCIe1				PCIe2				1111 2222

<Variant Name>

Project: ACB_0001_0		
Creation Date	Last modify date	Page title: EC&SD
Designed by: Wednesday, June 17, 2020	Controlled by:	approved by:
PCB Code	BOM file	Sheet 9 of 44 / REV. 0 / Format A3

T2080 USB INTERFACE



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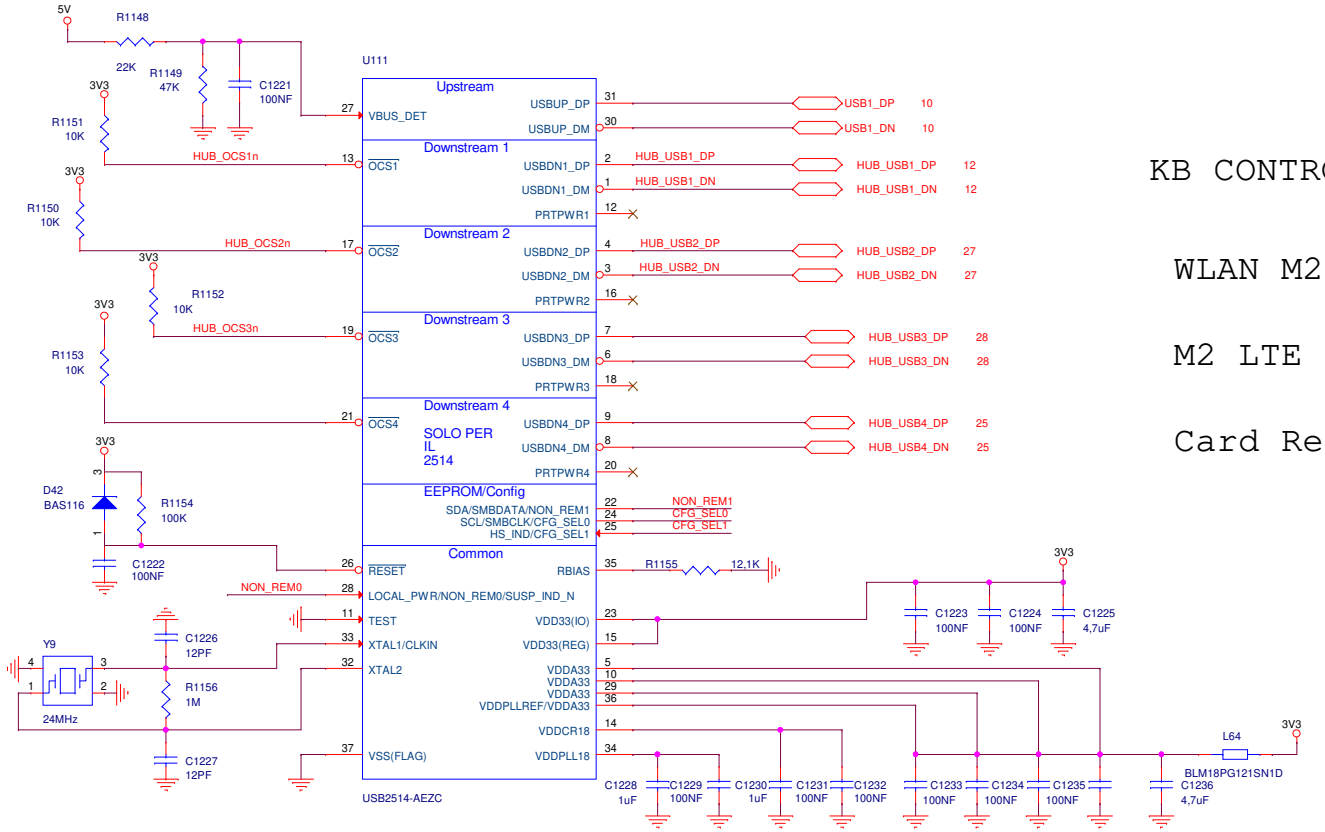
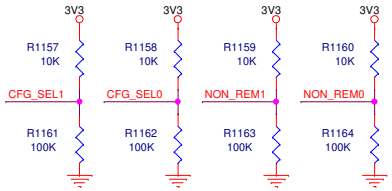
Project ACB_0001_0		
Creation Date	Last modify date	Page title: USB
Designed by: Wednesday, June 17, 2020	Controlled by:	approved by:
PCB Code	BOM file	Sheet 10of 44 / REV. 0 / Format A3

HUB USB





KB CONTROLLER

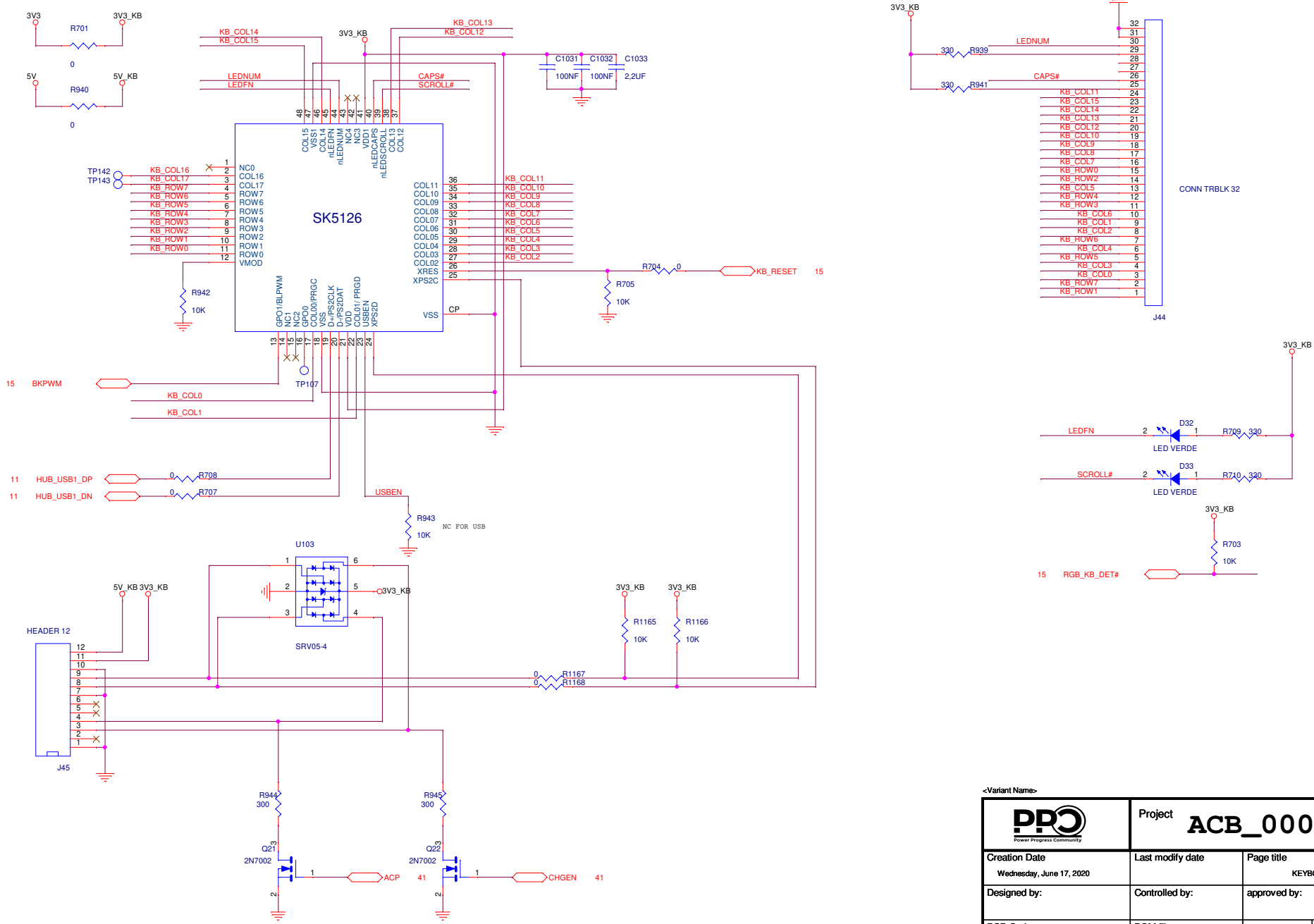
WLAN M2

M2 LTE

Card Reader

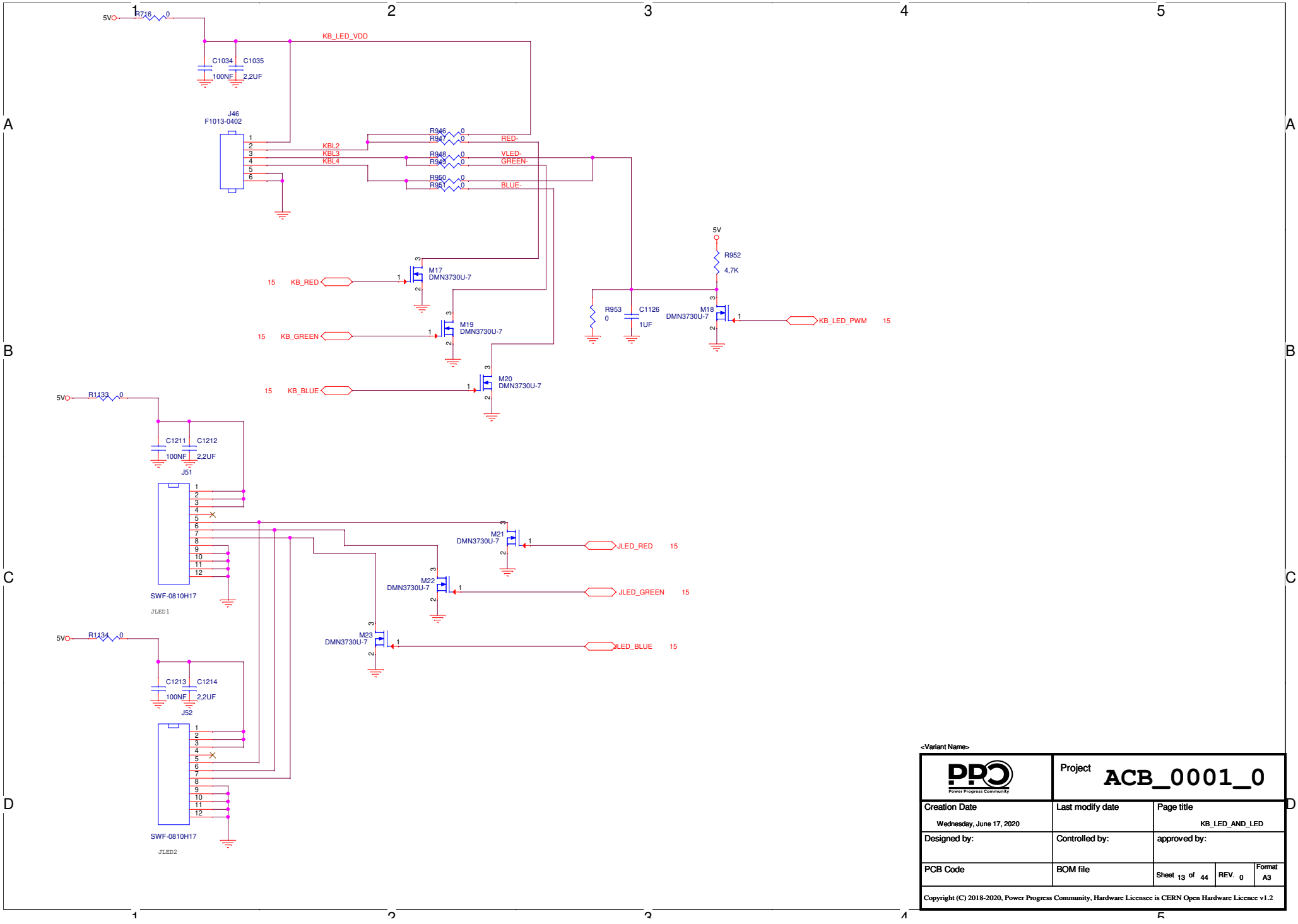
<Variant Name>

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date:	Page title: USB HUB
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 11of 44 / REV. 0 / Format A3



<Variant Name>

Project **ACB_0001_0**		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: KEYBOARD
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 12of 44 / REV. 0 / Format A3



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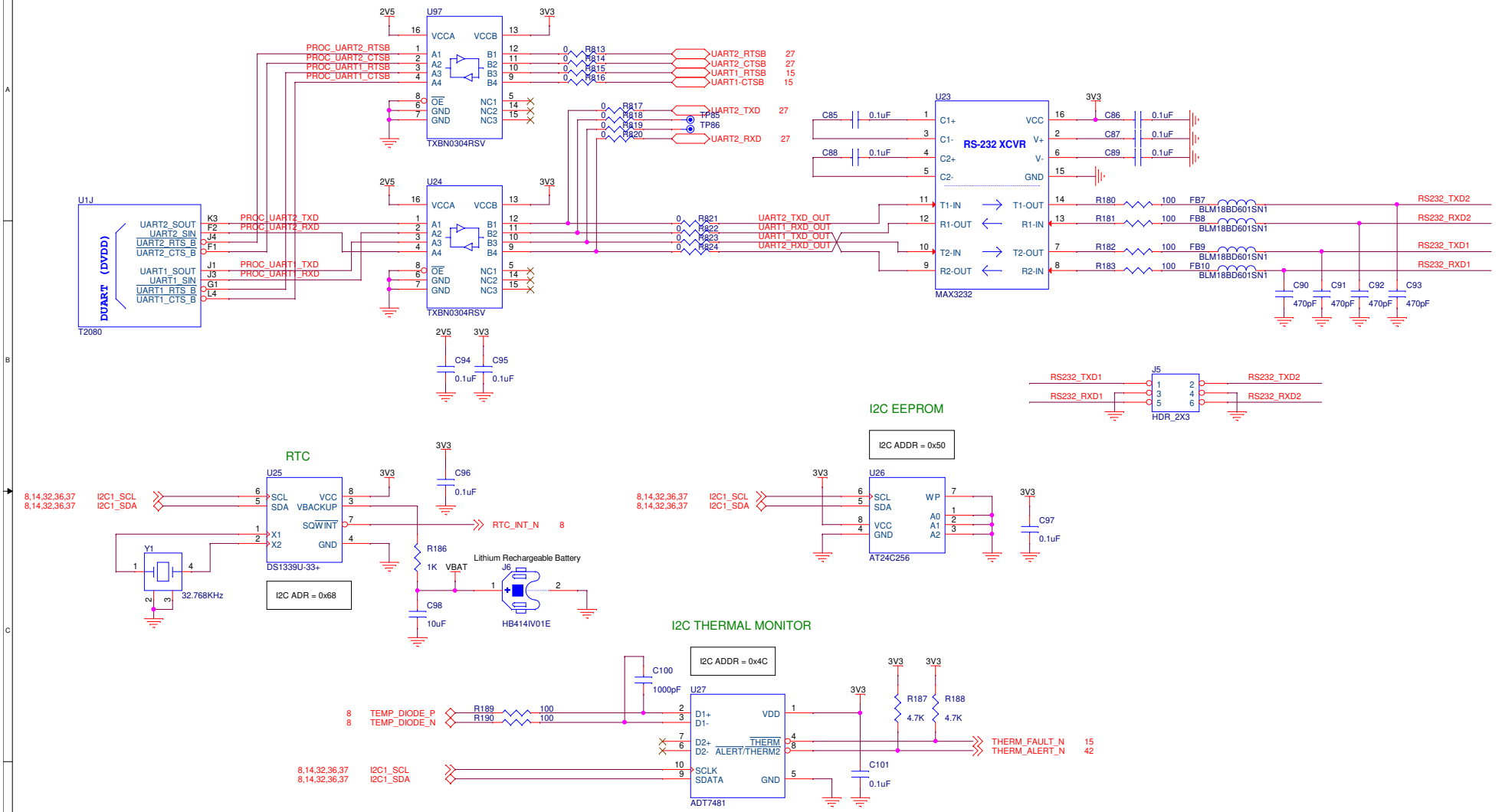
PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: KB_LED_AND_LED
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 13 of 44 / REV. 0 / Format A3

T2080 DUART and I2C DEVICE INTERFACE



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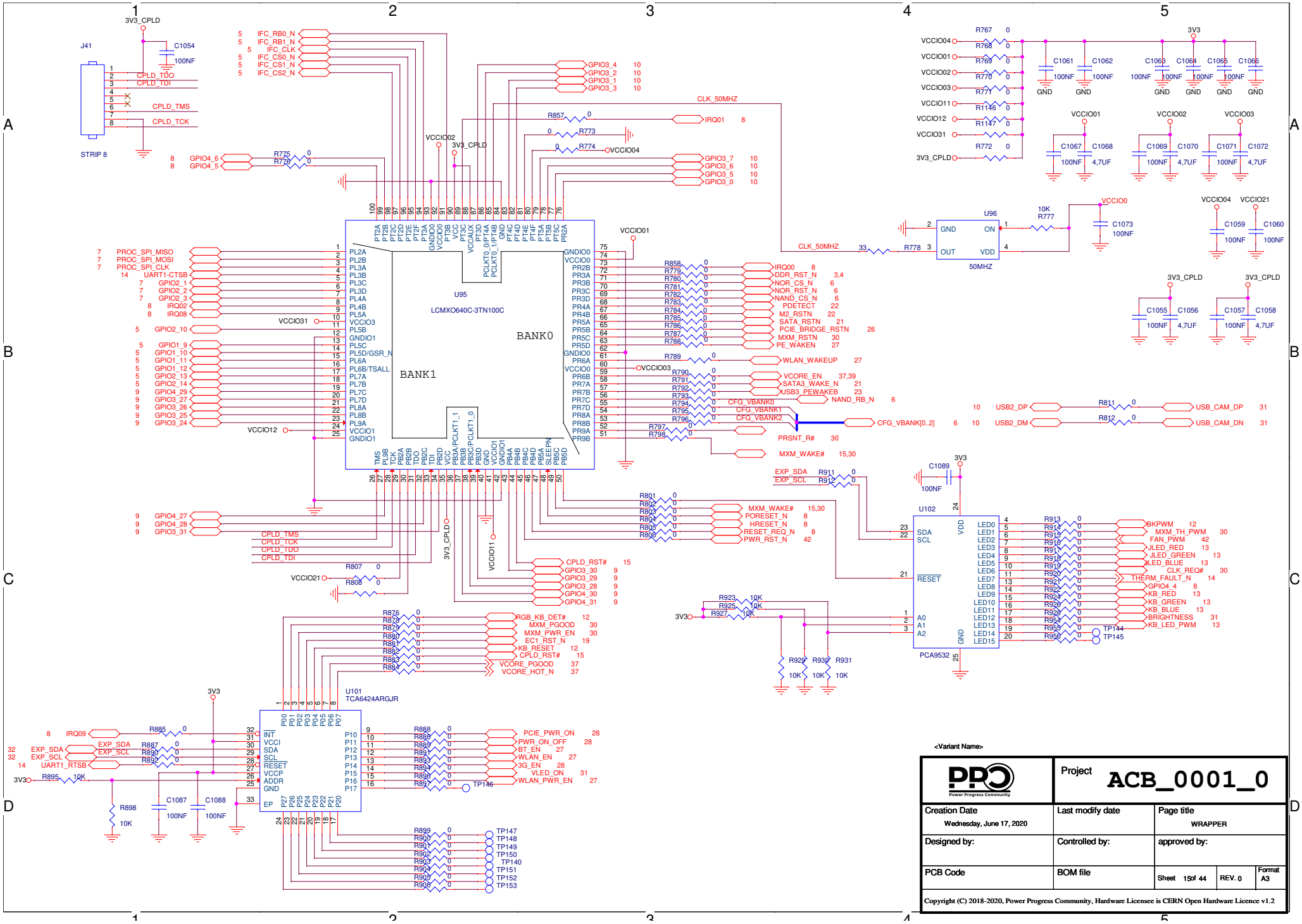
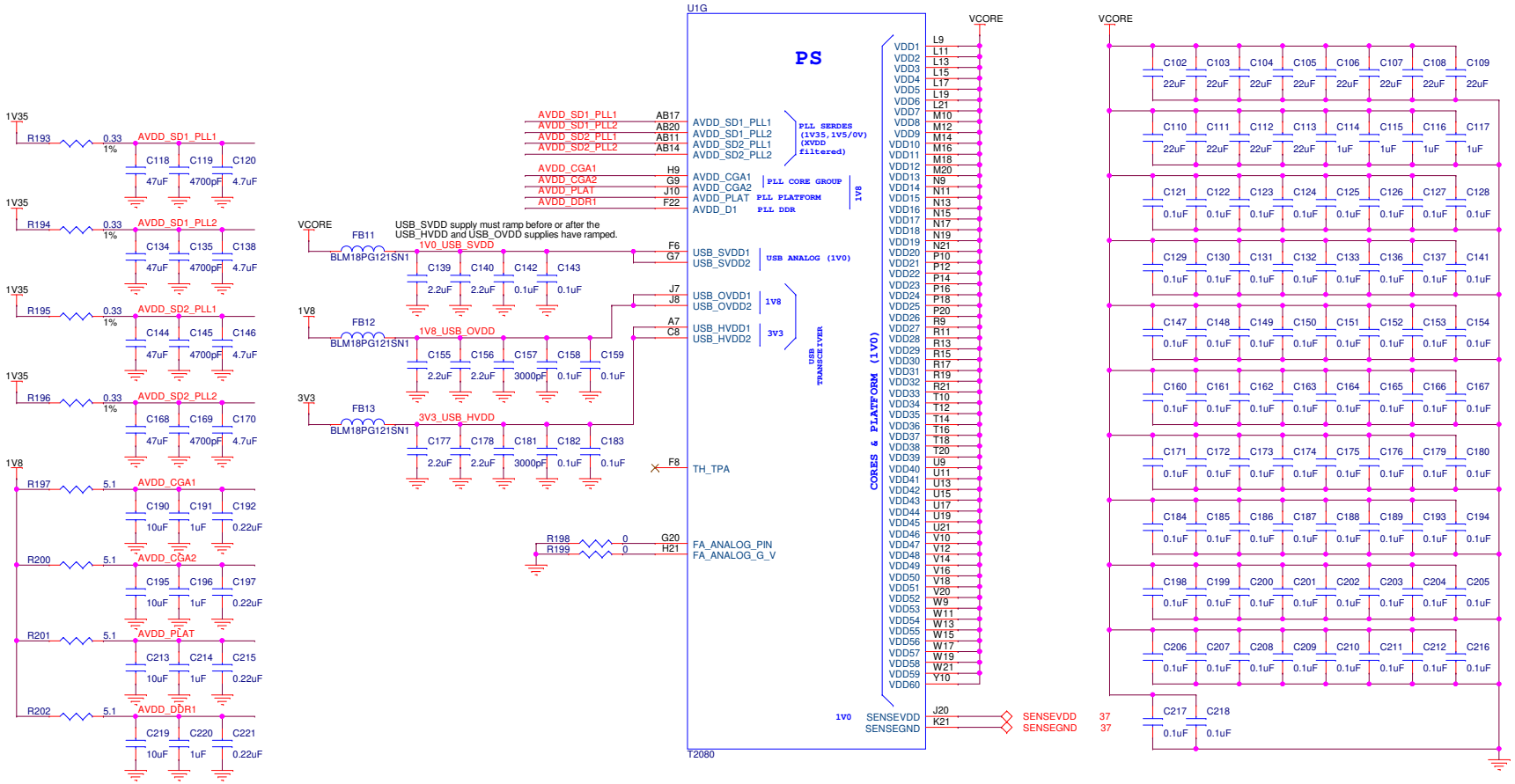
Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date:	Page title: UART&I2C
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 14of 44 / REV. 0 / Format A3


J41
STRIP 8
CPLD_TDO
CPLD_TDI
CPLD_TMS
CPLD_TCK
U95
LCMXO640C-3TN100C
BANK0
BANK1
U96
50MHZ
U102
PCA9532
U101
TCA6424ARGJR
<Variant Name>
Project ACB_0001_0
Power Progress Community
Creation Date Wednesday, June 17, 2020
Last modify date
Page title WRAPPER
Designed by:
Controlled by:
approved by:
PCB Code
BOM file
Sheet 15of 44
REV. 0
Format A3
Copyright (C) 2018-2020, Power Progress Community, Hardware Licensee is CERN Open Hardware Licence v1.2

T2080 POWER SUPPLY



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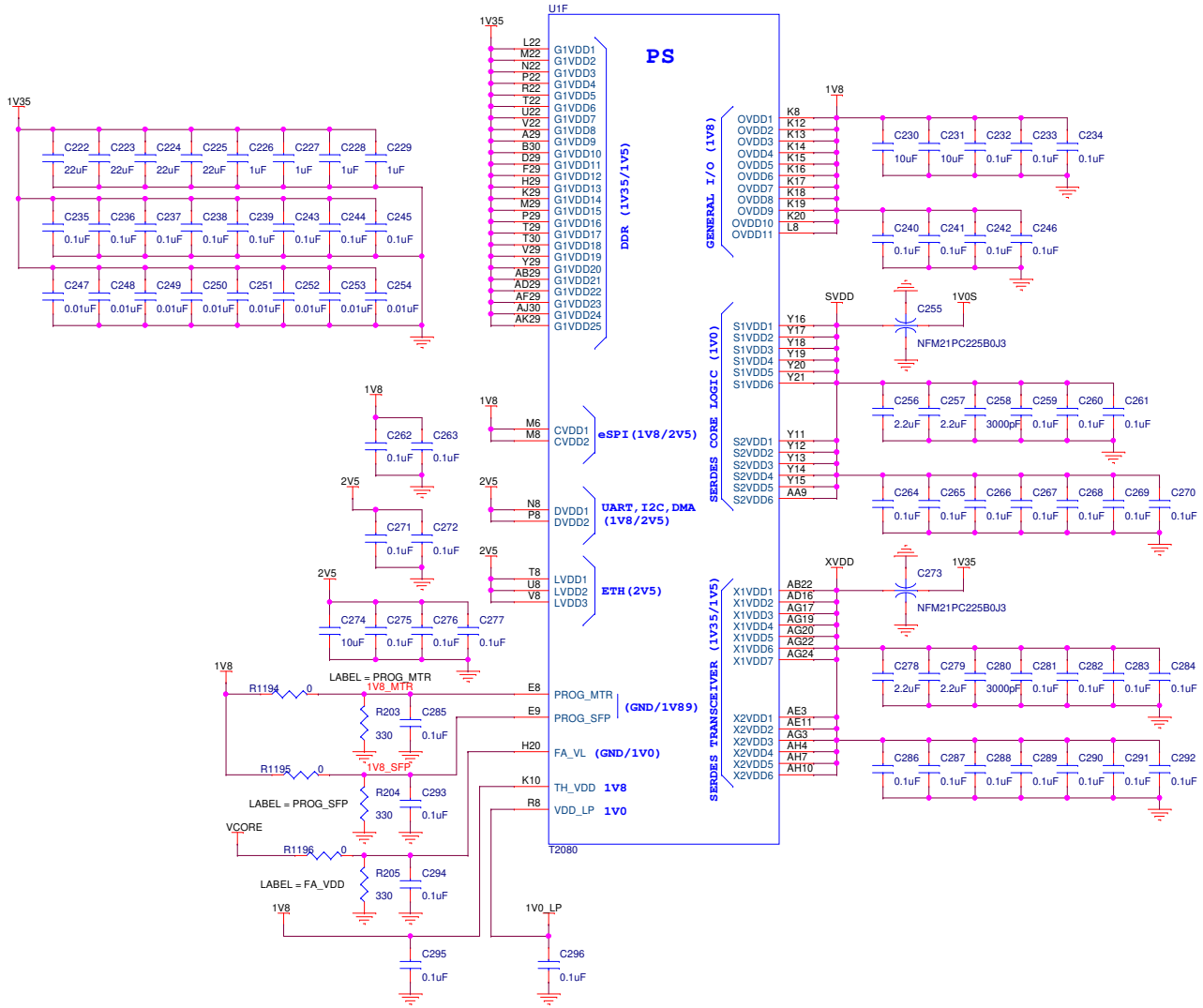
Project ACB_0001_0		
Creation Date: Wednesday, June 17, 2020	Last modify date:	Page title: PROC PWR1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 16of 44 / REV. 0 / Format A3

T2080 POWER SUPPLY (cont.)



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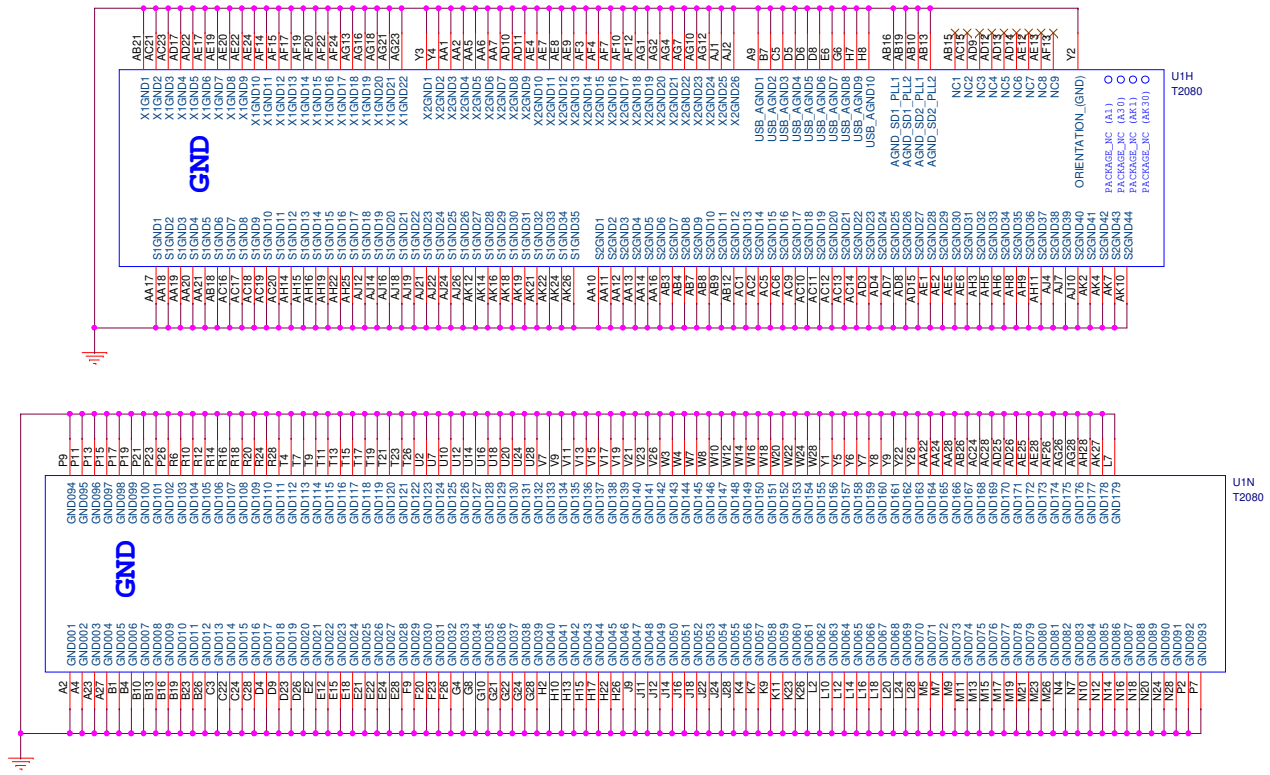
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: PROC PWR2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet17 of 44 / REV. 0 / Format A3

T2080 GROUND



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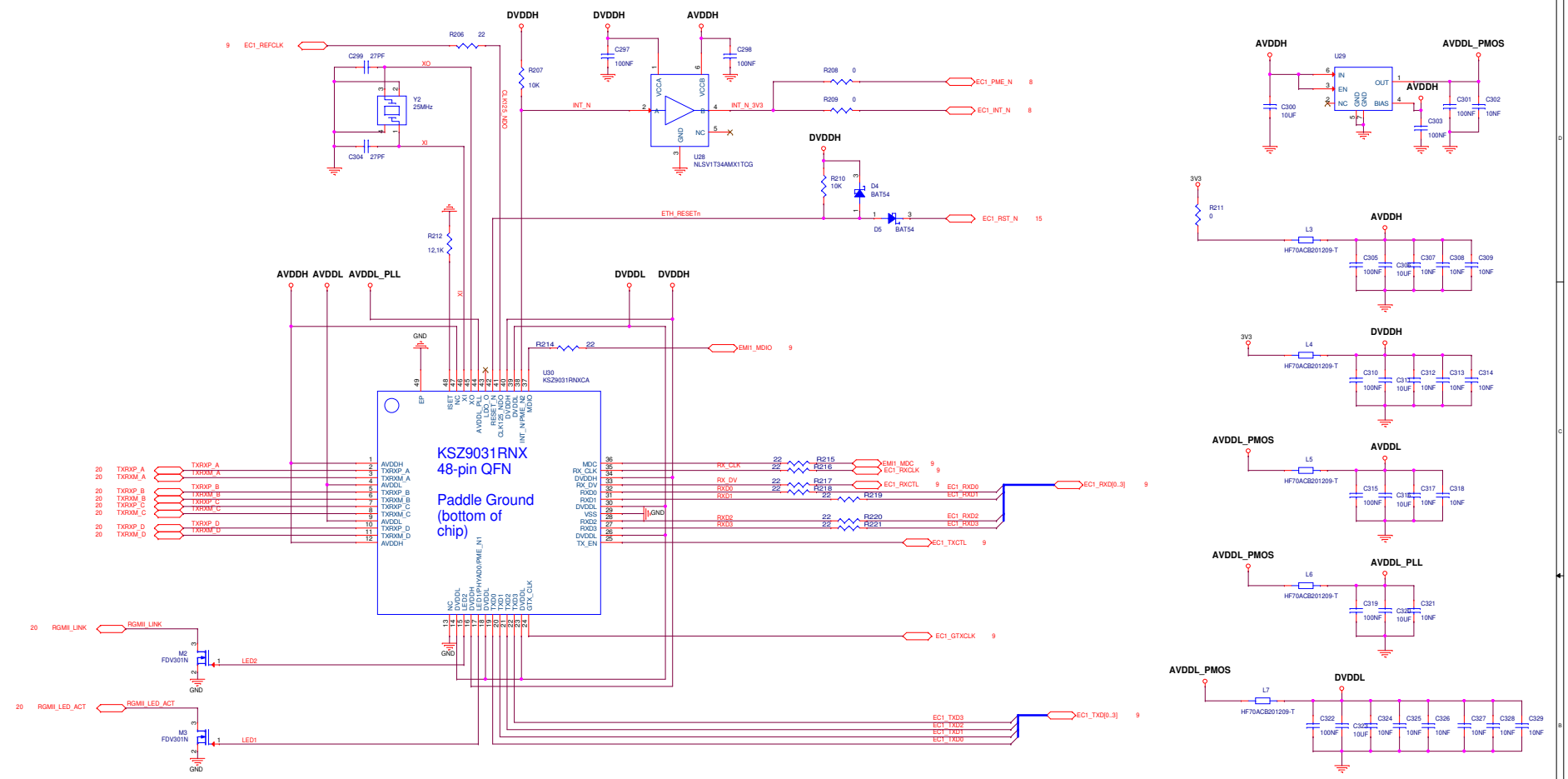
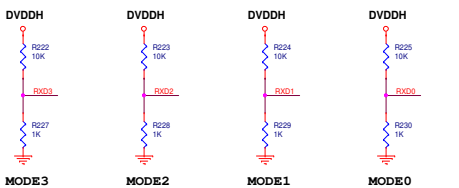
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: PROC GND
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 18 of 44 / REV. 0 / Format A3



Strapping Pins

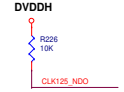


MODE[3:0]	Description
0000	reserved
0001	reserved
0010	reserved
0011	reserved
0100	NAND Tree mode
0101	reserved
0110	reserved
0111	Chip Power Down

MODE[3:0]	Description
1000	reserved
1001	reserved
1010	reserved
1011	reserved
1100	Advertise 1000BT full-duplex only (RGMII)
1101	Advertise 1000BT full- and half-duplex only (RGMII)
1110	Advertise all capabilites, except 1000BT half-duplex (RGMII)
1111	Advertise all capabilites (RGMII)

Strapping Pin

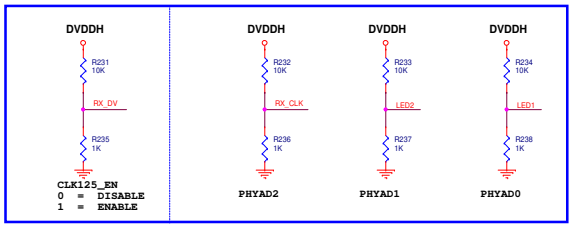
Single LED Mode



Single LED Mode

Pin	Description
LED2	1 : Link off 0 : Link on (any speed), solid color
LED1	Blinking : Activity (RX, TX)

Strapping Pins



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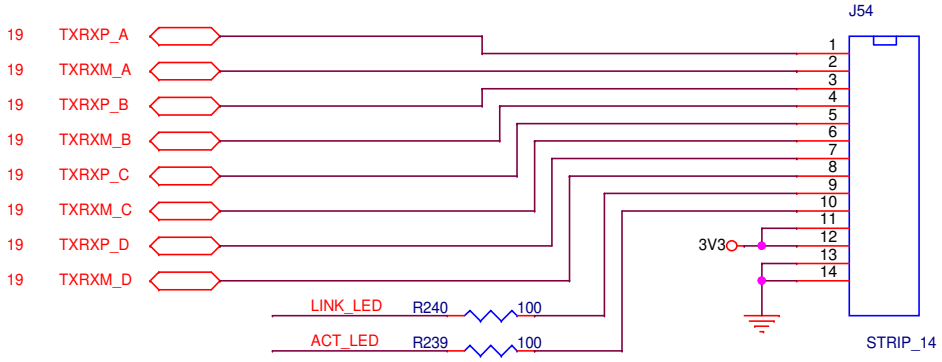
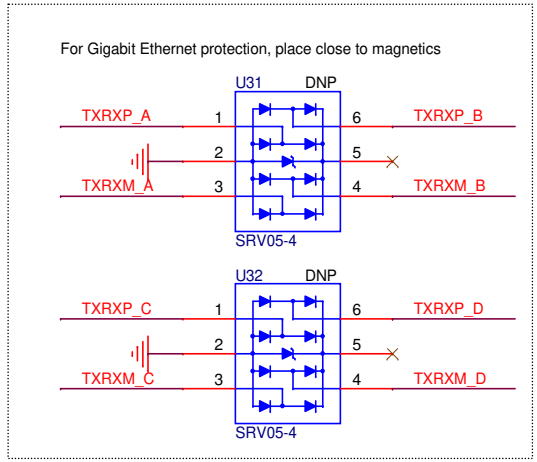
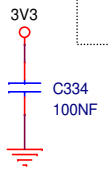
Creation Date: Friday, August 17, 2018	Last modify date: Wednesday, June 17, 2020	Page title: EC1 PHY
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 19 of 44 / REV. 0 / Format A2

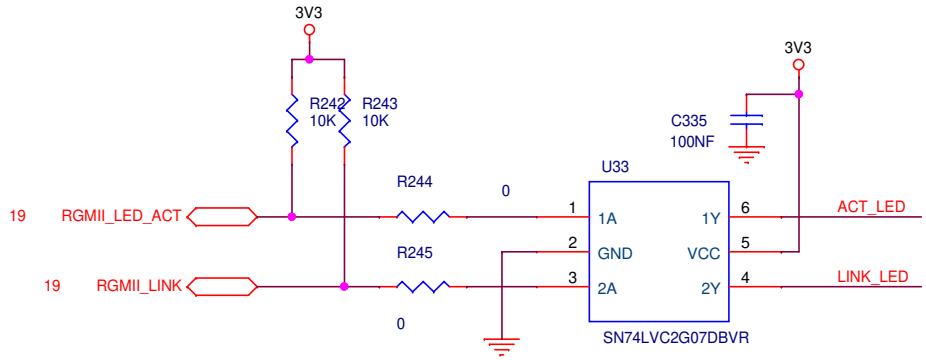
Gigabit Ethernet







Led Ethernet Buffer



<Variant Name>

PPC Power Progress Community	Project ACB_0001_0		
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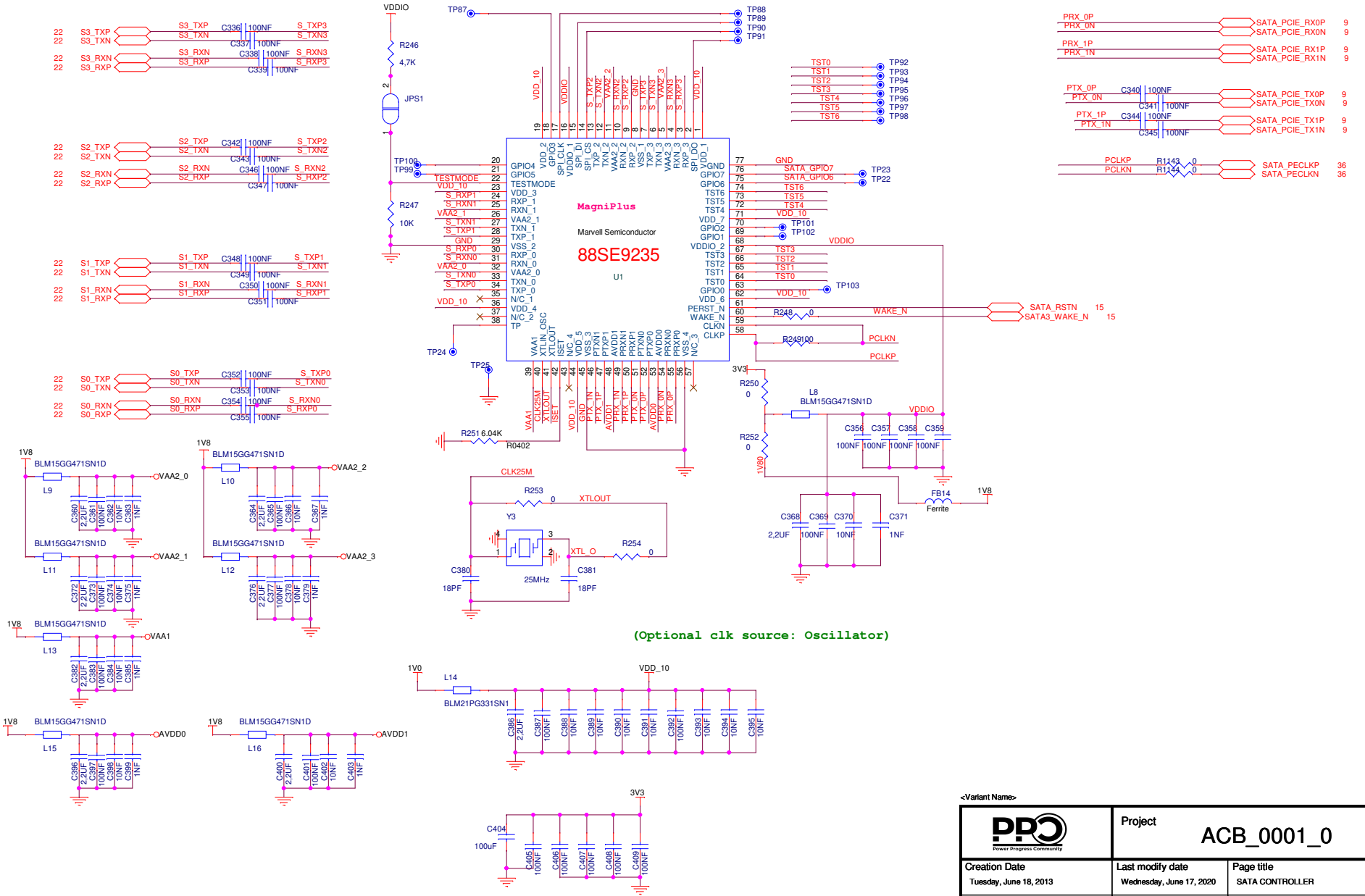
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 20 of 44 / REV. 0	Format A4

MagniPlus -SATA Interface



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Project: ACB_0001_0		
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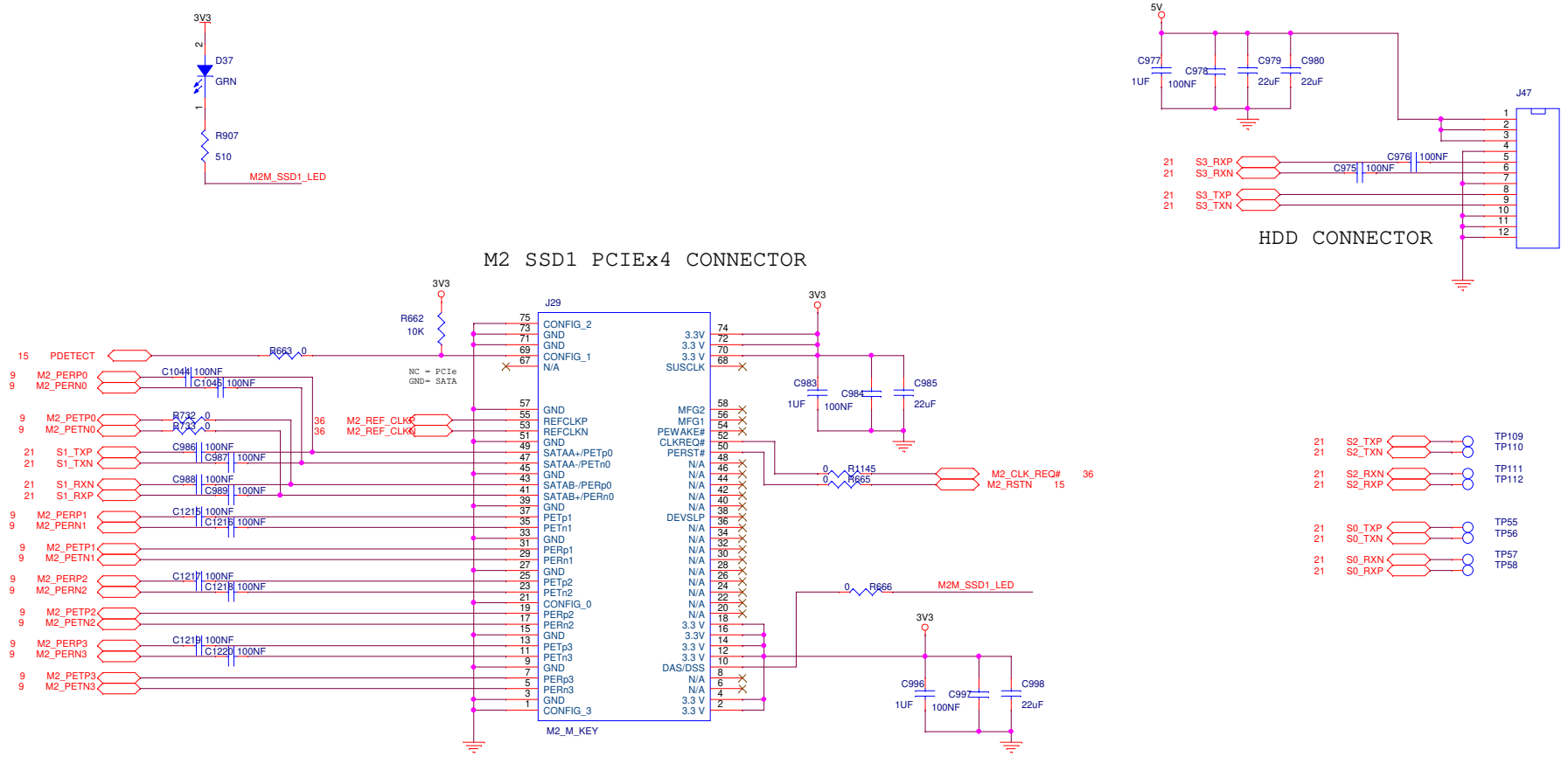
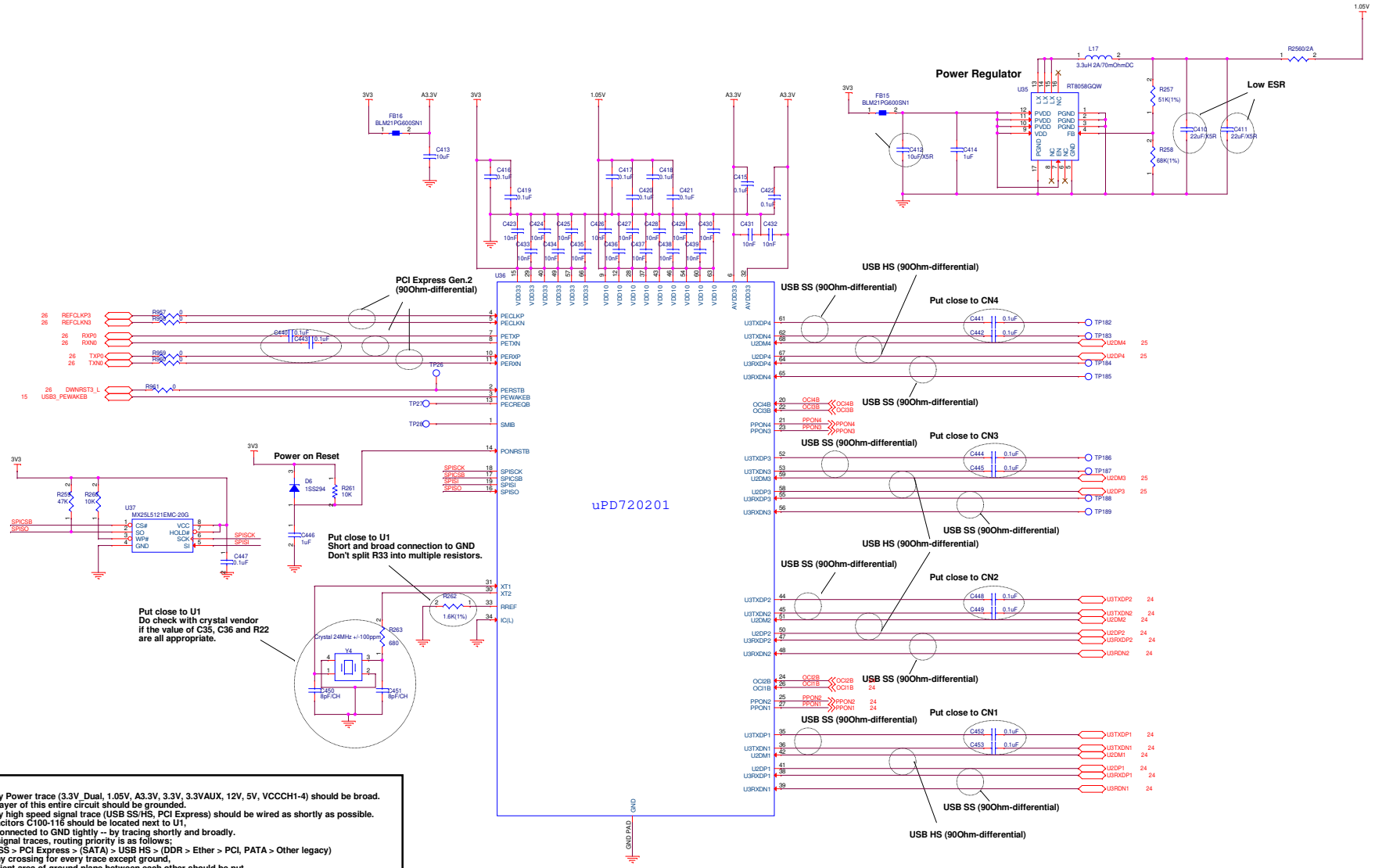
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 21 of 44 / REV. 0 / Format A3



<Variant Name>

PRO Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, November 30, 2018	Last modify date: Wednesday, June 17, 2020	Page title: SATA CONNECTOR		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 22 of 44	REV. 0	Format A3

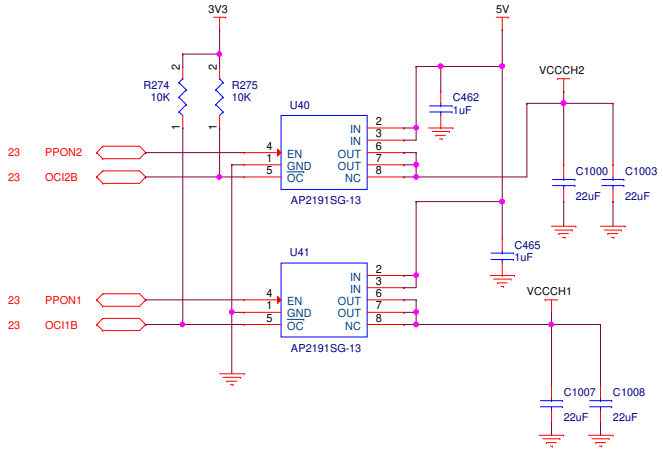


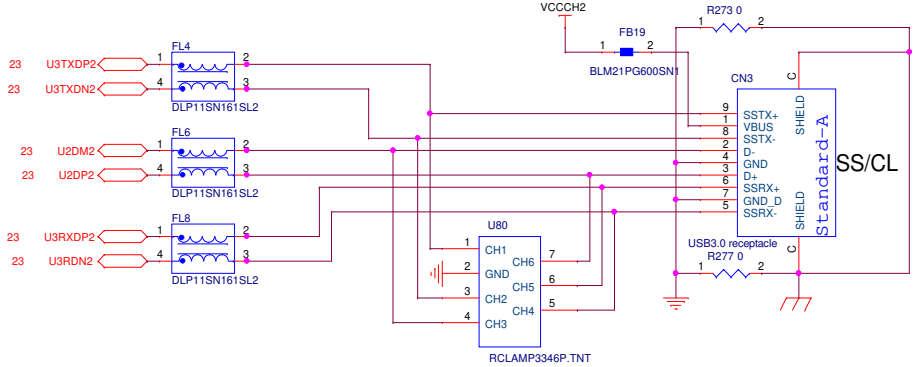
Note:

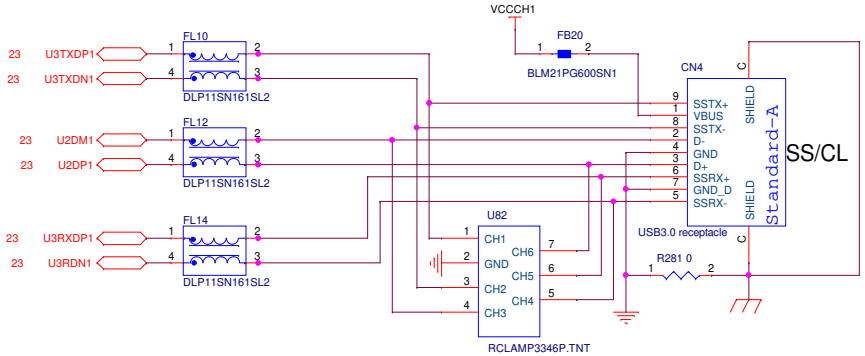
1. Every Power trace (3.3V_Dual, 1.05V, A3.3V, 3.3V, 3.3VAUX, 12V, 5V, VCCCH1-4) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express) should be wired as shortly as possible.
4. Capacitors C100-116 should be located next to U1,
   and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
   USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground,
   sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
   > Remove any impairment or discontinuity.
   > Keep same length by each other.
   > Keep same width and spacing.
8. The differential impedance of nominal value is as follows.
   > USB 3.0 / 2.0 --- 90ohm
   > PCI express Gen 1.(2.5GT/s) --- 100ohm PCI express Gen 2.(5GT/s) --- 85ohm
   PCB trace impedance would be a non-continues value by its design rules.
   The differential impedance adopt the nearest value that can be manufactured at PCB
   For more information please refer to 'USB3.0 Board Design Guide' in design kit.

<Variant Name>

PPO Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: USB3 CONTROLLER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 23 of 44 / REV. 0 / Format A2

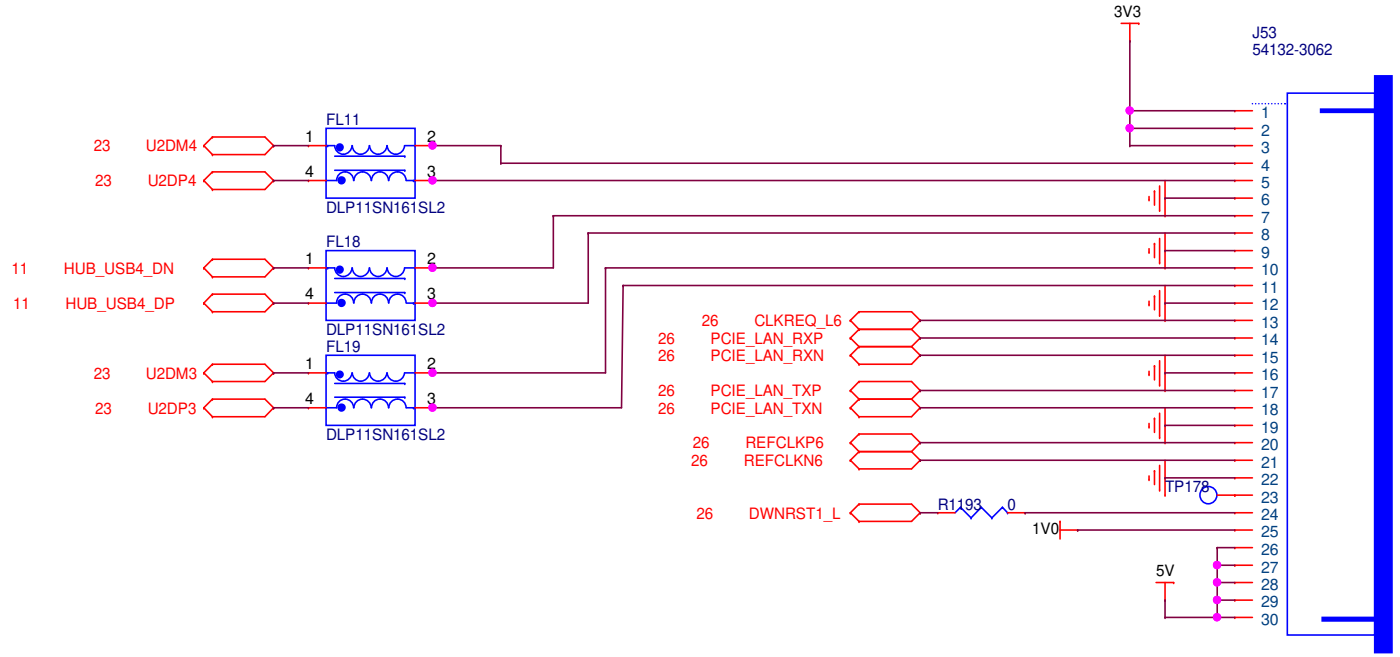






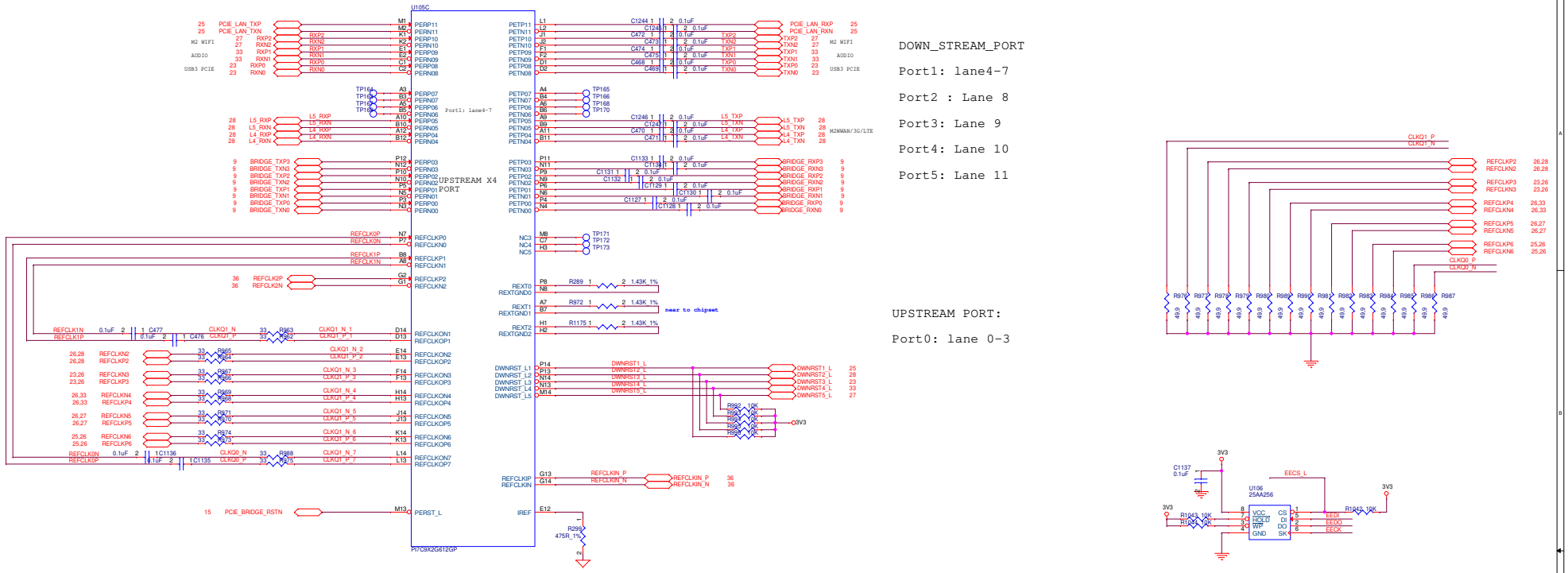
<Variant Name>

Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: USB3 PORTS
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 24of 44 / REV. 0 / Format A3



<Variant Name>

PPC Power Progress Community	Project ACB_0001_0			
Creation Date Wednesday, June 17, 2020	Last modify date	Page title ETHERNET_CARD		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 25 of 44	REV. 0	Format A4



DOWN_STREAM_PORT

Port1: lane4-7

Port2 : Lane 8

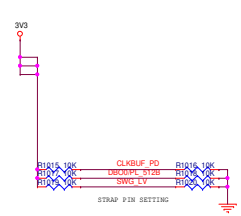
Port3: Lane 9

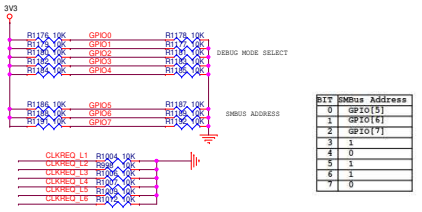
Port4: Lane 10

Port5: Lane 11

UPSTREAM PORT:

Port0: lane 0-3



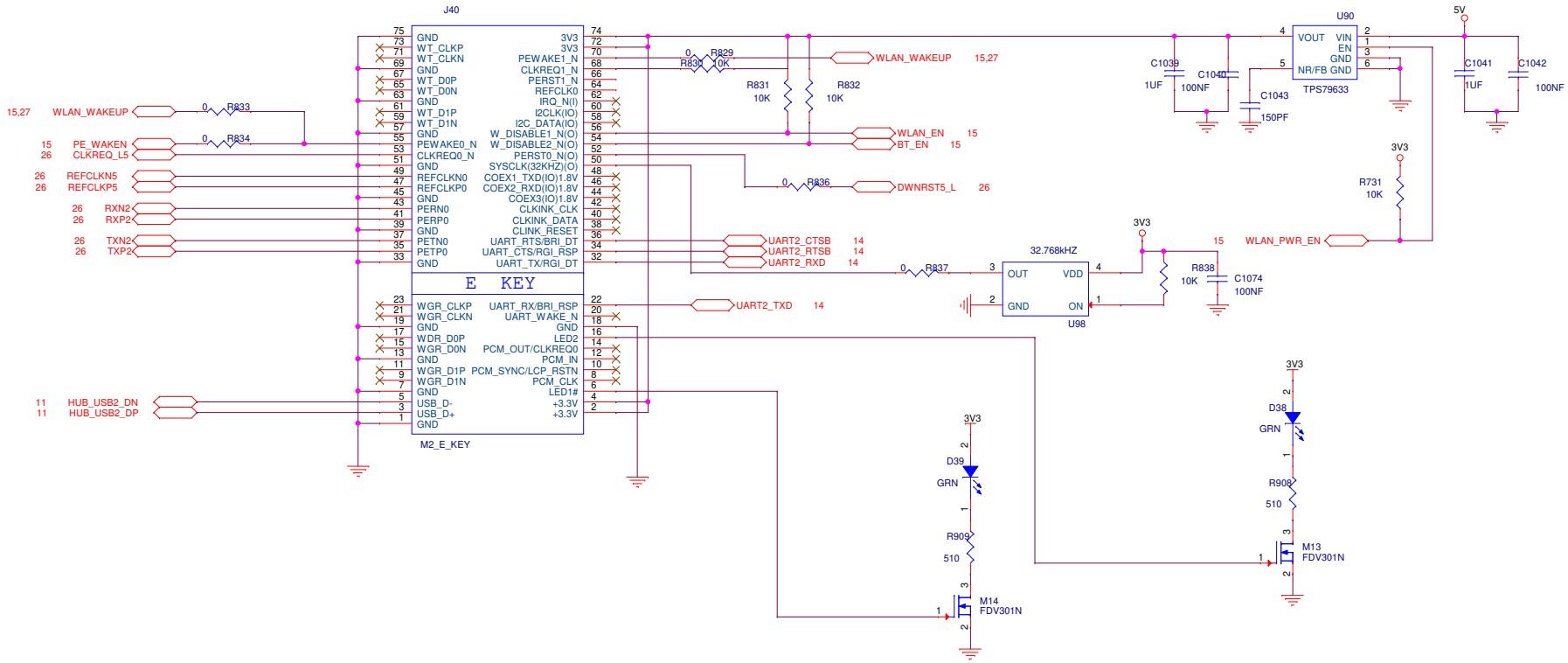


BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	0
5	1
6	1
7	0

<Variant Name>

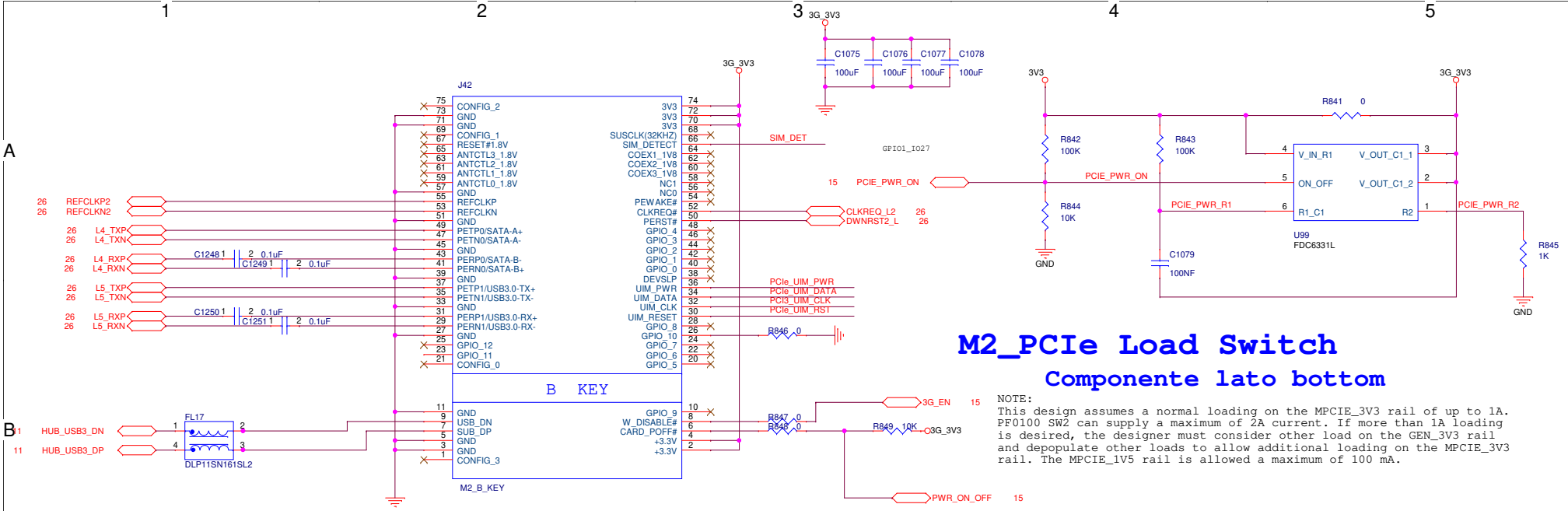
Project: ACB_0001_0		
Creation Date: Tuesday, June 25, 2013	Last modify date: Wednesday, June 17, 2020	Page title: PCIE BRIDGE
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 26 of 44 / REV. 0 / Format A2

M2 WLAN+BT PCIEx1 CONNECTOR



<Variant Name>

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, December 28, 2018	Last modify date: Wednesday, June 17, 2020	Page title: M2.WLAN CONNECTOR		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 27 of 44	REV. 0	Format A3

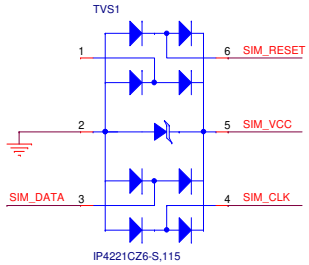


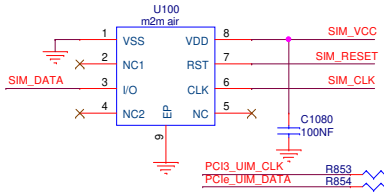
M2_PCIe Load Switch

Componente lato bottom

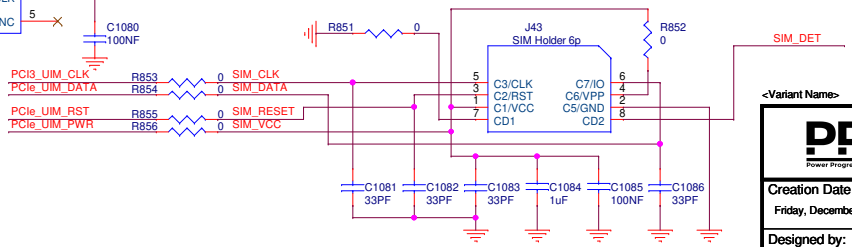
NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.

SIM ON CHIP



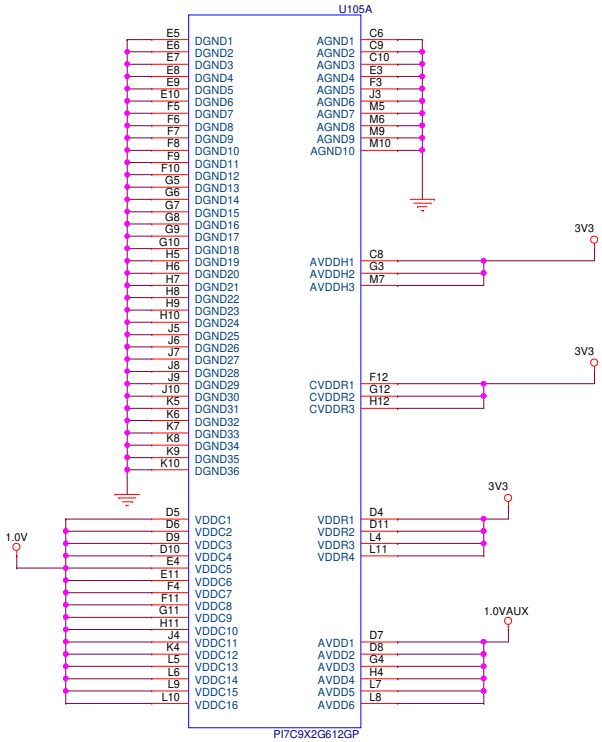


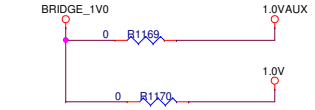
SIM HOLDER

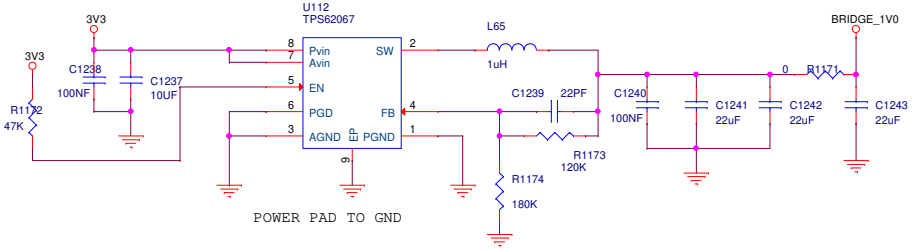


<Variant Name>

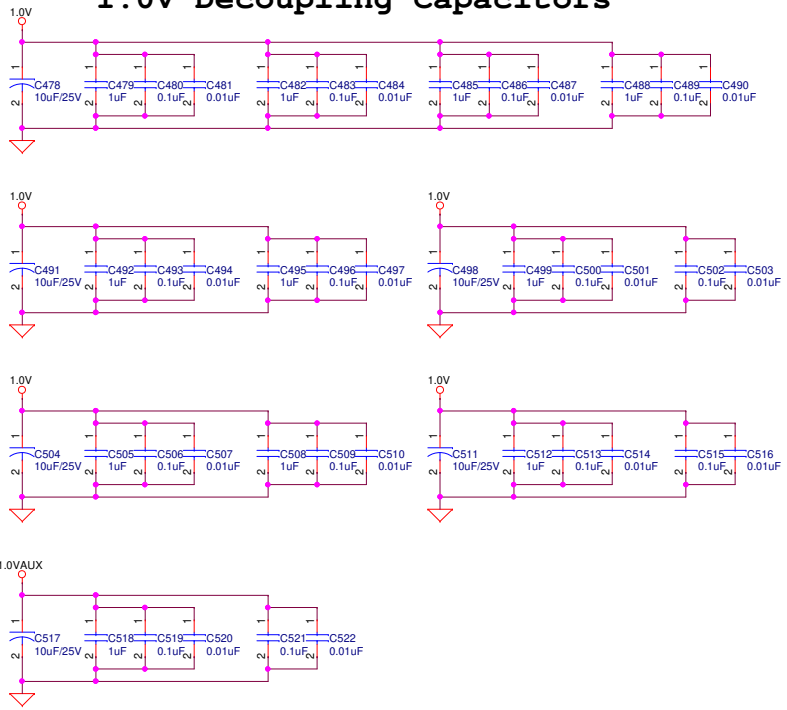
Project: ACB_0001_0		
Creation Date: Friday, December 28, 2018	Last modify date: Wednesday, June 17, 2020	Page title: 3G/LTE MODEM
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 28 of 44 / REV. 0 / Format A3



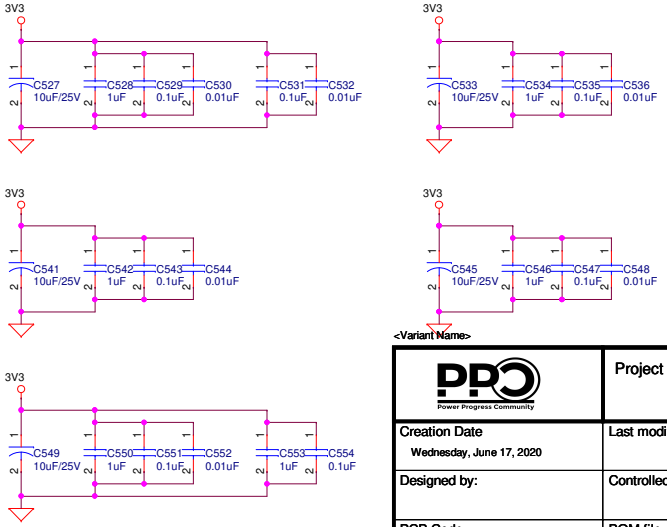




1.0V Decoupling Capacitors

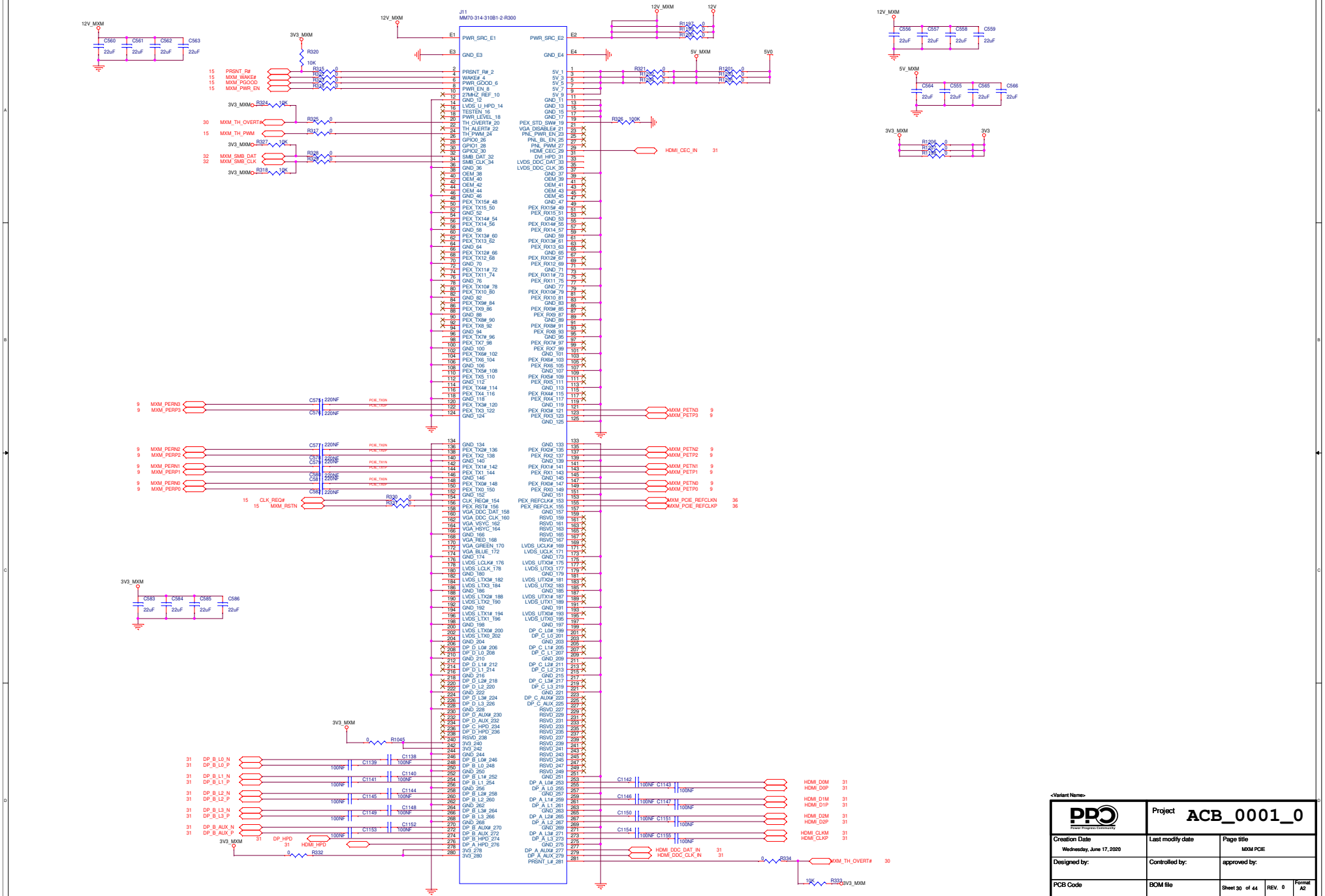


3.3V Decoupling Capacitors



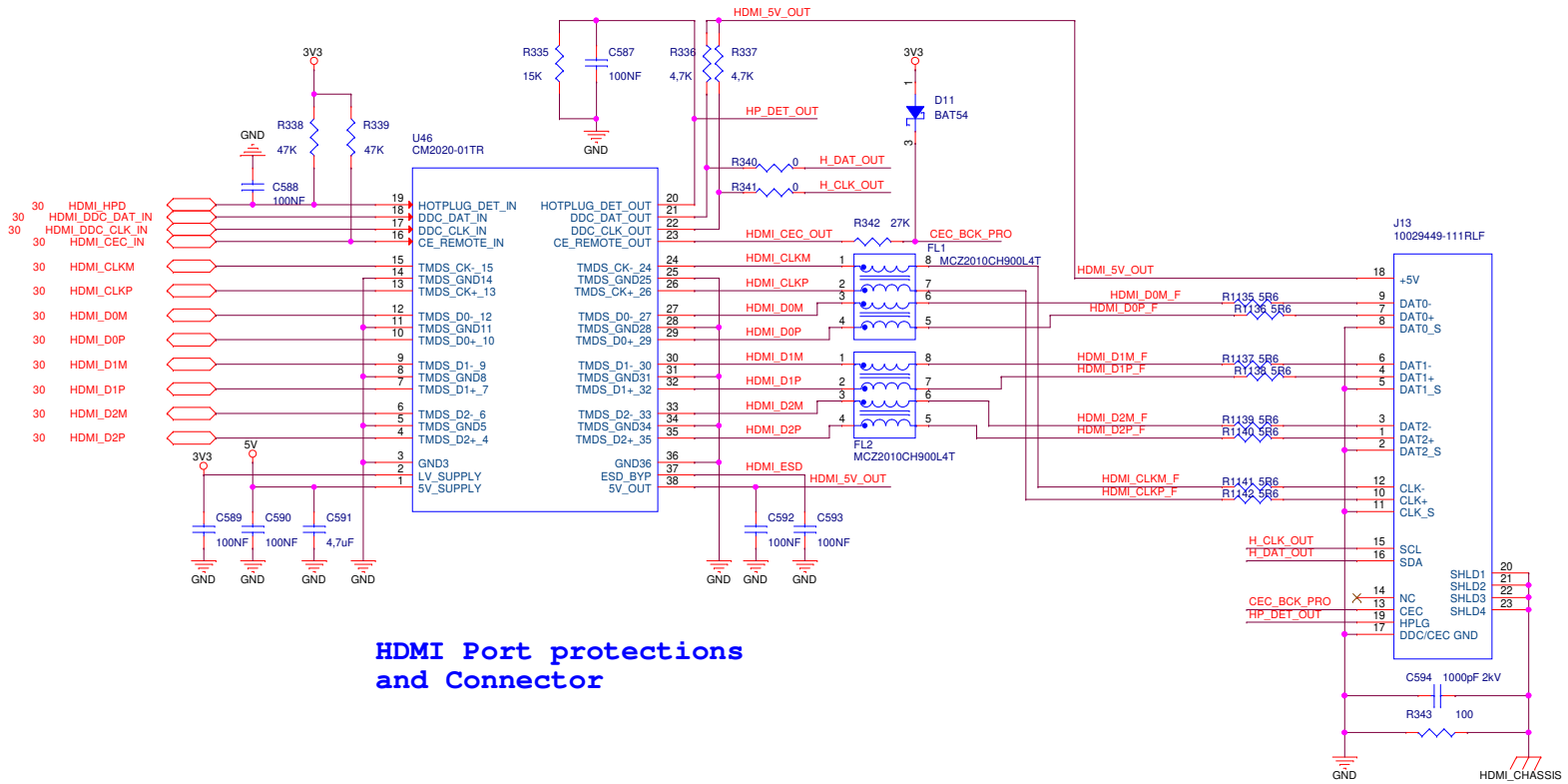
<Variant Name>

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: PCIE BRIDGE POWER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 29 of 44 / REV. 0 / Format A3

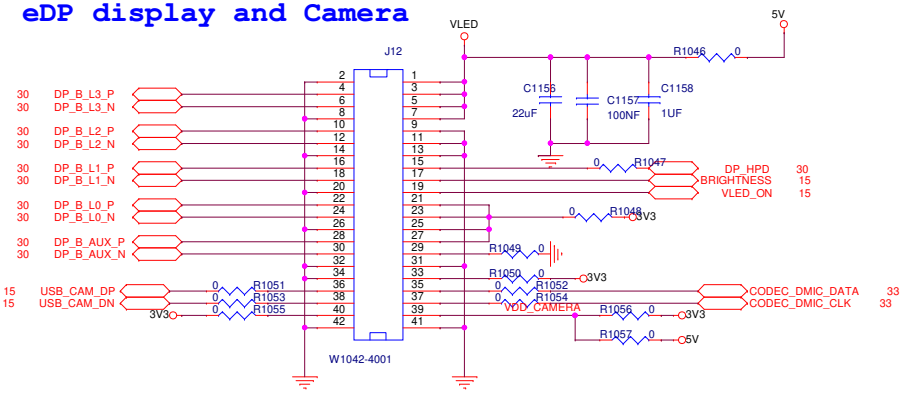


<Variant Name>

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: MXM PCIE
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 30 of 44 / REV. 0 / Format A2



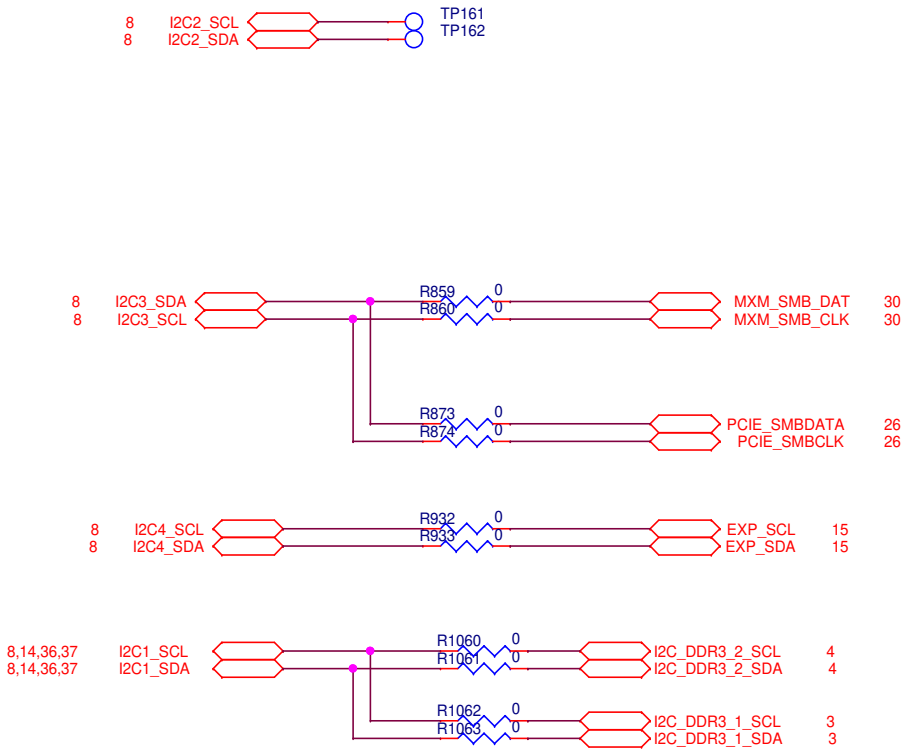
HDMI Port protections and Connector



eDP display and Camera

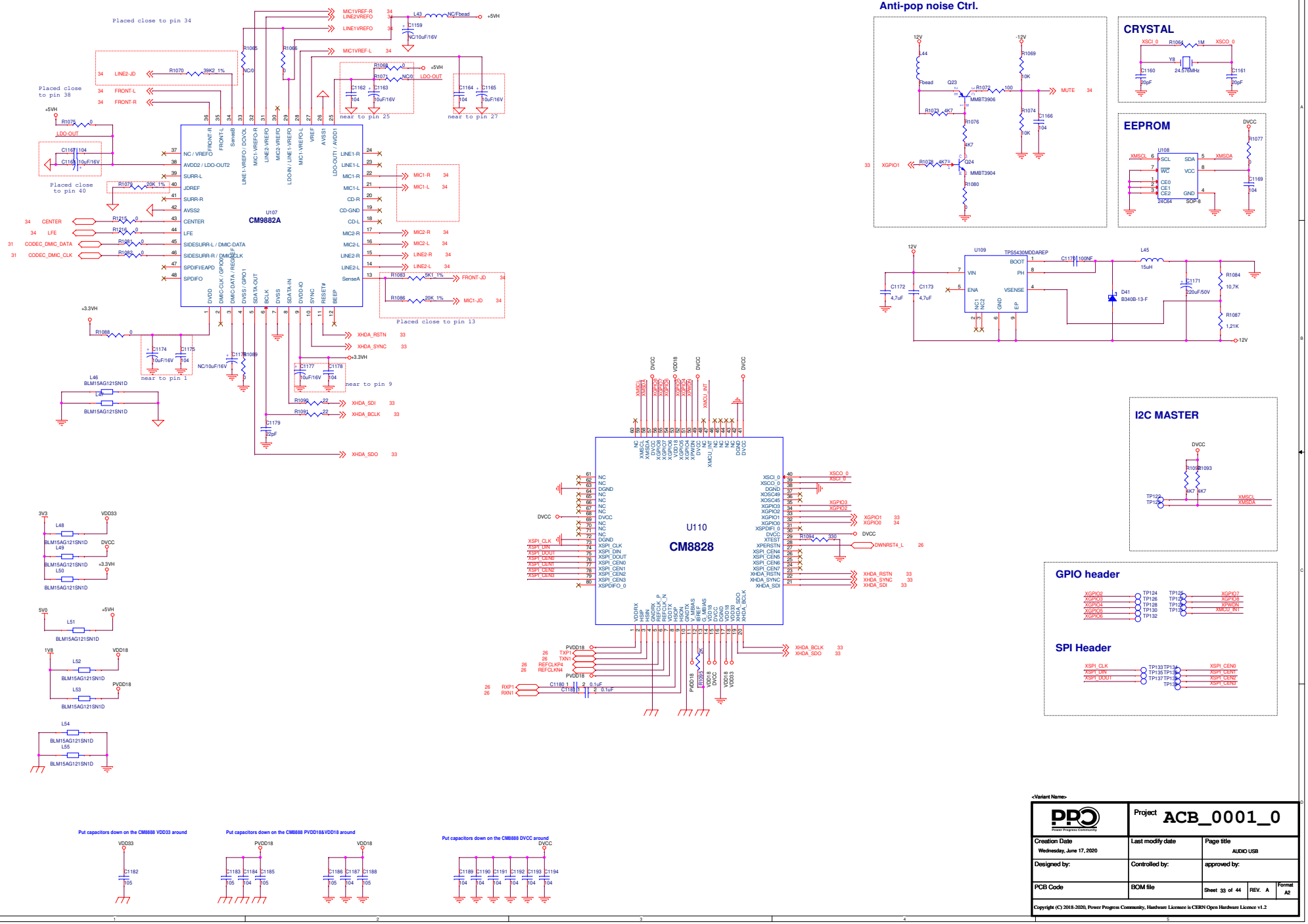
<variant_name>

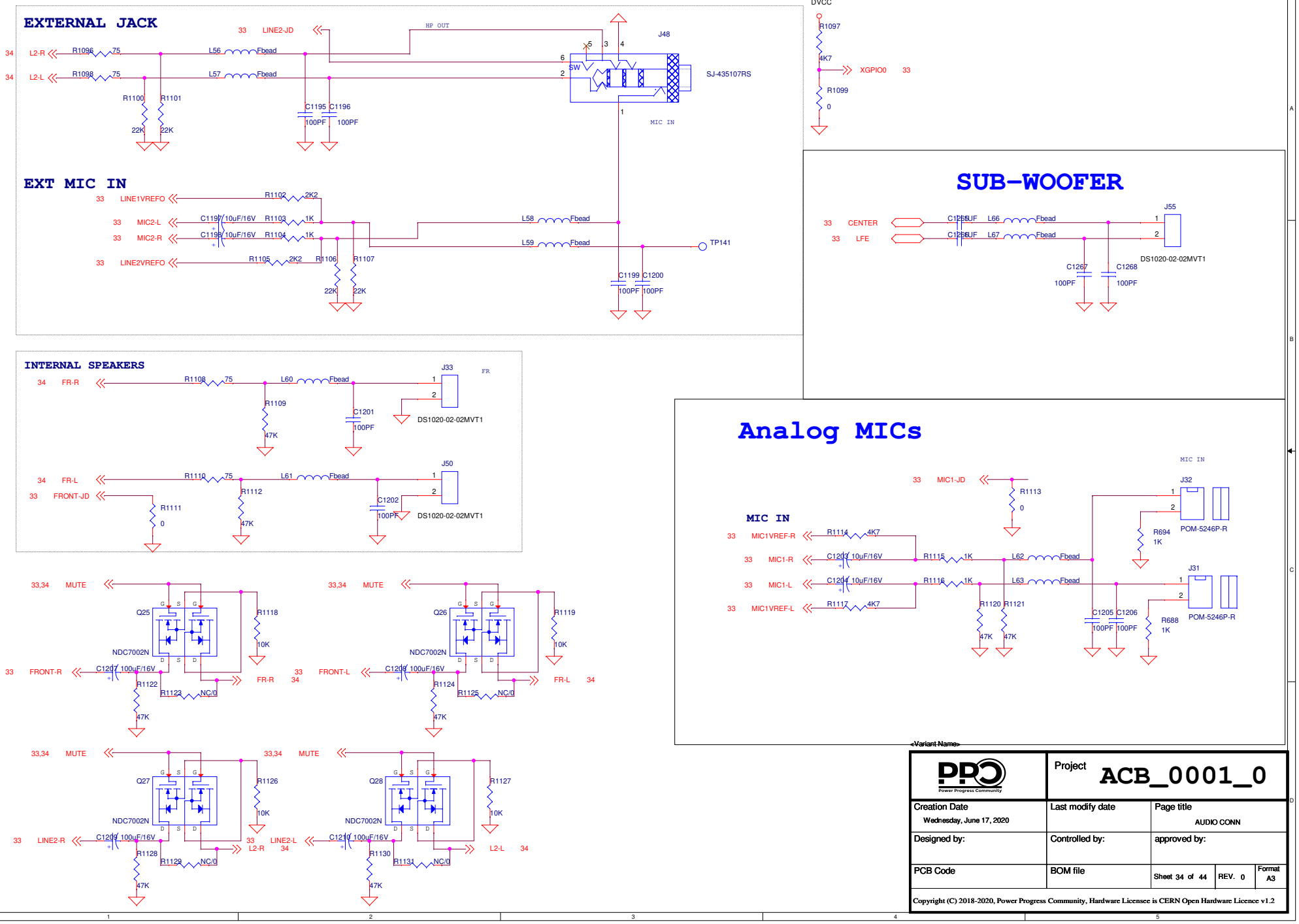
Project ACB_0001_0		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: MXM VIDEO OUT
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 31 of 44 / REV. A / Format A3



<Variant Name>

PPC Power Progress Community	Project			
Creation Date Wednesday, June 17, 2020	Last modify date	Page title I2C WRAP		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 32 of 44	REV. 0	Format A4

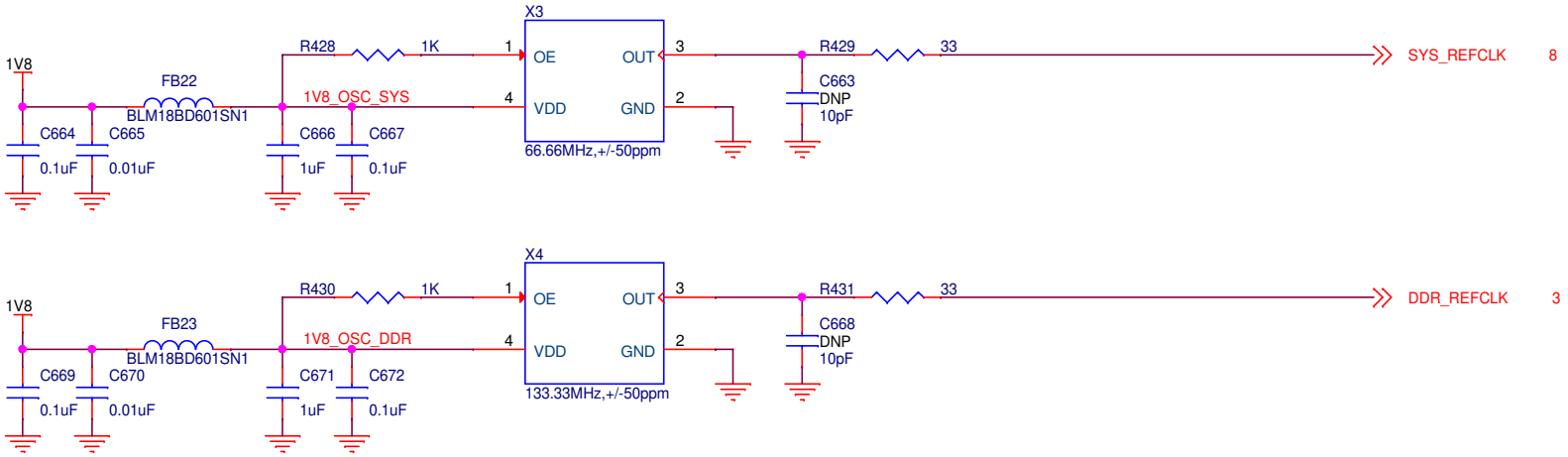

Anti-pop noise Ctrl.
CRYSTAL
EEPROM
I2C MASTER
GPIO header
SPI Header
U107
CM9882A
U110
CM8828
U109
TPS5430MDDAREP
U108
24C64
Placed close to pin 34
Placed close to pin 38
Placed close to pin 40
Placed close to pin 13
near to pin 25
near to pin 27
near to pin 1
near to pin 9
Put capacitors down on the CM8888 VDD33 around
Put capacitors down on the CM8888 PVDD18&VDD18 around
Put capacitors down on the CM8888 DVCC around
<Variant Name>
Project ACB_0001_0
Creation Date Wednesday, June 17, 2020
Last modify date
Page title AUDIO USB
Designed by:
Controlled by:
approved by:
PCB Code
BOM file
Sheet 33 of 44
REV. A
Format A2
Copyright (C) 2018-2020, Power Progress Community, Hardware Licensee is CERN Open Hardware Licence v1.2



<Variant Name>

Project ACB_0001_0		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: AUDIO CONN
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 34 of 44 / REV. 0 / Format A3

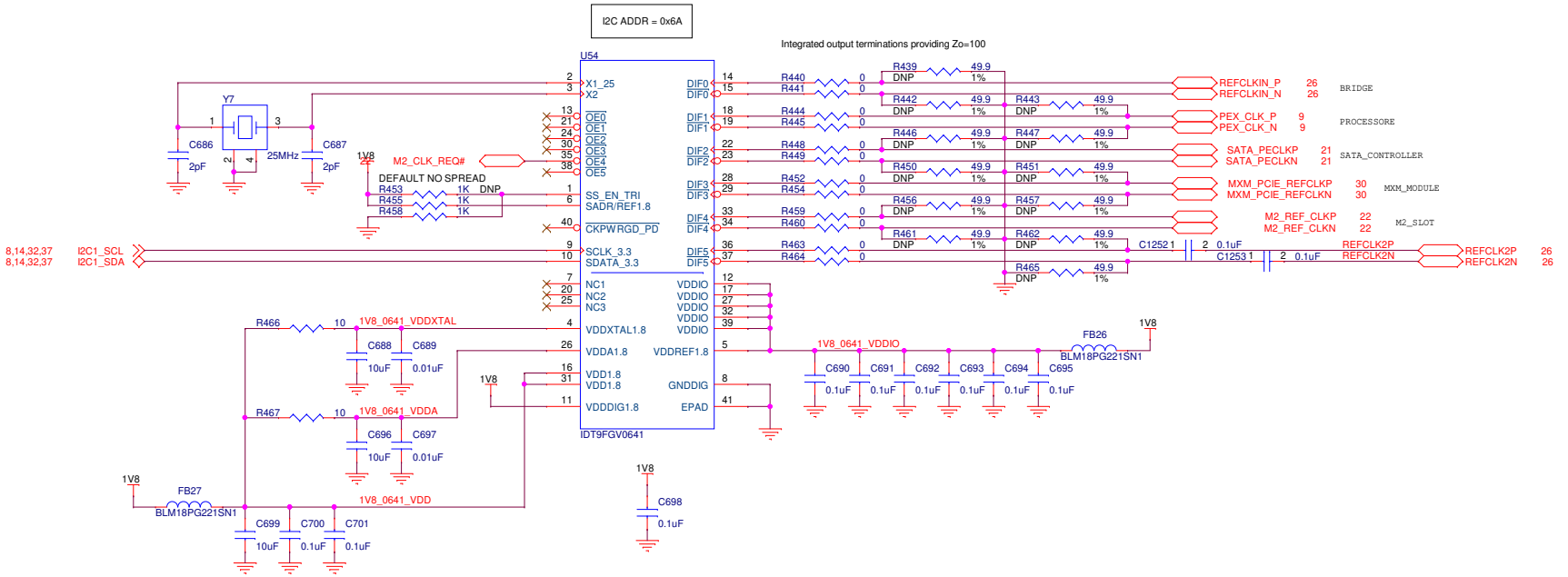
SYSTEM CLOCK GENERATORs



<Variant Name>

PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: CLOCK 1	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 35 of 44 / REV. 0	Format A4

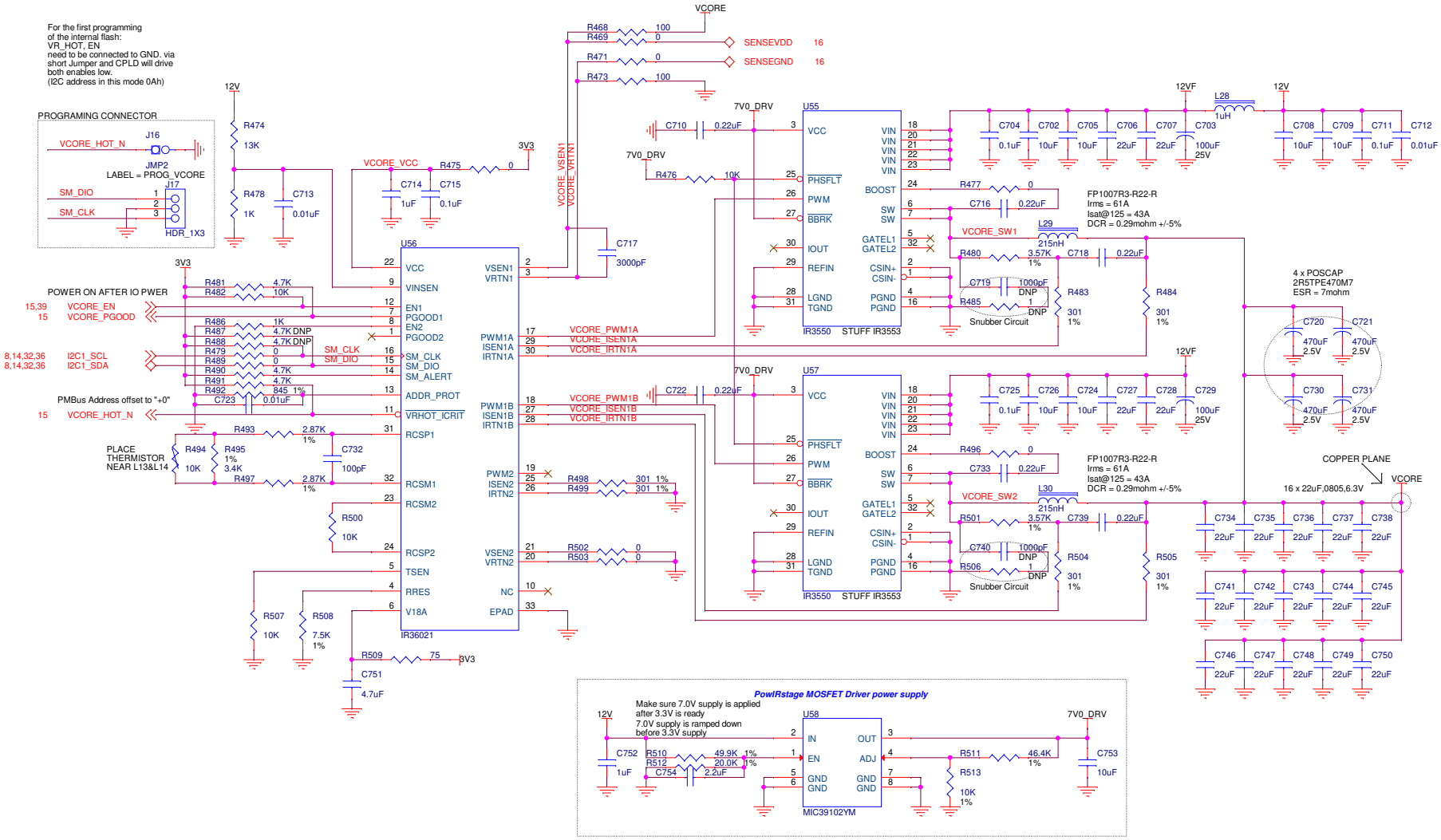
SYSTEM CLOCK GENERATORs (cont.)



<Variant Name>

Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: CLOCK 2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 36 of 44 / REV. 0 / Format A3

T2080 CORE POWER CONVERTOR

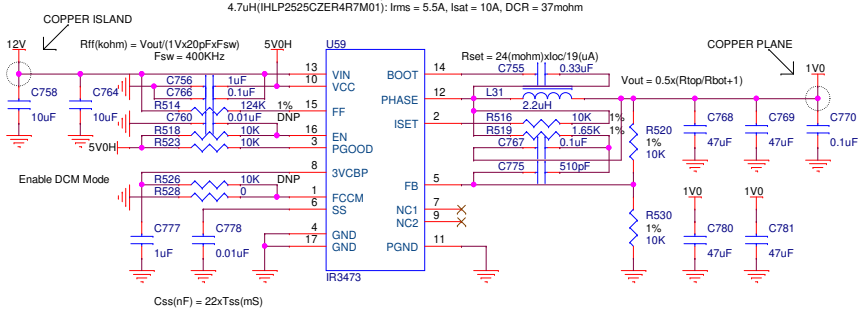


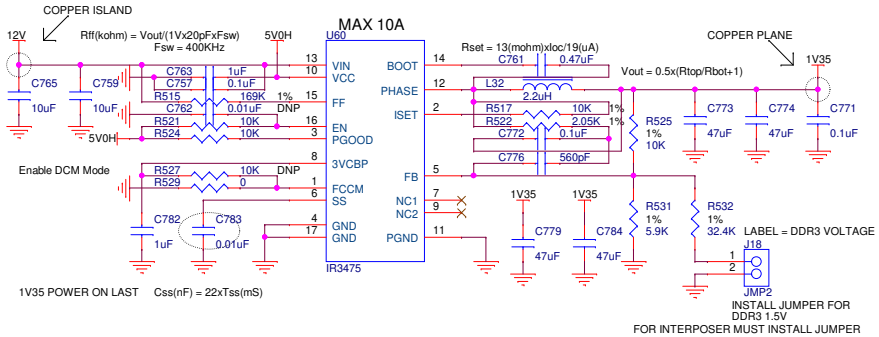
<Variant Name>

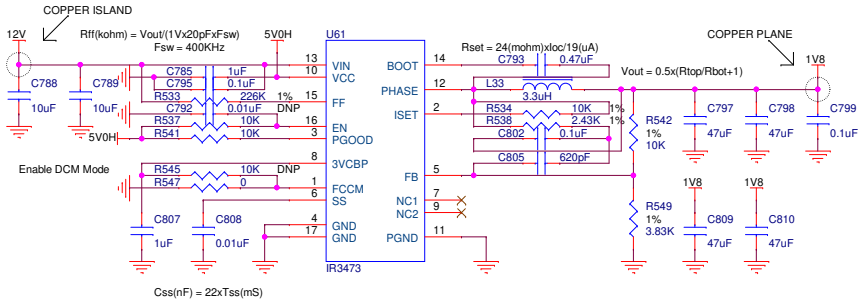
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: CORE PWR
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 37 of 44 / REV. 0 / Format A3

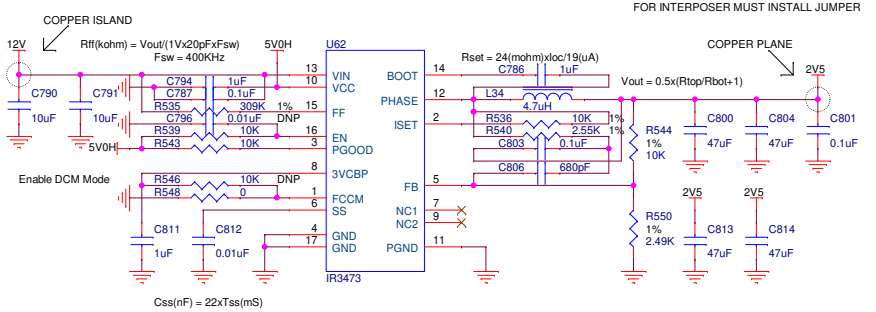
SYSTEM POWER CONVERTORs

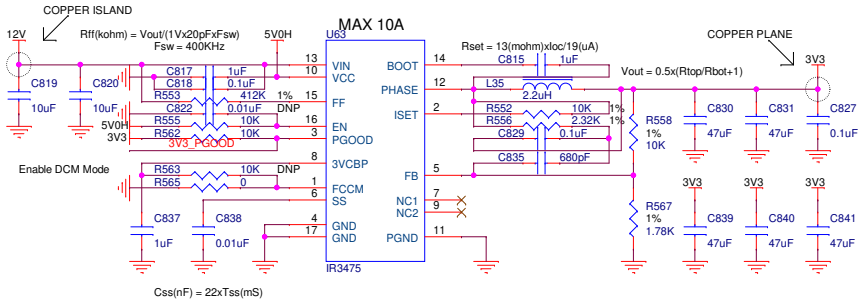
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

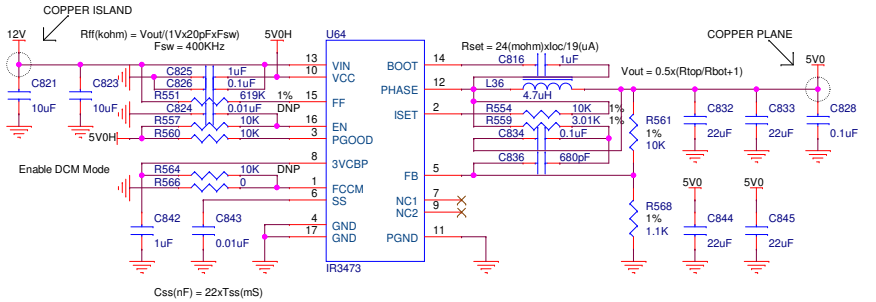




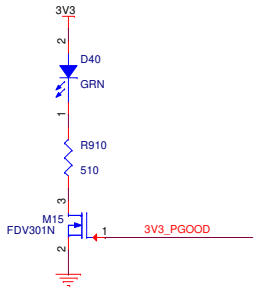








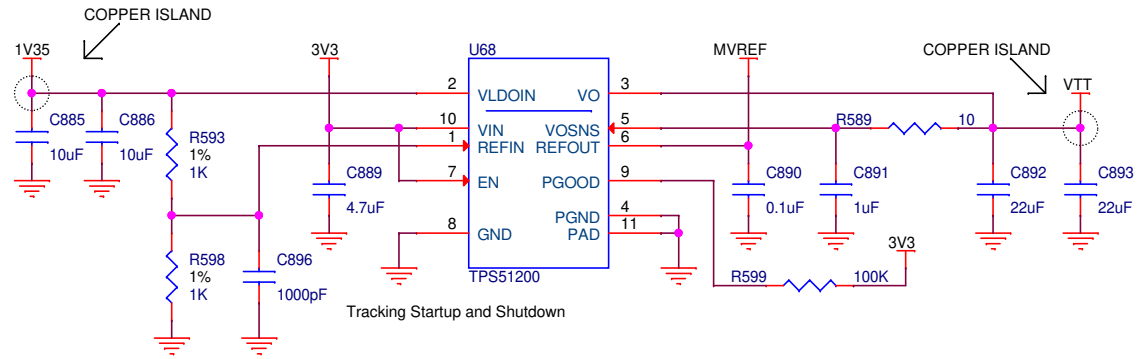
Caution: separate analog and power ground and make connection at GND plane

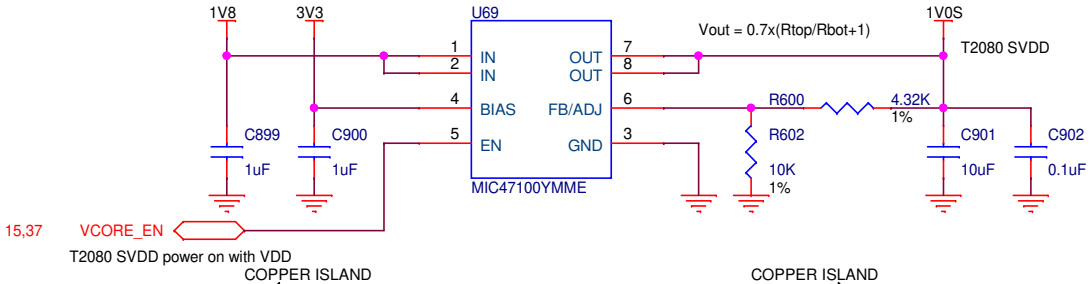


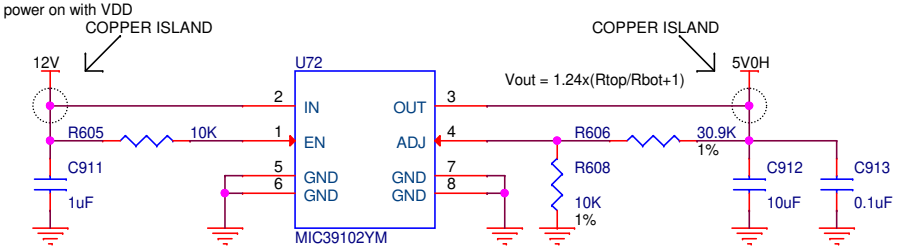
<Variant Name>

Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: OTHER PWR1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 38 of 44 / REV. 0 / Format A3

SYSTEM POWER CONVERTORs (cont.)

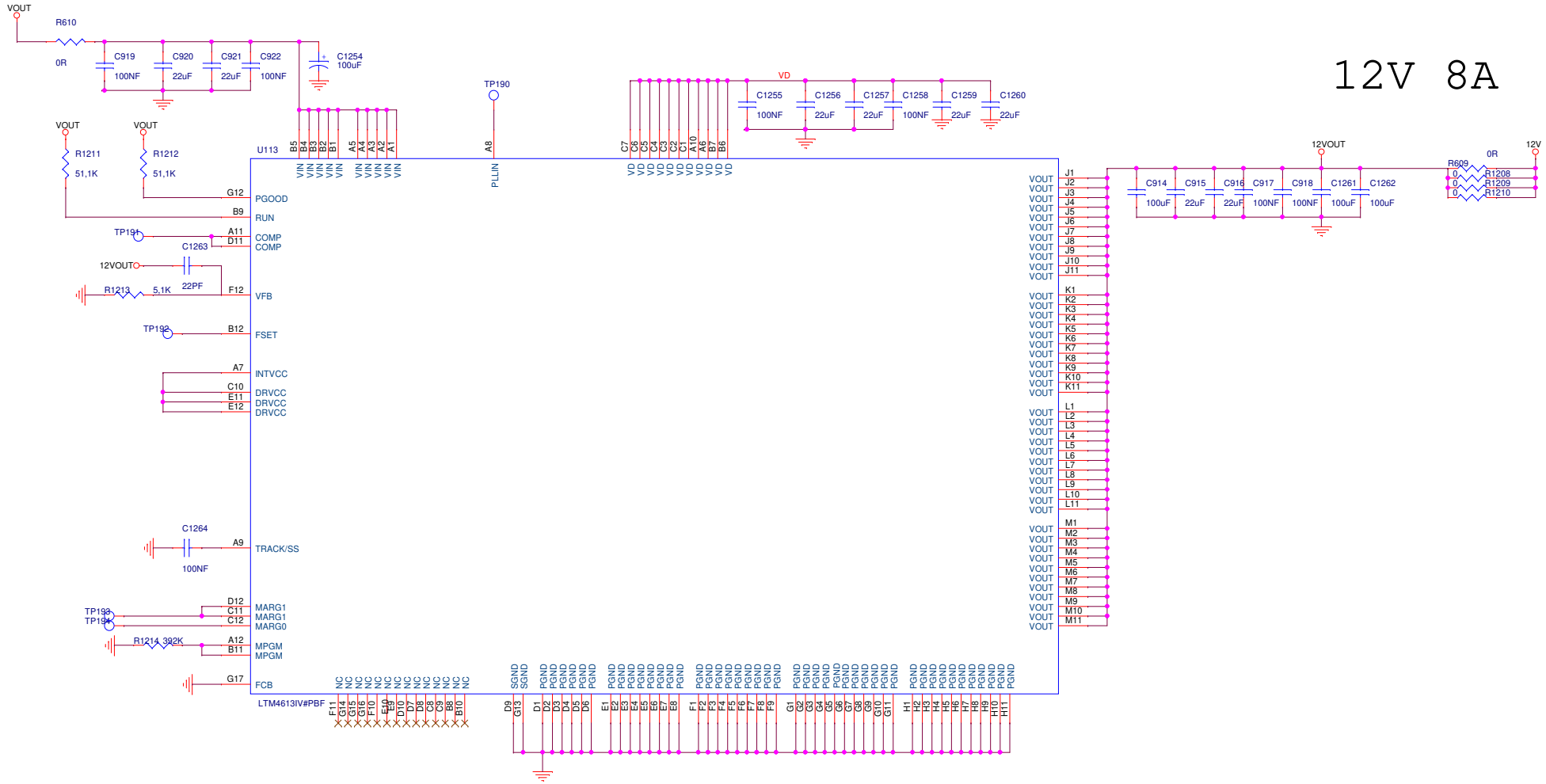






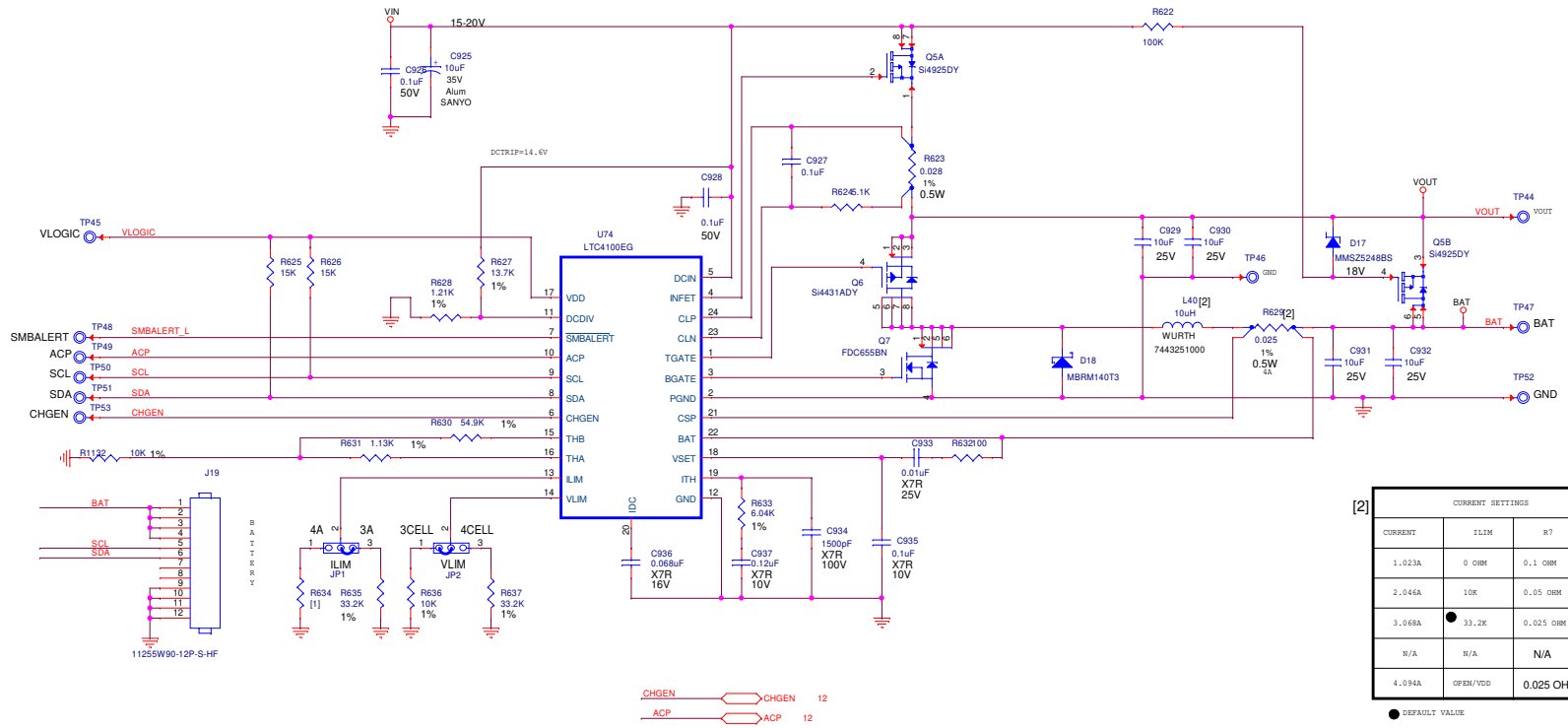
<Variant Name>

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: OTHER PWR2		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 39 of 44	REV. 0	Format A4



<Variant Name>

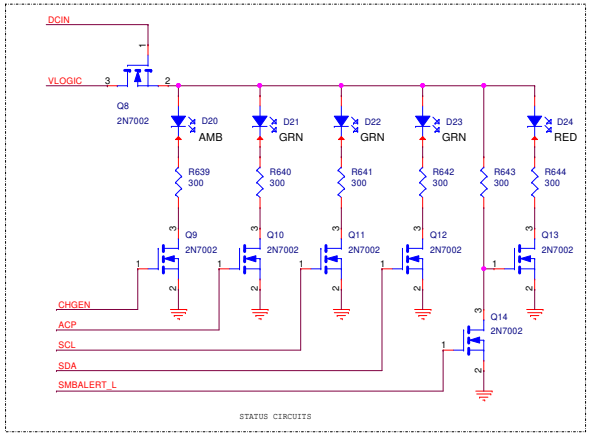
Project **ACB_0001_0**		
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: MAIN POWER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 40 of 44 / REV. 0 / Format A3

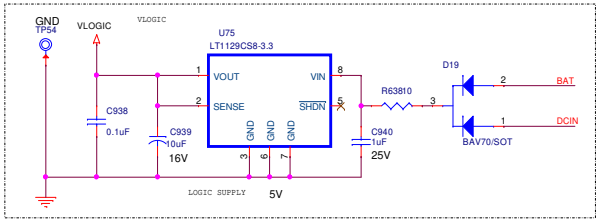


[2]

CURRENT SETTINGS				VOLTAGE SETTINGS	
CURRENT	ILIM	R7	L1	VOLTAGE	VLIM
1.023A	0 OHM	0.1 OHM	40uH	8.438V	0 OHM
2.046A	10K	0.05 OHM	20uH	12.646V	● 10K
3.068A	● 33.2K	0.025 OHM	10uH	16.870V	33.2K
N/A	N/A	N/A	N/A	21.062V	100K
4.094A	OPEN/VDD	0.025 OHM	10uH	32.758V	OPEN/VDD

● DEFAULT VALUE

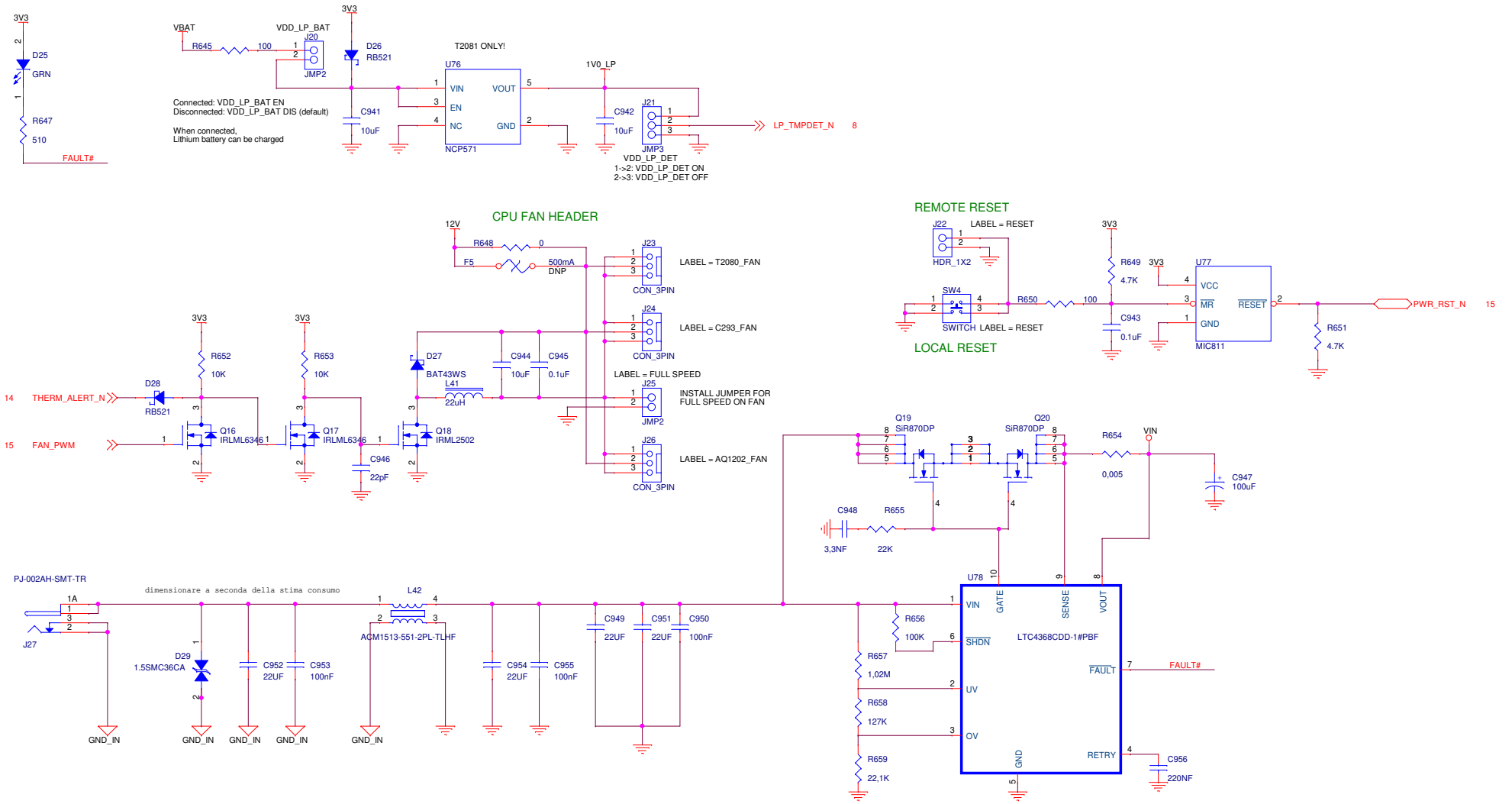




<Variant Name>

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, August 08, 2018	Last modify date: Wednesday, June 17, 2020	Page title: BATTERY CHARGE
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>
PCB Code	BOM file	Sheet 41 of 44 / REV. 0 / Format Custom

SYSTEM POWER INPUT



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PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, June 17, 2020	Last modify date	Page title: PWR IN
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 42 of 44 / REV. 0 / Format A3

<Variant Name>

PPC Power Progress Community	Project **ACB_0001_0**			
Creation Date Wednesday, June 17, 2020	Last modify date	Page title MECANICAL		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet of	REV. 0	Format B

CHANGE LIST

<Variant Name>

PPC Power Progress Community	Project **ACB_0001_0**			
Creation Date Wednesday, June 17, 2020	Last modify date	Page title CHANGE LIST		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 44 of 44	REV. 0	Format B