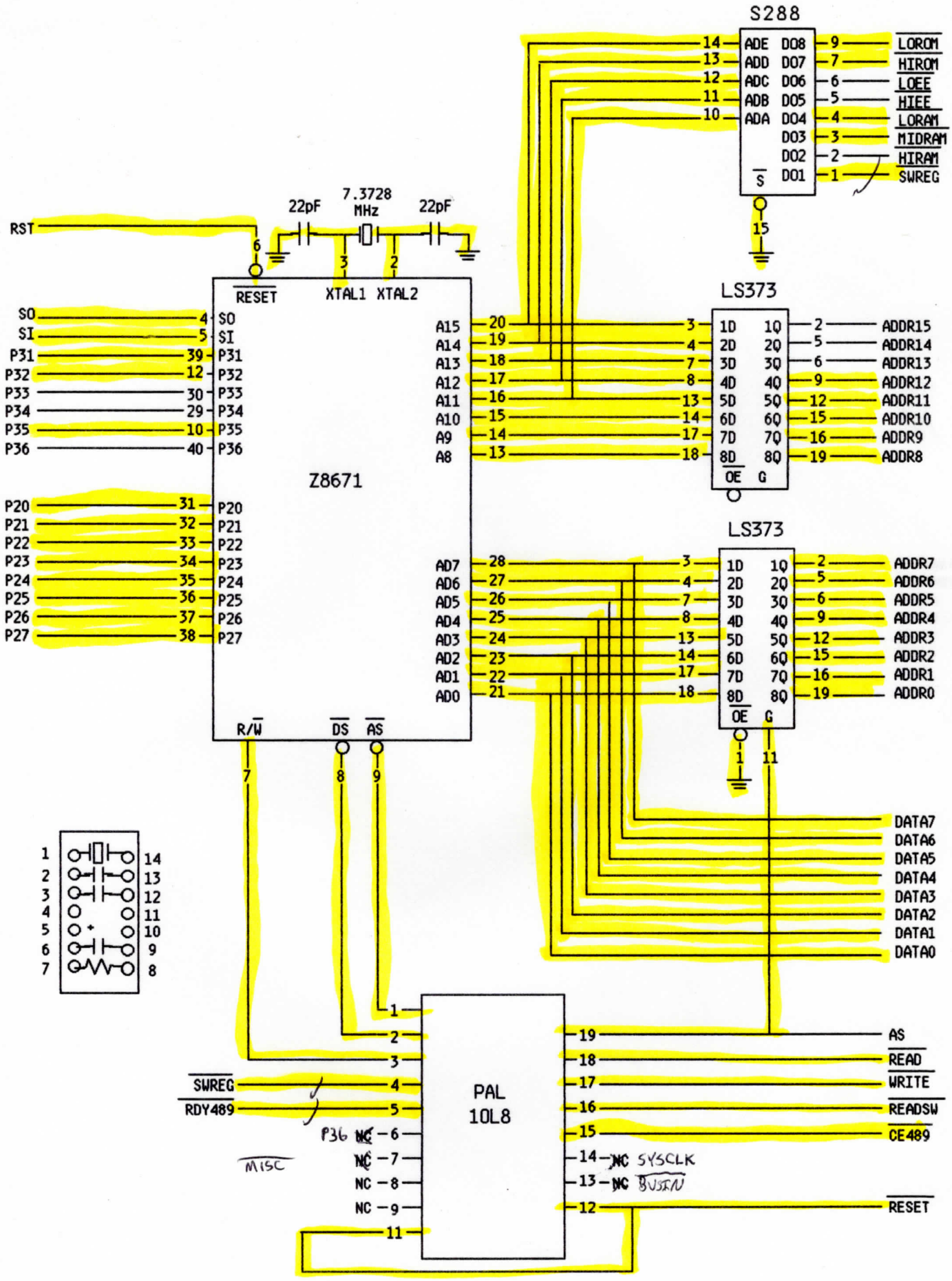
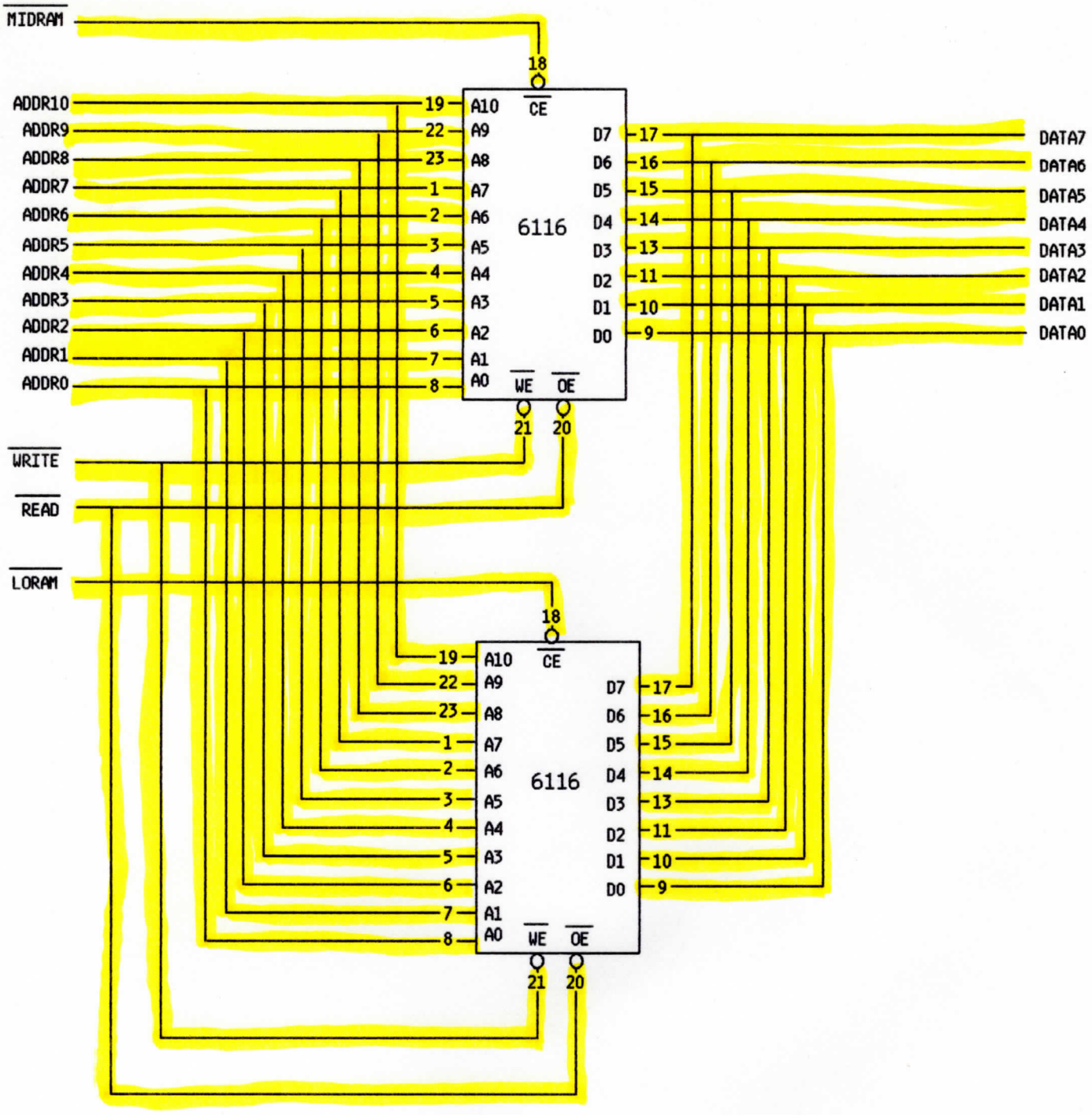
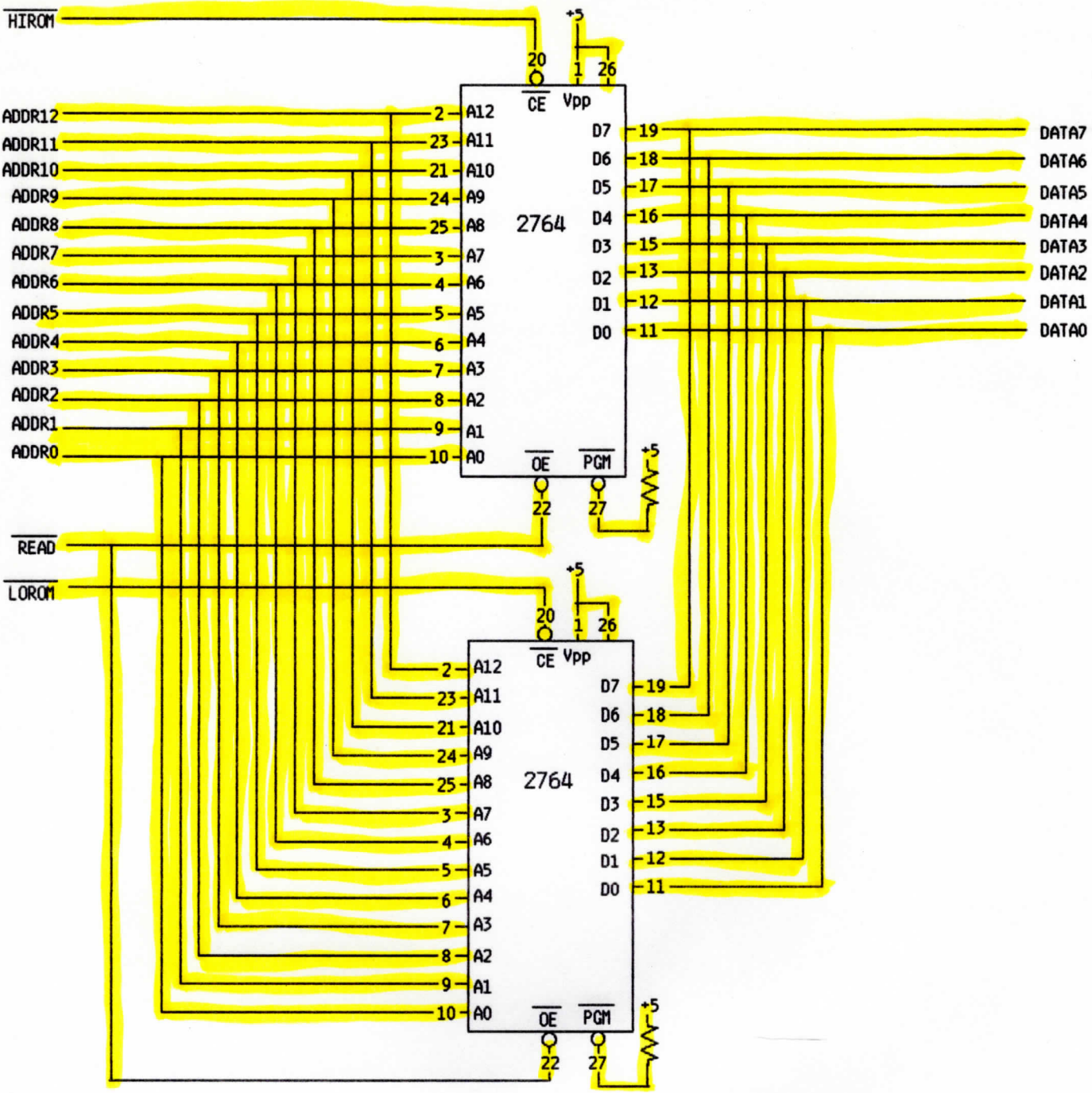
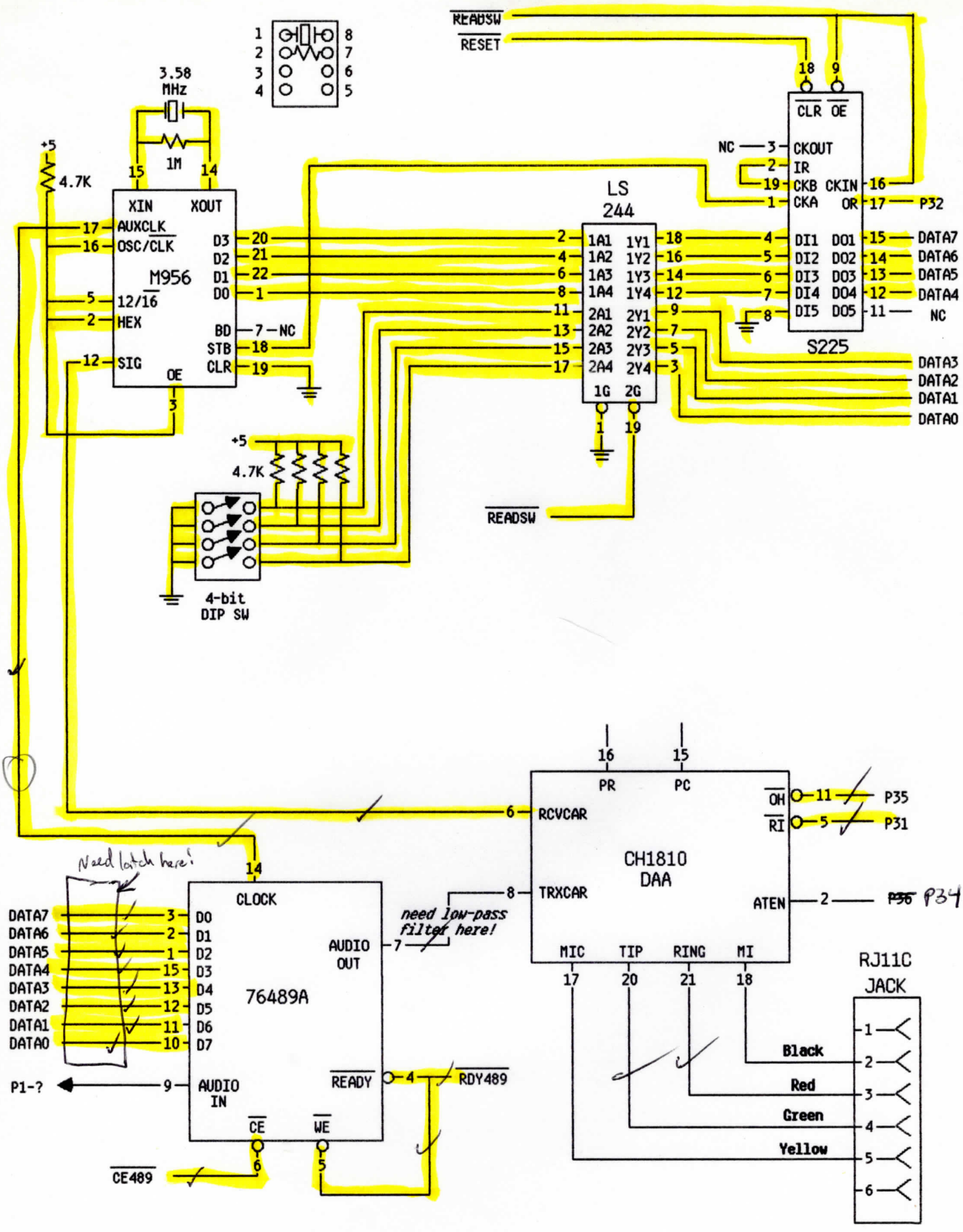
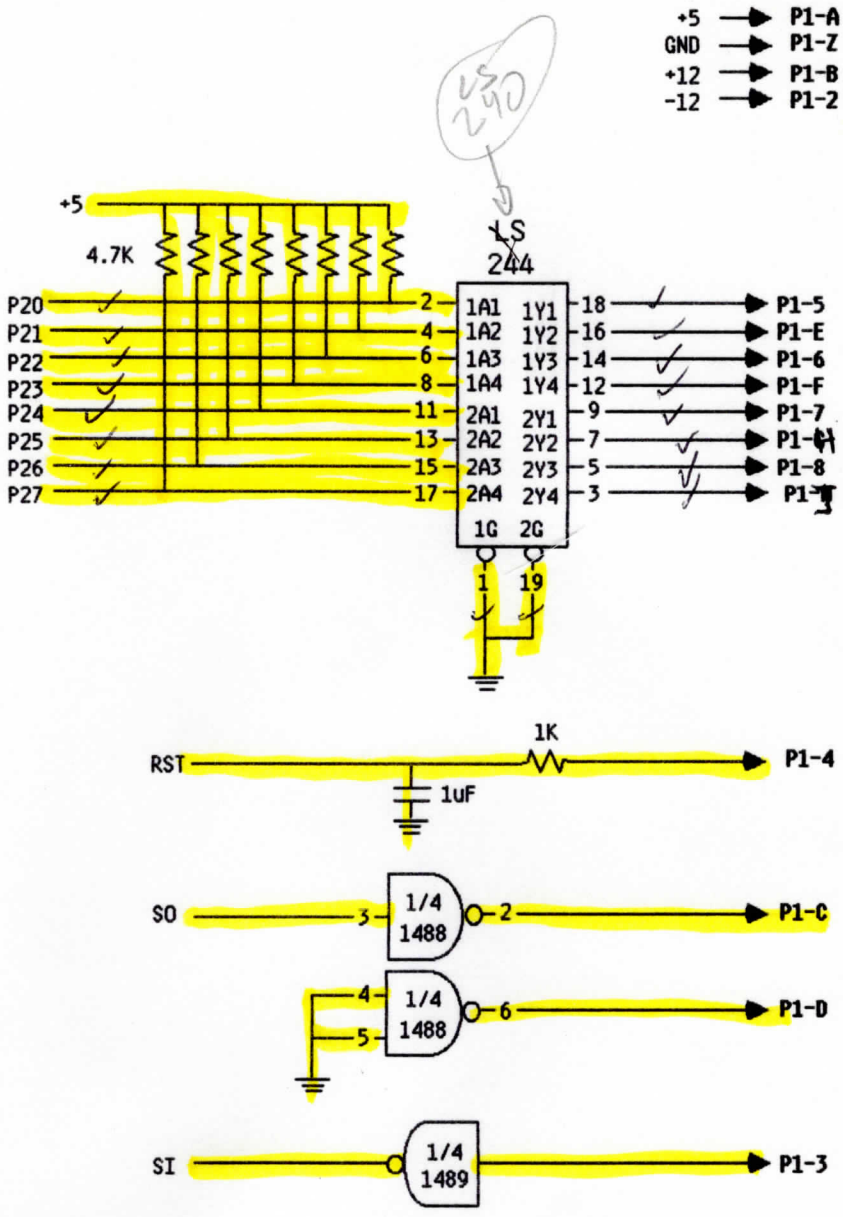

S288
ADE DO8
ADD DO7
ADC DO6
ADB DO5
ADA DO4
DO3
DO2
S DO1
LOROM
HIROM
LOEE
HIEE
LORAM
MIDRAM
HIRAM
SWREG
22pF
7.3728 MHz
22pF
RST
RESET
XTAL1 XTAL2
Z8671
SO
SI
P31
P32
P33
P34
P35
P36
P20
P21
P22
P23
P24
P25
P26
P27
A15
A14
A13
A12
A11
A10
A9
A8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
R/W
DS
AS
LS373
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
7D 7Q
8D 8Q
OE G
ADDR15
ADDR14
ADDR13
ADDR12
ADDR11
ADDR10
ADDR9
ADDR8
LS373
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
ADDR2
ADDR1
ADDR0
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
PAL
10L8
SWREG
RDY489
P36 NC
NC
NC
NC
MISC
AS
READ
WRITE
READSW
CE489
NC SYSCLK
NC BUSIN
RESET


MIDRAM
ADDR10
ADDR9
ADDR8
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
ADDR2
ADDR1
ADDR0
WRITE
READ
LORAM
6116
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CE
WE
OE
D7
D6
D5
D4
D3
D2
D1
D0
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0


HIROM
LOROM
READ
ADDR12
ADDR11
ADDR10
ADDR9
ADDR8
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
ADDR2
ADDR1
ADDR0
+5
20
1
26
CE
Vpp
2764
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
19
18
17
16
15
13
12
11
2
23
21
24
25
3
4
5
6
7
8
9
10
OE
PGM
22
27
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0


READSW
RESET
3.58 MHz
1M
+5
4.7K
XIN
XOUT
AUXCLK
OSC/CLK
M956
12/16
HEX
SIG
OE
D3
D2
D1
D0
BD
STB
CLR
NC
LS 244
1A1 1A2 1A3 1A4
2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4
2Y1 2Y2 2Y3 2Y4
1G 2G
CLR OE
CKOUT
IR
CKB CKIN
CKA OR
DI1 DI2 DI3 DI4 DI5
DO1 DO2 DO3 DO4 DO5
S225
P32
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
4-bit DIP SW
PR
PC
RCVCAR
TRXCAR
OH
RI
ATEN
CH1810 DAA
P35
P31
P34
MIC
TIP
RING
MI
RJ11C JACK
Black
Red
Green
Yellow
Need latch here!
CLOCK
AUDIO OUT
AUDIO IN
READY
CE
WE
76489A
need low-pass filter here!
RDY489
CE489
P1-?


+5 → P1-A
GND → P1-Z
+12 → P1-B
-12 → P1-2
LS 244
+5
4.7K
P20
P21
P22
P23
P24
P25
P26
P27
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
1G 2G
P1-5
P1-E
P1-6
P1-F
P1-7
P1-8
1K
RST
1uF
P1-4
SO
1/4 1488
P1-C
1/4 1488
P1-D
SI
1/4 1489
P1-3

NEW PAL (Random Logic New)

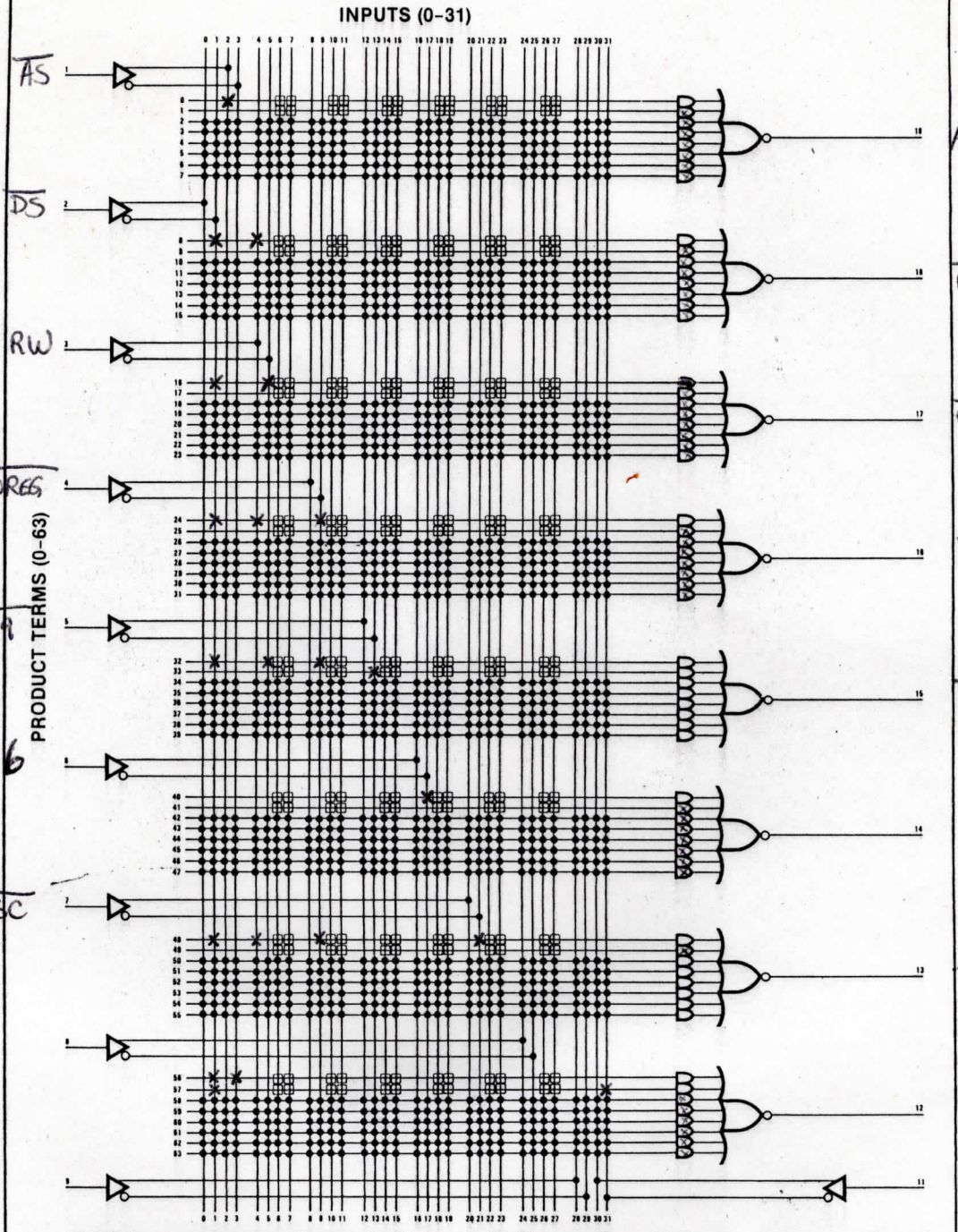


FIGURE 3-42. Logic Diagram, PAL10L8.

Programming Format PAL10L8
PATTERN:
NAME:
PRODUCT TERMS (0–63)
DATE:

95/13

HLLL = 8
HLLH = 9
HLHL = A
HLHH = B
HHLL = C
HHLH = D
HHHL = E
HHHH = F

Programming Format PAL10L8

PATTERN:

NAME: Random Logic New

DATE:

PRODUCT TERMS (0-63)

INPUTS (0-31)

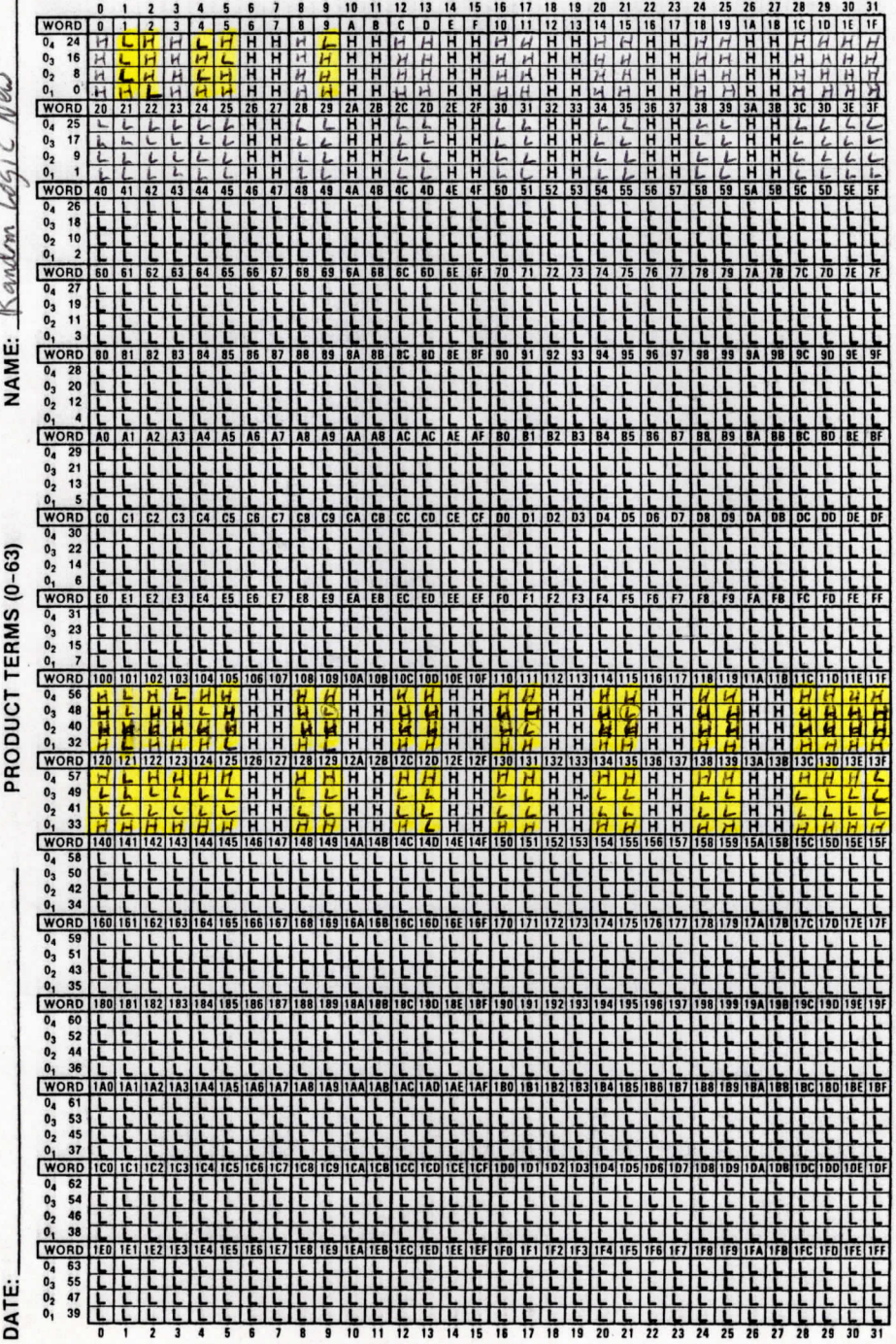


FIGURE 3-43. Programming Format Sheet, PAL10L8.

The 74S288 PROM divides the Z8's 64K address space into 32 2KByte chunks. Each PROM output line is used as a Chip Enable for a different memory chip.

ROM 129 is programmed for 2 4K (e.g. 2732) EPROMs in low memory, 2 2K EEPROMs, 3 2K RAMs, and the baud rate switches. Output lines are assigned as follows:

DO1 (LSB)	Switch Register
DO2	High RAM
DO3	Middle RAM
DO4	Low RAM
DO5	High EEPROM
DO6	Low EEPROM
DO7	High EPROM
DO8 (MSB)	Low EPROM

ROM 129 is programmed as follows:

ROM Loc	Processor locs(hex)	Data
0	0000-07FF	FF
1	0800-0FFF	FF
2	1000-17FF	7F (Low EPROM)
3	1800-1FFF	7F (Low EPROM)
4	2000-27FF	BF (Hi EPROM)
5	2800-2FFF	BF (Hi EPROM)
6	3000-37FF	FF
7	3800-3FFF	FF
8	4000-47FF	FF
9	4800-4FFF	FF
10	5000-57FF	FF
11	5800-5FFF	FF
12	6000-67FF	FF
13	6800-6FFF	FF
14	7000-77FF	DF (Low EEPROM)
15	7800-7FFF	EF (Hi EEPROM)
16	8000-87FF	F7 (Low RAM)
17	8800-8FFF	FB (Mid RAM)
18	9000-97FF	FD (Hi RAM)
19	9800-9FFF	FF
20	A000-A7FF	FF
21	A800-AFFF	FF
22	B000-B7FF	FF
23	B800-BFFF	FF
24	C000-C7FF	FF
25	C800-CFFF	FF
26	D000-D7FF	FF
27	D800-DFFF	FF
28	E000-E7FF	FF
29	E800-EFFF	FF
30	F000-F7FF	FF
31	F800-FFFF	FE (Switch)

1	-NC-	A	+5
2	-12	B	+12
3	SI	C	SO
4	RESET	D	DSR
5	P20	E	P21
6	P22	F	P23
7	P24	G	P25
8	P26	J	P27
9	DATA0	K	DATA1
10	DATA2	L	DATA3
11	DATA4	M	DATA5
12	DATA6	N	DATA7
13	$\overline{\text{READ}}$	P	$\overline{\text{WRITE}}$
14	SYSCLK	R	INTREQ
15	TTYSEL	S	SPCHSEL
16	(RSVD)	T	(RSVD)
17	TIP	U	RING
18	(ADDR6)	V	(ADDR7)
19	~~TIP~~(ADDR4)	W	~~RING~~(ADDR5)
20	ADDR2	X	ADDR3
21	ADDR0	Y	ADDR1
22	-NC-	Z	GND

CPU Board I/O Assignments

LS245 DIR=0 ⇒ B to A
1 ⇒ A to B
so A is CPU side

BUSIN = READ · MISC · $\overline{\text{SWREG}}$

@
RW.DS

VECTOR ELECTRONIC CO., INC.
12460 GLADSTONE AVE.
SYLMAR, CALIF. 91342

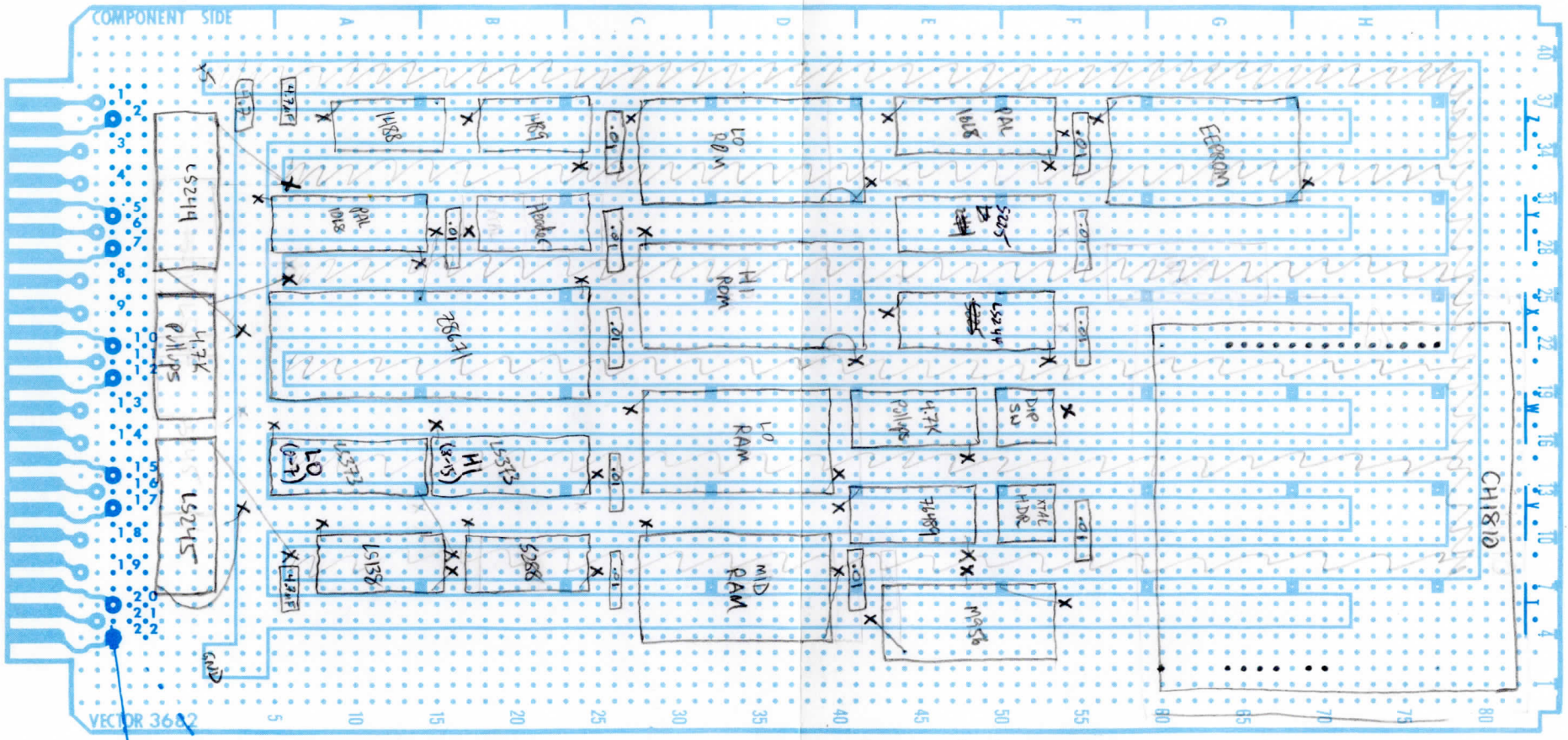
VECTOR D.I.P. PLUGBORD
PATTERN .042" x 0.1" SPACED HOLES
LA3-P7 LAYOUT PAPER Issue 81-05

= No. 1 DIP Position

Zone Letters A,B,C,etc., on Y axis and X, Y, Z on X axis mark position for 14- or 16-pin DIPs

3682 9.6" LONG CARD

COMPONENT SIDE



CAUTION: In any plug contact area on either side of Plugbord, use only those holes having pads. Holes without pads may have insufficient clearance to adjacent circuitry, and using them could cause shorting.

4. To prevent shorting wrapped wire to etched circuit when wire wrapping, use one or more insulated turns at bottom of wrap post; also, do not chisel-cut wire against etched circuit as a shorting burr may occur.

3. Before pressing terminals into board, position (rotate) terminals to maximize the clearance between the widest part of the terminal and the nearest adjacent conductor.

2. Where tin coated circuitry exists, a small percentage of the holes may have solder blockage. This is usually a light "skin" easily penetrated by component leads. In some cases a soldering iron may be required.

1. Intended for use in non-hostile environments up to 200 volts RMS or 300 volts DC.

NOTES: