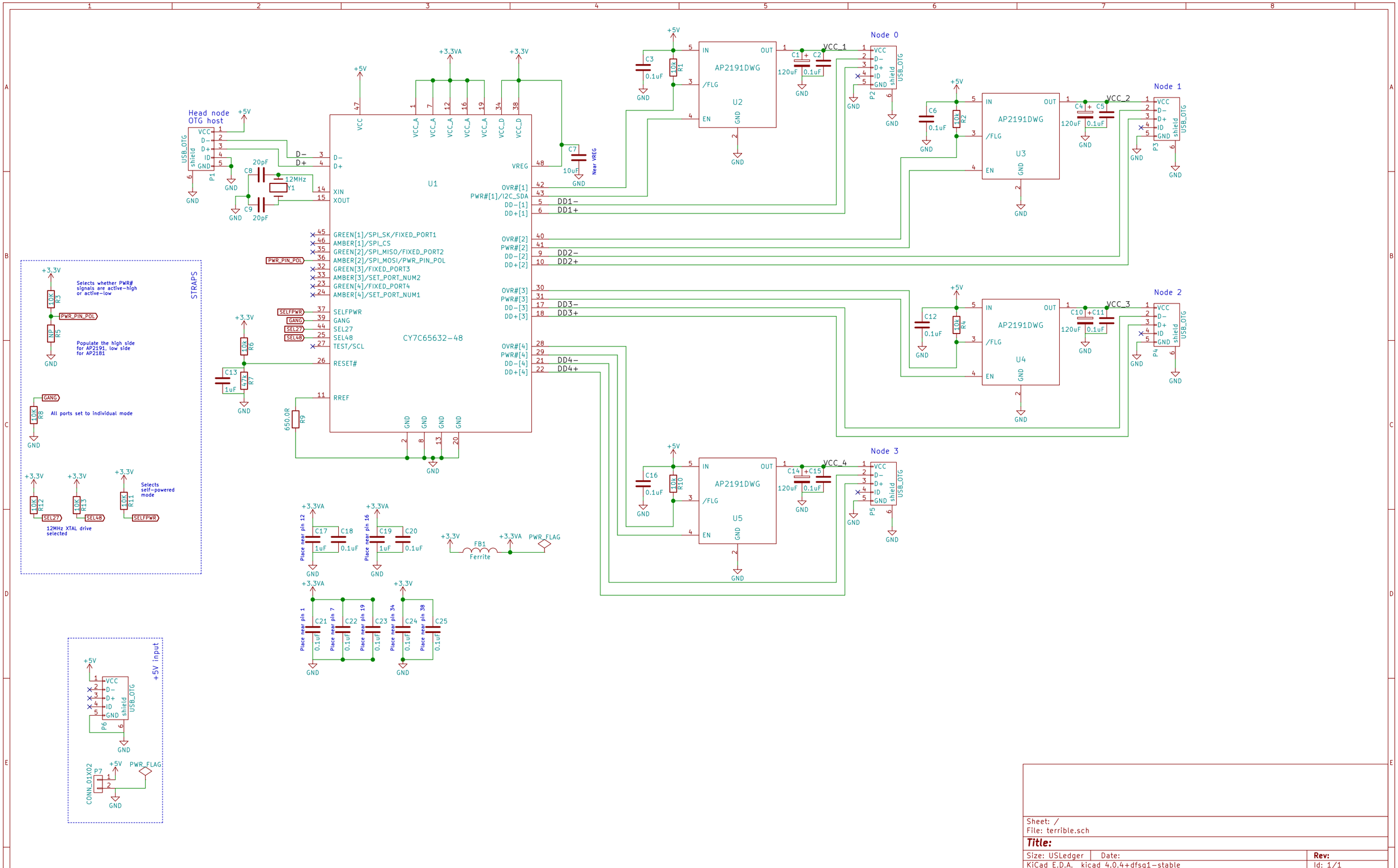
Head node
OTG host
U1
CY7C65632-48
U2
U3
U4
U5
AP2191DWG
Node 0
Node 1
Node 2
Node 3
VCC_1
VCC_2
VCC_3
VCC_4
DD1−
DD1+
DD2−
DD2+
DD3−
DD3+
DD4−
DD4+
12MHz
Y1
STRAPS
Selects whether PWR# signals are active-high or active-low
Populate the high side for AP2191, low side for AP2181
All ports set to individual mode
Selects self-powered mode
12MHz XTAL drive selected
+5V input
FB1
Ferrite
PWR_FLAG
Sheet: /
File: terrible.sch
Title:
Size: USLedger
Date:
Rev:
KiCad E.D.A. kicad 4.0.4+dfsg1-stable
Id: 1/1