STE

Standard Eurocard bus

Applications of Standard Eurocard bus range from simple control to multi-processor systems – and all boards are interchangeable.

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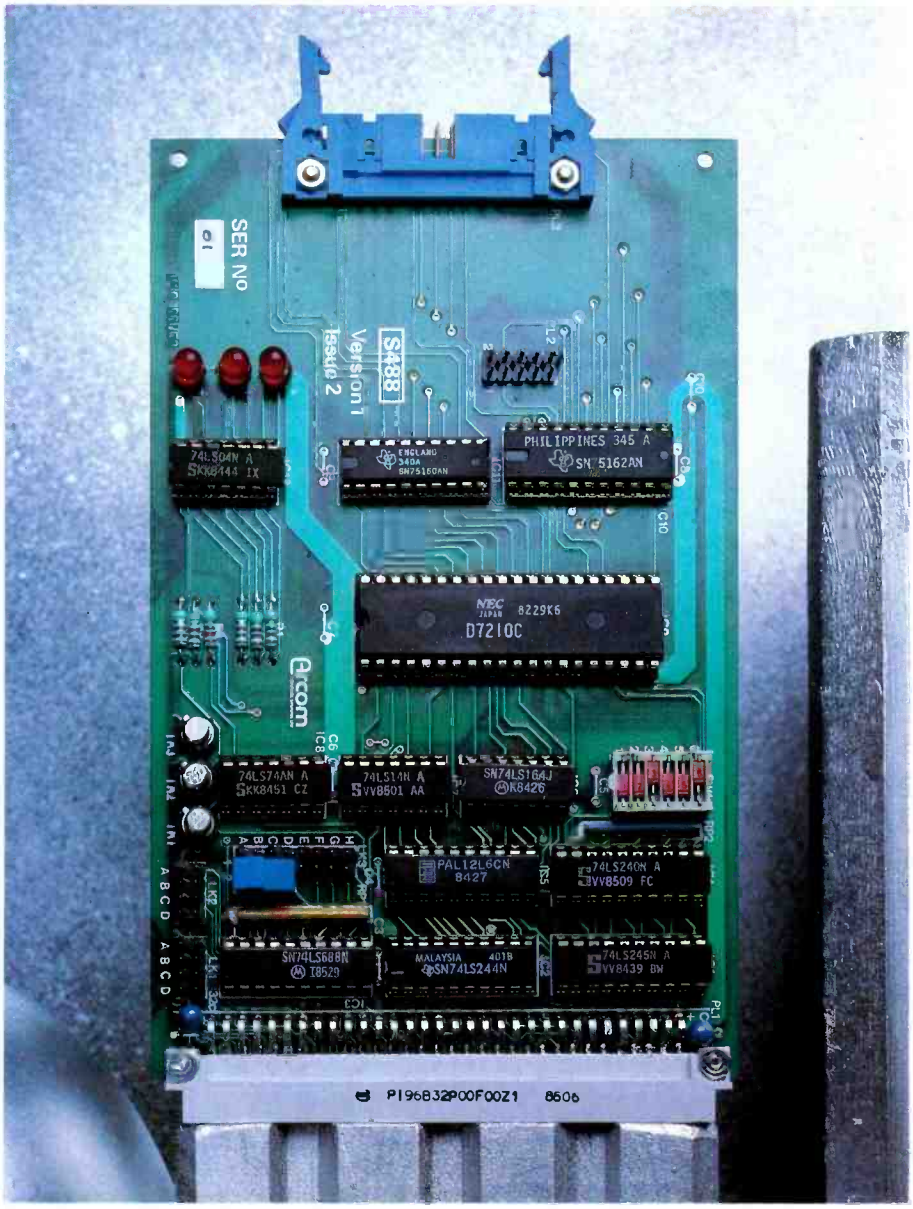
In low-to-medium complexity designs, STE bus suits the kinds of applications that buses like STD are currently used for, but with performance, security and cost advantages.

Being based on the DIN connector and Eurocard, STE can be used with other buses to form relatively low cost multiple-bus systems. And, in relation to edge connectors, the DIN connector is more reliable.

Although designed for eight-bit data buses STE can be used with the latest generation of 8/16-bit processors. The bus was first specified in 1982, and the first boards were available in mid 1984. Since then, it has been widely adopted by board manufacturers. There are now hundreds of processor, peripheral and signal-conditioning modules. Moreover STE is a standard backplane bus and so you can mix boards from any sources.

Processing units now available span a broad application range, with microprocessors from the popular Z80 to newer and more powerful devices like the 80188, Fig. 1.

In the UK so far, STE has an estimated 100 users and at least 18 companies manufacturing boards, backplanes and packaging. Applications range from software development, through real-time control, to laboratory computing.



BUSES ARE CHANGING

As more complex v.l.s.i. circuits become available, backplane buses have grown in importance helped by their recent improvements in quality. Most growth is in the high-performance 16-bit buses such as VME and Multibus-II, which include advanced features and are based on the Eurocard standard and DIN connector.

If you are looking for a standard at lower performance levels, however, choice is limited. Two current popular choices, STD and S100, are edge-connector based, with outdated signal schemes originally designed for a single 8-bit processor family. Although they have been modified to take account of more advanced processors and large memories, the patches are showing.

The situation is similar with Eurocards. There are dozens of single-Eurocard buses but almost all are designed for a single processor family and intended for simple one-processor systems. Here, none has emerged as a standard with worldwide use and support.

A typical example is G64, which uses Motorola 6809 signals. The G64 bus has now been 'enhanced' to cope with other processors, often at the expense of compatibility with earlier designs.

STE was originally conceived as a Eurocard replacement for STD. It is similar to VME, and can be viewed as an 8-bit version of that standard but, unlike VME, STE has been

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designed from scratch to be an independent bus, suitable for a broad range of processors and tasks.

BUS ATTRIBUTES

The STE signal scheme may be summarized as an eight-bit data path, with 1M-byte of memory space, 4K-bytes of i/o space, asynchronous data transfer, board position-independence, multiple master capability and inter-module flags for interrupts or d.m.a. Using Eurocard form boards with 64-way (rows A/C) DIN connectors makes STE reliable.

An eight-bit data path is used, but this is not a disadvantage. There are already good bus standards for 16-bit data paths like VME but there is no standard eight-bit Eurocard bus. Also, STE goes beyond most existing eight-bit buses in two respects. First, it can accommodate the latest generation of eight-bit processors, and of course, most 16-bit processors are also made in eight-bit versions. Secondly, the bus has multiple-master capability; up to three processors may work in a system. Another point worth noting is that almost all peripheral i.c.s are designed for eight-bit operation.

The bus is equally at home in simple systems with a single processor and a few expansion modules. Used as a vehicle for systems using familiar and popular processors like the Z80, it suits applications for which STD is currently being used.

Another advantage of STE over STD is the expansion potential given by the Eurocard packaging. The bus can be used alongside VME as a low-cost i/o channel for instance, or as a local bus for processing.

Many systems are hampered by the restricted addressing ranges of earlier buses, which were generally designed around processors limited to 64K-byte. STE provides two separate addressing fields; 4K-byte of i/o locations and a 1M-byte memory addressing space.

Processors like the Z80 can switch the top four address lines with a latch. This form of bank switching is used to advantage in operating systems like CP/M-plus, which uses this extra memory to speed up disc operations by a significant amount.

Input/output capability is similarly large. Twelve i/o address lines provide 4096 i/o locations, enough for most conceivable small-to-medium systems. Processors with no i/o space, like the 6809 pr 68008, can set aside a 4K memory block for bus i/o accesses.

A significant problem with nearly all buses is their inability to work with boards designed later in the standard's life. This is primarily because most buses use synchronous operation.

Data from a peripheral board, for example, must be available to the c.p.u. within the defined time. Processor speeds are currently doubling every four or five years, and peripherals may not be able to keep up.

To overcome this lifetime limitation, STE uses asynchronous handshaking. For example, slave boards need to acknowledge that they've received data from a master. This has two main advantages. It makes it easy to interface devices of differing speeds, and provides technology independence. As better devices become available, they will still work with boards based on earlier technology.

STE compared with other popular backplane buses.

Feature	STE	STD	G64
Signal lines	64	56	64
Address range	1M-byte	64K-byte*	64K-byte
Data path	8 bit	8 bit	8 bit
I/O space	4K-byte	256-byte*	1K-byte
Multiple masters	up to 3	off-bus connection required	yes
Error checking	error line	none	yes
Primary board size	100×160mm	114×165mm	100×160mm
Connector	DIN	Edge	DIN

*various expansion schemes

CONFIGURING STE

Users of only modest experience should be able to assemble systems successfully. STE is free from 'levels of compliance' which means that all boards are compatible with all other boards and no slots are reserved. Boards are truly position-independent.

Another feature is STE's multiple processor or multi-master ability. Up to three processors may reside on the bus, taking control of the common bus resource after going through an arbitration procedure.

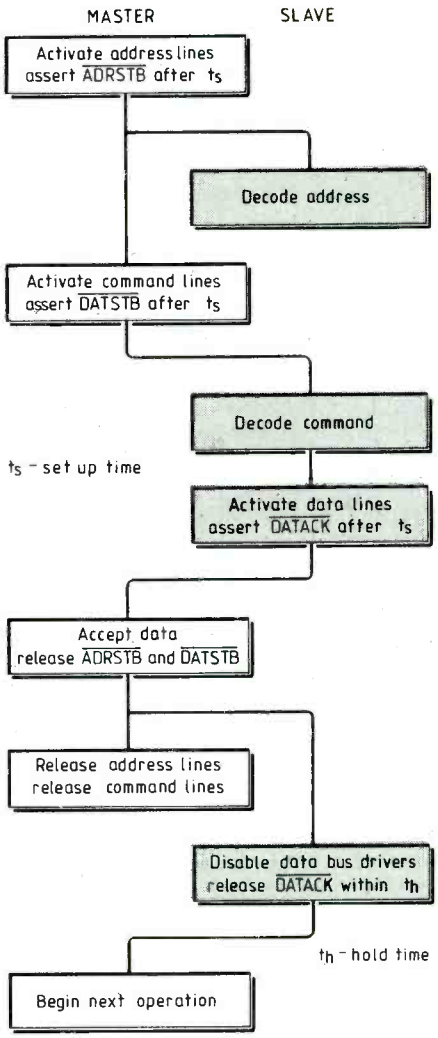
Typically, masters are c.p.u boards and d.m.a. devices. A bus slave must be able to respond to bus signals to produce an acknowledge signal when addressed.

The bus is used for communicating between boards, for example to transfer data or handle interrupts. Often, if there is enough circuitry on one board, a master can do its processing locally, freeing the STE bus for other masters to use.

For example, the Arcom SC88D board includes an 80188 processor, 256K-byte ram, and serial i/o. It only needs to use the bus to program an eprom or, say, read a value from an a-to-d converter module. Simultaneously (within a microsecond or so) another c.p.u. could be processing the converter values stored in ram on a common memory board.

Using multiple processors allows highly fault-tolerant designs to be made or reduces the cost of high-performance systems by allowing several simple low-cost masters to take the place of an expensive state-of-the-art c.p.u. board.

The STE specification permits up to three bus masters, one default and two others termed 'potential'. A default master is a board with a bus arbiter and a master, for example a c.p.u. The bus arbiter deals with requests from the master on its own board and from any other potential masters in the system.



DATA TRANSFER

An important feature of STE is asynchronous operation which increases a system's useful lifetime by allowing mixing of devices of different generations and operations speeds for example. An example of a read operating illustrates how this works in practice.

Data transfers from a slave to a master are designated read sequences. First, the master places the address of the memory or i/o location to be selected on the address lines. After a set-up time, during which the address lines become valid, the master asserts the address strobe ADRSTB. The master then activates the command lines to indicate the type of transfer, i/o or memory read, asserting DATSTB after an appropriate set-up time, thus indicating that it is ready to accept data.

The addressed slave now enables its bus drivers, placing the requested data on the data lines, then asserts DATACK after a set-up time to indicate that data is available. In response to this signal, the master accepts the data and then releases ADRSTB and DATSTB. When the slave sees this operation, it disables its data bus drivers and releases DATACK to indicate a completed sequence.

No time restrictions are placed on this operation, but designers have the option of specifying an 8μs timeout value, which serves to notify the c.p.u. of a board failure.

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Bus arbitration works at high speed so that if the bus is free the master requesting it will be granted access without unnecessary delay, typically 125ns. If the bus is busy, there may be a delay of a few hundred nanoseconds while the new master takes control, and the arbiter ensures that no contention takes place during this process.

A system error signal provides integrity of data transfer. This is asserted by the system controller if an acknowledge is not returned within a reasonable period of time. The signal can also be asserted by a slave should a local error occur during a transfer.

Integrity of the bus is also aided by careful layout of the signal lines on the DIN connector to facilitate connection while minimizing crosstalk. Ground lines are evenly distributed across the connector. Another contributing factor is increased reliability compared with edge-connected arrangements through use of the two-part DIN 41612 connector (64-way, rows a/c).

There is an intricate system for dealing with inter-modular communication, using up to eight 'attention-request' lines. Such communication usually occurs when interrupts or d.m.a. signals need to be processed, although the STE bus specification does not limit designers to these.

Interrupts can be processed in several ways. At the simplest level, no acknowledge is necessary (a power-fail interrupt for example), and an attention-request line is asserted (pulled low) by the interrupting module. With a common interrupt, the interrupting module is acknowledged by a read or write operation on one of its registers; this is also easy to arrange.

Bus-vectored interrupts are the most powerful. Here, an interrupt handler uses the command modifier lines to indicate an acknowledge cycle and puts the encoded attention-request line number onto the address bus as a three-bit address. The module which interrupted on this attention-request line can then put an interrupt vector onto the bus, which the handler reads in the acknowledge cycle.

PACKAGING

Boards for STE can be either single or double Eurocards, though the single card is the preferred size, and is expected to be used by the majority of suppliers Board depth is 160mm and extended versions are not accommodated. Small boards allow a high degree of system partitioning, i.e. they allow boards performing a narrowly-defined function such as digital i/o, serial i/o, memory etc. to be used which conceptually simplifies the system and eases fault-finding.

However some modules, especially processor boards, can be very high-density. This allows the board to work with few bus accesses, avoiding the potential bandwidth limitation that any bus imposes and thereby increasing system-throughput potential.

Most users buy boards off-the-shelf, but in some cases specialized i/o is required. With STE bus, making special i/o is relatively simple because the majority of protocol conversion circuitry required for interfacing is concentrated on the master c.p.u. boards. These boards are the ones most likely to be bought off-the-shelf and designed by a specialist board maker.

To interface a simple slave i/o board is relatively easy. A design has been published by the STE manufacturers and users group, and prototyping i/o boards, are available from Arcom.

APPLICATIONS

Where will STE be used? The answer is in all areas from data-acquisition and control to information-processing applications. These areas range from those currently catered for by STD to many of the less demanding VME applications.

Simple data acquisition and control systems are a first example. Being single Eurocard, STE allows the same kind of system partitioning as STD, but it can be used for simple control as well as for advanced 8-bit processor and multi-processor systems. An example is a Z80 c.p.u. running a disc operating system such as CP/M Plus on the same bus as a secondary Z80 board doing real-time process control; both these boards are available.

Data processing systems are another application for STE bus. Reliable rapid movements of large data blocks are possible using d.m.a. transfers and STE has a large memory addressing range.

For example, Arcom's SC88 can access 1M-byte of memory on the bus directly, and uses the on-board d.m.a. system to transfer data from the floppy and s.c.s.i. controllers at high speed, powerful operating systems like Concurrent DOS from Digital Research can be used.

Being capable of accommodating advanced processors and having other advanced design features, STE will certainly take some of the lower-level applications for which VME is often considered. It goes a step further, however.

Eurocard compatibility means that designers will be able to mix buses in a system for the best cost/performance ratio.

By selecting STE as an i/o channel for instance, you can cut costs by removing the unnecessarily complex bus-interface circuitry of VME which also increases the system's effective bandwidth by removing slow or lengthy i/o transfers.

Boards with dual-bus interfaces for this new kind of architecture have been appearing for around two years and you can now buy a VME-to-STE interface board for dual-bus systems. You will probably soon see a VME board with secondary STE bus interface on the second connector.

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STE BUS PIN-OUT

Below is the 64-signal STE bus pin-out defined on rows a and c of a DIN41612 connector. Address lines A_{0-19} provide 1M-byte of main-memory addressing. Depending on the cycle, A_{0-11} are used to address the 4K-byte of i/o space and A_{0-2} provided a three-bit ackowledge address.

Lines D_{0-7} are the eight bit data bus. Signals $\overline{ADRSTB}$ and $\overline{DATSTB}$ are address and data strobes. Lines CM_{0-2} define the type of bus cycle in progress, i.e. whether it is memory or i/o read or write, or an acknowledge; three codes are free for future expansion.

Request lines $\overline{BUSRQ}_{0,1}$ are for use by temporary masters, $\overline{BUSRQ}_0$ being higher priority. The bus is asynchronous and $\overline{DATACK}$ is asserted when a master accepts data (on a read cycle) or when its data is valid (during a write) signal $\overline{TFERR}$ is used if data from a slave is wrong.

Signals $\overline{ATNRQ}_{0-7}$ are attention-request lines and $\overline{SYSCLK}$ and $\overline{SYSRST}$ are for 16Mkz system clock and reset functions. Remaining lines are for power with fully distributed grounds.

Pin	Row a	Row c
1	0V	0V
2	+5V	+5V
3	D_0	D_1
4	D_2	D_3
5	D_4	D_5
6	D_6	D_7
7	A_0	0V
8	A_2	A_1
9	A_4	A_3
10	A_6	A_5
11	A_8	A_7
12	A_{10}	A_9
13	A_{12}	A_{11}
14	A_{14}	A_{13}
15	A_{16}	A_{15}
16	A_{18}	A_{17}
17	CM_0	A_{19}
18	CM_2	CM_1
19	$\overline{ADRSTB}$	0V
20	$\overline{DATACK}$	$\overline{DATSTB}$
21	$\overline{SYSERR}$	0V
22	$\overline{ATNRQ}_0$	$\overline{SYSRST}$
23	$\overline{ATNRQ}_2$	$\overline{ATNRQ}_1$
A3 24	$\overline{ATNRQ}_4$	$\overline{ATNRQ}_3$
25	$\overline{ATNRQ}_6$	$\overline{ATNRQ}_5$
26	0V	$\overline{ATNRQ}_7$
27	$\overline{BUSRQ}_0$	$\overline{BUSRQ}_1$
28	$\overline{BUSAK}_0$	$\overline{BUSACK}_1$
29	$\overline{SYSCLK}$	+VSTBY
30	−AUXV	+AUXV
31	+5V	+5V
32	0V	0V

Standard progress

Specification of STE is nearing completion. The P1000 Working Group, formed at the request of the IEEE Microprocessor Standards Committee, recently voted to accept draft 3.2, and the standard is now awaiting final approval. We should see publication in late-1986.

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