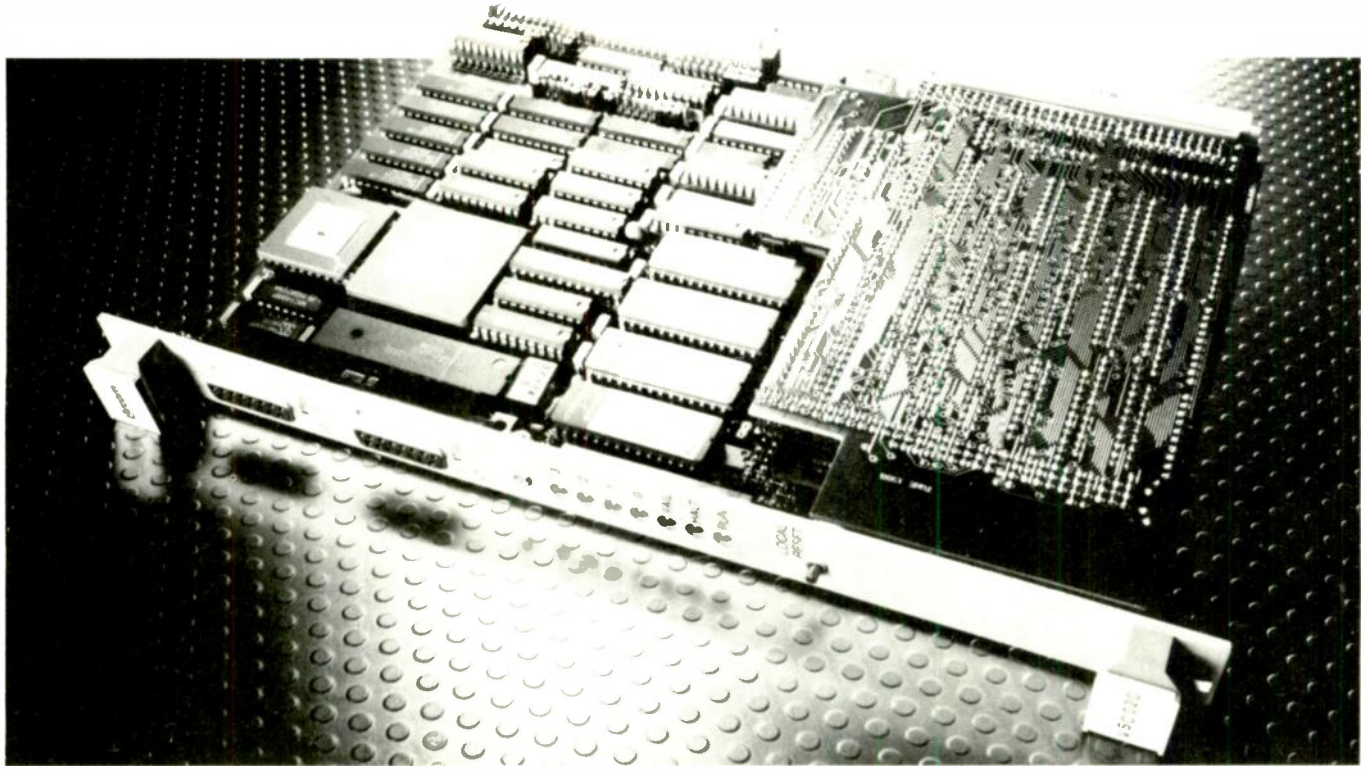


Dual buses for industrial I/O

Anthony Winter of Arcom Control Systems outlines some of the cost-saving options provided by the use of VME/STE mixed-bus architectures

It seems that the vast majority of complementary bus developments over the past few years have been aimed at increasing or optimizing overall system throughput. Typical examples are buses to provide fast local memory accessing or message passing between semi-independent intelligent subsystems. This is good news for the designer of, say, CAE workstations whose foremost concern is handling as many microinstructions per second as possible, but what about the more down-to-earth engineer developing a medium-complexity industrial control system? This type of project needs a reasonable amount of computing power and, perhaps because of this, the engineer initially opts for a bus like VME. But when it comes to implementing the I/O scheme, which might run into hundreds of channels, cost reduction becomes the major driving force. Unfortunately, this need is generally incompatible with the interfacing requirements of the VMEbus scheme and also, it has to be said, with the apparent high-profit business objectives of the majority of VMEbus board manufacturers.

This makes industrial I/O an area ripe for exploitation by multiple-bus architectures, which allow significant reductions in costs. It is now possible to achieve this result using a standard bus*. The bus in question is IEEE-1000 STEbus: a single-Eurocard scheme which is closely matched to the needs of the industrial control designer. Its 'limitation' of an 8-bit data path is, in fact, a benefit for industrial I/O applications, because it makes interfacing both simple and cheap and there is little or no performance penalty for the majority of tasks, because most I/O chips are designed for 8-bit buses. With more than 50 suppliers now in the STEbus market, there are hundreds of modules to choose from and, moreover, the members of the STEbus industry have co-operated to adopt a further informal 'signal-conditioning' standard which has resulted in a very wide range of complementary, single-Eurocard, real-world interface functions with screw terminals for easy connection to plant.

The concept of integrating the VME and STE buses was designed into STE from the start. It can be achieved by either adding an interface to a VME processor board and porting the processor's memory to both the VME and STE buses, or by building VME I/O boards with dual-bus interfaces and some latching circuitry to allow very low-cost (STEbus) processors to be used for adding intelligence to an I/O subsystem. Both these approaches are embodied in Arcom's VME-bus board line. The easiest way to understand the concept is to consider a CPU board which has dual-bus interfaces.

*See, for example, 'STE bus as an I/O bus in VME systems' by Tim Ellsmore, *Electronics & Wireless World*, February 1987, pages 143-6.

ONE BOARD, TWO BUSES

The VSC020 CPU board illustrated is a conventional double-height VMEbus 68020 processor module with an expansion connector to accept a single Eurocard containing the STEbus interface; the 68020's memory is linked to the VMEbus, STEbus and 68020. The interface to STEbus memory and I/O space appear as windows in the CPU's memory map. All the system designer needs to do to access the STEbus is write into this portion of the memory map – in the same manner as if defining the width of VMEbus memory access, for instance – and the command is transferred. The memory map opposite illustrates this.

With two bus interfaces available, the designer is free to partition the system for optimum cost-effectiveness, choosing VME modules for computation and memory, but selecting STEbus modules for the industrial

The VSC020 board with dual VME and STEbus interfaces. The STEbus interface is a daughter board, connected to the outer rows of the P2 connector. The board contains a 68020, a socket for a 68881 floating-point unit, 1Mbyte of ram, four 32-pin eprom sockets and two serial I/O channels. It costs £1250 in its 12MHz form

STEBUS BASICS

STEbus is now approved as a full world standard by the American IEEE. The 1987 standard, IEEE 1000, brings major benefits to the systems-building community, offering designers a powerful, fast and above all cost-effective means of implementing systems for applications such as control and instrumentation systems.

The bus was designed by a group of engineers independently of commercial interest, and now has a major following, with dozens of suppliers and hundreds of users. STEbus' main features are

- an 8-bit bus embracing the Eurocard standard and designed for low cost
- independence of processor manufacturers, giving the widest choice of processor on any 8-bit bus
- provision for future requirements through asynchronous, non-multiplexed data transfers at over 5Mbyte/s
- a full 1Mbyte addressing range
- up to 4Kbyte I/O space
- a position-independent, non-daisy-chained bus
- multiprocessor capability
- high-speed burst transfer mode
- eight attention-request lines
- vectored or non-vectored interrupts
- interrupt-acknowledge cycle
- read-modify-write cycle
- fully buffered signals and terminated backplane for data integrity

For many designers, one of the key design choices influencing bus selection is processor type. STEbus gives virtually unlimited freedom in this respect. Arcom alone offers no less than 12 choices of CPU embracing nine different processor families: Z80A, 64180, Z280, 80188, 8052, 6809, 68008, 8088 and 68020.

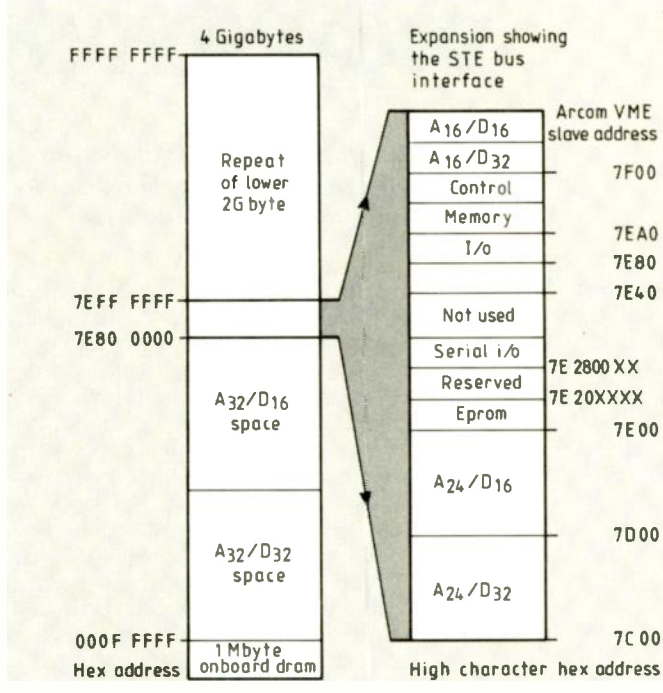
Information on STEbus is available freely via an independent manufacturers' and users' group – STEMUG. This organisation provides a number of helpful services including a document which describes the bus in considerable detail for prospective users. Free copies may be obtained from Arcom on request (Units 8-10, Clifton Road, Cambridge CB1 4WH).

In the UK, the bus has over the last 3-4 years, literally changed the face of the UK's board-level computer market, sweeping aside STD and dozens of proprietary single-Eurocard bus standards to become the dominant 8-bit board-level standard. Its main application area is in small-to-medium size data acquisition and control systems, and its standardisation as IEEE-1000 has resulted in widespread user acceptance and a fast-growing following of manufacturers. The result is a UK STEbus market currently running at some £7M pa and growing at around 50% pa.

I/O. This approach to system design changes the economics drastically. For example, a typical VMEbus I/O board, say a digital I/O function, costs around £500. Implementing the equivalent function via STEbus – which requires a simpler bus interface – works out at around £250. The larger the system, the greater the savings. VSC020 also provides a powerful upgrade path for STEbus users: some simple software changes allow an existing STEbus system's processing power to be multiplied around tenfold (this figure is taken from benchmarks of an 8MHz 68008 STEbus CPU against the 16MHz version of this 68020 board), whilst retaining all the basic programs and OS-9 operating system environment.

This facility to migrate the design either up or down in processing power is an additional and powerful capability. When a design cycle starts, unless you possess some similar detailed experience or have undertaken extensive feasibility studies, it is usually not clear how much processing power you need. The result can be a 32-bit VMEbus system performing a control task that is well within reach of a Z80 running on STEbus (at say one-quarter of the cost), or an STEbus system designer resorting to techniques such as rewriting sections of code in assembler or adding another CPU, offloading a computing task to get the system functional. An STEbus system configured in this manner has nothing left in reserve to cope with any future system expansions. The VMEbus designer has to pay a very high price for the system, whilst the STEbus designer's costs and development time have mounted out of proportion – and with the possibility of a redesign.

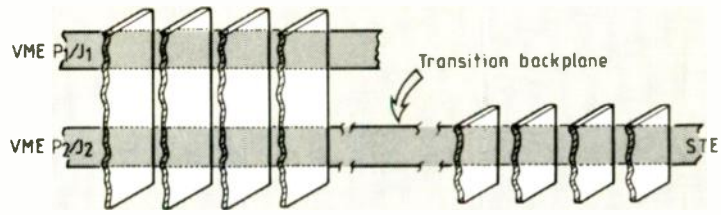
The dual VME/STEbus concept changes this situation. Provided that you choose a 68K-family processor running under the OS-9 operating system, you can start with an STEbus CPU and upgrade the computer power at a later date, or start on VME with STEbus I/O and downgrade to, say, a 68008 for the target-system versions. This flexibility also extends to the field, and consequently offers a considerable benefit to people who have started to outgrow their original STEbus systems as the I/O workload increases. This is a particular issue with STEbus systems running OS-9, the industry-standard operating system for real-time multi-tasking systems based on Motorola processors. OS-9 has a complicated and rigidly-defined I/O structure and imposes a considerable computing penalty on I/O operations. If the processor is only 8- or 8/16-bits wide, as is almost invariably the case with STEbus, then an expansion of I/O



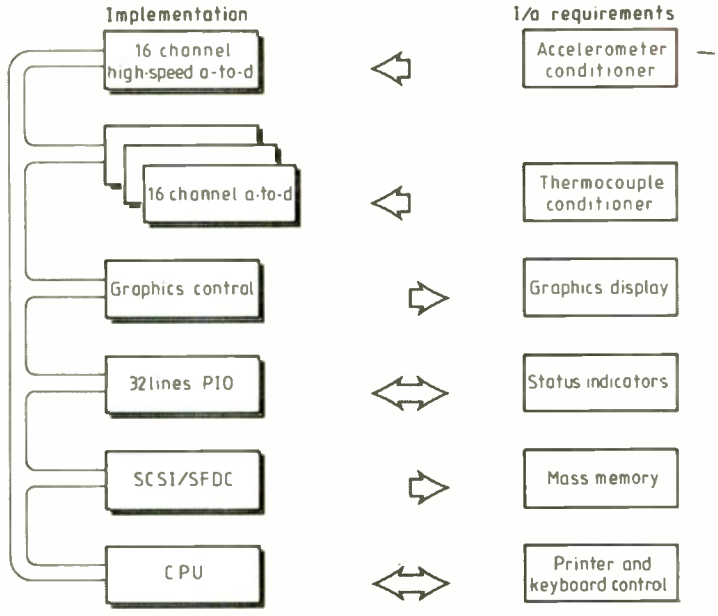
VSC020 memory map, showing how the module's memory is ported to VMEbus, STEbus and the 68020 microprocessor.

Example application demonstrates costs savings by using STEbus boards

Board function	Typical VMEbus implementation costs (£)	Typical VMEbus/STEbus implementation costs (£)
A-to-D conversion (×3)	1000 [2×1/2-height]	567 (3 boards)
High-speed A-to-D	535 [1/2-height]	372
Graphics controller	525 [1/2-height]	485
Parallel I/O	295 [1/2-height]	125
SCSI/FDDC	595	341 (2 boards)
Backplane (J1/STE)	165	98
Total	£3095	£1988



Physical connection of dual-bus systems. A full 32-bit double-height VMEbus system needs a simple transition backplane to connect STEbus to the two outer rows of P2. A 16-bit system can use an STEbus backplane directly as VME J2



An example application, illustrating the system's input/output requirements

can outgrow the system's processing capabilities. The dual-bus concept allows an upgrade to be implemented while retaining all the installed I/O and wiring. The final computer, as well as costing less can look identical to a pure VMEbus system, since both buses are based on Eurocards and can easily be integrated in standard 19-inch racks.

Physically, the STEbus interface appears on the two outer rows of the lower P2/J2 connector – the two rows unused in standard VMEbus pin assignment. This allows STEbus I/O boards – with CPUs if required – to be connected very easily: a small transition backplane takes the signals from VME to STEbus, allowing the use of two backplane systems in one cabinet. If only one 32-bit VMEbus CPU is required in the system, as it might be if the system designer started out on STEbus and is now purely upgrading the CPU power, then the position is even easier: you simply use a standard STEbus backplane on the bottom and a standard, half-height 16-bit VMEbus backplane on the top row if the VMEbus needs expanding. It is worth pointing out that not all single-Eurocard buses can work with VMEbus in this way. The G64 scheme, for example, is implemented on the a/b rows of the DIN connector, and therefore cannot work with a full 32-bit specification VMEbus system.

Adopting this approach to industrial control design does not restrict the use of either bus in any way. The VME 'side' of the VSC020 has an arbiter and mailbox circuitry, allowing it to function with other VMEbus CPUs, so that the full multiple-processor capability of VME can be exploited. Similarly, the STEbus side can also incorporate intelligence and this bus allows you to run systems with up to three processors communicating over the bus (see the box for background on STEbus).

EXAMPLE SYSTEM

The most obvious way to understand the benefits of this approach to systems design is to look at an example application. The hypothetical system shown in the diagram performs high-speed data acquisition, monitoring real-time vibration and temperature data from an engine test-bed. Even in this relatively simple system, multiple sensor in-puts demand a reasonable amount of I/O.

Accelerometers acquire the vibration data, their outputs being taken to a high-speed A-to-D converter. Less than 16 channels are needed, but rapid conversion and analysis are needed to provide a real-time graphic display of the resultant data, with signal processing using fast fourier Transforms to analyse the harmonic levels of the signal. This requires a substantial amount of computing power, so a 68020 processor board, with the built-in option of adding a floating-point processor device, is chosen.

Forty thermocouples measure temperature, the signals being digitised via three 16-channel 12-bit A-to-D converter boards. Low-cost boards are suitable for this part of the system because high-speed conversion is unnecessary.

A colour monitor presents the temperature information, some led bargraphs show the vibration levels and lamps indicate the test bed status. The hardware requirement is a high-resolution graphics board, plus 32 lines of parallel digital I/O, SCSI and floppy-disk drive.

In this example, we have not ignored the use of low-cost 'half-height' VME boards, where they are relevant. However, in general, this approach suffers from two key problems. Firstly, although the half-height VMEbus interface circuitry is simpler than for a 32-bit system, it still imposes a significant relative cost and size penalty; in systems for process control, which require low cost per channel there is still an appreciable difference compared to STEbus.

Secondly, and more fundamentally, a totally half-height VME system only allows you to upgrade to 16-bit processors – a relatively small advance in processing power, particularly when you consider some of the combined 8/16-bit chips that are readily available on STEbus. The feeling is that most designers would like to make a large jump in processing power all the way to 32 bits. Half-height VMEbus seems to be coming to an end; it fulfilled a temporary market niche whilst VMEbus was on its early curve, lowering the cost of target systems for 16-bit users, and will now begin to fade away.

The example system – despite its relatively modest I/O needs, clearly demonstrates the costs savings that can be achieved by using lower-cost STEbus boards for I/O. In this case, as can be seen from the cost breakdown shown in the table, there is around £1000 saving in I/O cost on a £3000 system. The CPU boards were not included in the figures – Arcom's VSC020 complete with dual bus interfaces, 12.5MHz 68020 and 1Mbyte ram costs £1250.

OTHER ARCHITECTURES

The dual-bus concept in this article has been introduced by looking at it on a processor board, but the system is just as easily applied to a VMEbus I/O board. Taking a 'dumb' board called VSP80 – an 80-channel parallel I/O module – as an example, the STEbus interface again appears on the two outer rows of the P2 connector, and is linked to the VMEbus via two 16-bit wide data latches, which can cause interrupts when written to. This somewhat simpler kind of inter-bus allows VMEbus users to implement their I/O systems with the benefit of low-cost STEbus CPU's as intelligent controllers. The latches provide a mechanism for controlling the use of the board between the host VMEbus CPU and the slave STEbus I/O controller.

In a further article, Jeremy Bentham will outline the software considerations of dual bus systems.