SCO9

STEbus 6809 Processor Board

Technical Manual

Product Information

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Contents

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Section 1. introduction

The SC09 is a 6809 based microprocessor board for use on the STEbus. It will run the OS-9 operating system, and can be used either as a development or a target system; alternatively those not wishing to use OS-9 can write code on a different 9809 system and blow that code into EPROM for use on the SC09.

The board contains all the necessary interface logic for the STEbus including an arbiter. An RS232 serial port is provided for connection to a terminal, and additional serial or parallel links can be provided over the STEbus. The interrupt capabilities of the board have been made very flexible so the board can be used in a large number of system configurations.

The fact that the STEbus is a standard bus means that a wide range of peripheral boards are available from several sources. The bus allows the user to add memory and I/O boards to their system with both flexibility and expandability. Up to two other processors can share the STEbus with the SC09 and so share expensive peripherals, for example one possible system might be to use an SC09 running OS-9 for control purposes and a Z80 CPU for text processing.

Section 2. Circuit Description

The SC09 uses a 2 MHz 6809E processor (by cutting a track and making a link a 1 MHz system can be selected). The serial link is provided by a 6850 ACIA (Asynchronous Communications Interface Adaptor) chip and runs at 4800 baud (2400 baud for a 1MHz system). Signals from the ACIA are converted to RS232 levels by IC18, and signals to the ACIA are converted to TTL logic levels by IC19. The ACIA can be programmed to use RTS and CTS handshaking. Data and handshaking lines are taken off the board via a ten way ribbon connector, PL3.

The 6840 PTM (Programmable Timer Module) provides three 16-bit counter/timers which can also be used for waveform generation. One of these (Timer 2) is used for baud rate generation, and the other two are for use as the OS-9 system clock or for user applications. The G inputs to to timer numbers 1 and 3 can be grounded by making links 18 and 19 - this should be done if the timers are being used solely for counting or generating waveforms. The input and output lines of the 6840 are available on the ten way ribbon connector PL2.

Four memory sockets are provided, two 24 pin and two 28 pin. One of the 24 pin sockets is for a 4k EPROM (2732) and resides at the top of memory, the other is for 1k of RAM (6116). Both of these chips are always in the memory map, thus the RAM can be used to store data required by different pages of STEbus memory.

The two 28 pin sockets are for 8k (6264) or 32k (55257) RAMs, and 8k (2764), 16 (27128) or 32k (27256) EPROMs. These two sockets can be individually mapped in and out of the memory map under software control, by bits four and five of the control latch. See 'Links and Options' and 'Memory Map' sections. Thus mapping them out means more STEbus memory is available whereas mapping them in means data or OS-9 modules are available across all STEbus pages. Links 14-17 select whether the sockets are RAM or EPROM.

On the STEbus the SC09 acts as the default master and contains an on-board arbiter to grant the bus to potential masters. When a potential master wishes to use the STEbus it asserts either BUSRQ0* or 1* (BUSRQ0* has higher priority). On receiving a BUSRQ* signal the arbiter (IC9) asserts the /HALT signal to the 6809 and when the 6809 has finished its present instruction and gone into a HALT state the arbiter will grant the bus to the potential master by asserting BUSAK0* or 1*. The potential master can now make use of the bus. When it has finished with it BUSRQ* is negated, and the arbiter negates BUSAK* to release the SC09 form its halted state.

The SC09 can access 16 pages each of 56k of STEbus memory and 1k of STEbus I/O locations. The I/O locations are always in the memory map; 6809 addresses &E000-E3FF correspond to STEbus I/O locations &000-&3FF. The chosen page of STE memory is contained in the lower four bits of the control latch (IC23, location &E400). This latch is zeroed on power-up or a reset signal. The control latch is write only so the user should keep a Read/Write copy if its contents in the 1k of RAM which is always mapped in. This allows a program running in STEbus memory to know which page it is running in and the state of the other control bits.

When the SC09 wishes to read or write to STEbus locations the following occurs; the SC09 sets up the address A0-19 (A16-19 are bits 0-3 of the control latch, A0-15 the 6809 address lines), the data lines D0-7 in the case of a write, and the command modifier lines CM0-2. These indicate whether the access is read or write and whether to memory or I/O locations. The CM0-2 lines are set up in hardware by the SC09 and so they are transparent to the user. The bus logic controller (IC10) then enables the bus driver chips (ICs 1, 2, 3, 5) and asserts the two strobe lines ADRSTB* and DATSTB*. These indicate to the accessed STE device (known as a slave) that the address, data and command modifier lines are valid. The 6809 processor E and Q clocks are then stopped until the bus logic receives either a DATACK*, TRFERR* or TIMOUT signal. The processor clocks are then re-enabled and the bus drivers disabled.

A ADTACK* signal from the slave indicates the slave has accepted or provided data , this being the response for a successful bus access. TRFERR* indicates that the slave has responded with an error condition, for example a parity error or an attempt to write to read only memory. TIMOUT is

generated by IC16 and indicates that no slave responded to the bus access within a period of about 8 µs. The TIMOUT signal prevents the board waiting interminably for a DATACK* or TRFERR*, which occurs if the SC09 attempts to access a non-existent memory or I/O location.The TIMOUT signal also ensures that the 6909 clocks are not stopped for long periods of time. The 6809 needs to refresh its internal registers at least every 15 microseconds or it will cease to function correctly. TRFERR* and TIMOUT both produce the same effect on the processor if an NMI or FIRQ (selected by link 6) is generated. The interrupt is cleared by the vector fetch cycle of the 6809 so the user does not need to clear the interrupt explicitly. It is strongly advised that the TIMOUT or TRFERR* routines are contained in on-board memory and use the on-board RAM for generating error messages, otherwise if TIMOUT is produced because of a faulty STEbus memory card and the NMI or FIRQ routine utilises this card then the system will crash. The user can use the TIMOUT facility to enable the SC09 to scan through STE memory on start-up either to search for OS-9 modules or simply to find out how much memory is available.

Since the STEbus accesses slow down the processor clocks, IC10 also provides a constant 2Mhz (or 1MHz if selected) E clock for the 6840 PTM and 6850 ACIA. This ensures that the 4800 baud rate is maintained. When the 6809 wishes to access either of these devices, IC10 stops the processor clocks until they are synchronised to the 6840/6850 clock, so the user should note that accesses to these two devices can take up to one additional CPU cycle.

The SC08 can respond to up to two STE interrupts selected from ATNRQ0-3* (See 'Links and Options' section). One of these interrupts can be jumpered to either /NMI or ?FIRQ (link J5B or A respectively), whichever is not being used for TIMOUT/TRFERR*. The other can be jumpered to /IRQ (J4). It is suggested that if an ATNRQ* line is used as a power fail indicator it should be jumpered to /NMI and TRFERR/TIMOU to /FIRQ, otherwise jumper TRFERR/TIMOUT to /NMI. The SC09 can send an interrupt to one of the ATNRQ0-3* lines (Link area 1). This ATNRQ* is asserted by writing a 1 into control latch bit 7, and the programmer is responsible for ensuring that it is cleared.

The board has a power-on reset circuit (IC6). If link J3 is made the reset signal is sent to the STEbus SYSRST* line. If link J7A is made the SC09 will be reset by the STE SYSRST* signal. Note that only one of these jumpers should be made otherwise the resets will 'loop' round and the SC09 will be held in a permanent reset state. The preferred reset arrangement is to make J3 leaving J7A open, and to connect a push-to-make switch across J7B.

IC14 produces the 16MHz STEbus clock (SYSCLK). This signal will be sent onto the STEbus backplane if link J8 is made. The STEbus must have ONE and ONLY ONE source of SYSCLK so before removing this link ensure that another board is supplying this signal.

Section 3. STEbus Interface

The SC09 has an STEbus interface, denoted IEEE 1000 1987. Here is a summary of the features of the bus with some notes on the implementation of he SC09.

Table 1. STEbus Interface on the SC09

Signal	In/Out	Type	Description	Implementation
A0-19	O	3s	20-bit memory address	A0-15 are driven directly from the 6809. A16-19 are bank-switch bits from the control latch.
A0-11	O	3s	12-bit I/O address	Driven directly from the 6809.
A0-2	O	3s	3-bit acknowledge address	The SC09 does not handle bus-vectored interrupts. It responds to bus interrupts on lines ATNRQ0* to ATNRQ3* if appropriately jumpered.
D0-7	I/O	3s	8-bit data bus	Driven by the CPU on write cycles, or by the slave on read cycles.
ADRSTB*	O	3s	Address strobe	Addresses, data and command modifiers are valid before the falling edge of ADRSTB* and DATSTB*.
DATSTB*	O	3s	Data strobe	On the write cycle, valid data and CMo are present before this is asserted. On a read cycle, CM0 is high before DATSTB* is asserted inform the slave that the processor is ready to accept data.
CM0-2	O	3s	Command modifiers	Indicates the kind of bus cycle, according to the following table: CM2, 1, 0 0 0 0 reserved 0 0 1 reserved 0 1 0 reserved 0 1 1 acknowledge 1 0 0 I/O write 1 0 1 I/O read 1 1 0 memory write 1 1 1 memory read (NOTE: the acknowledge cycle is not generated by the SC09)

Signal	In/Out	Type	Description	Implementation
BUSRQ0-1*	O	o/c	Bus requests	Potential (temporary) bus masters request the bus from the arbiter on either of these lines. BUSRQ0* has a higher priority than BUSRQ1*.
BUSAK0-1*	I	in	Bus acknowledge	The arbiter acknowledges a request from either of the two potential masters on these lines. A potential master may only drive the bus when it has received an acknowledge on the line corresponding to its request.

The SC09 is always the permanent bus master, and contains an on-board bus arbiter. Potential master may request the bus on the BUSRQ* lines and the arbiter will grant the bus to the highest priority request. Only one SC09 may be present on the bus. See ‘Links and Options’ for details of how to set up the board.

An SCO9 configured as standard will generate all necessary bus signals as a permanent master. All that is required to generate a bus access is that you try to read or write to a memory or I/O location that the on-board logic defines as on the bus. See the ‘Memory Map’ and ‘I/O Devices’ sections for details on which addresses are on board and which are not.

Signal	In/Out	Type	Description	Implementation
DATACK*	I	3s	Data acknowledge	The slave addresses by the master asserts this line to indicate that it has accepted data from a write cycle, or that its data is valid during a read cycle.
TRFERR*	I	3s	Transfer error	If data from the slave are wrong (for example due to a parity error) then the slave asserts this signal instead of DATACK*. The SC09 responds identically as if no error has occurred. This signal exists in the specification for compatibility with further advances in system design.
ATNRQ0-7*	I	o/c	Attention requests	It is suggested that ATNRQ0-3* are used for interrupts, and ATNRQ4-7* are reserved for DMA requests, with ATNRQ0* having the highest priority. ATNRQ4-7* are ignored by the SC09.

Signal	In/Out	Type	Description	Implementation
SYSCLK	O	tp	System Clock	16MHz system clock. May optionally be generated by the SC09.
SYSRST*	I/O	o/c	System Reset	The SC09 may either generate or accept this signal from the bus.

It is quite easy to use the SC09 on the STEbus. You will need a terminated backplane and one or more slave (peripheral) boards, such as A/D converters. In order to fully comply with the specification, the impedance of each backplane line should be 60 ohms +/- 10%. However a short backplane is not likely to cause any malfunction even if its impedance varies considerably from this. A terminator is necessary because some of the lines are open-collector, and timing is critical on the strobes. Suitable terminated backplanes are available from Arcom.

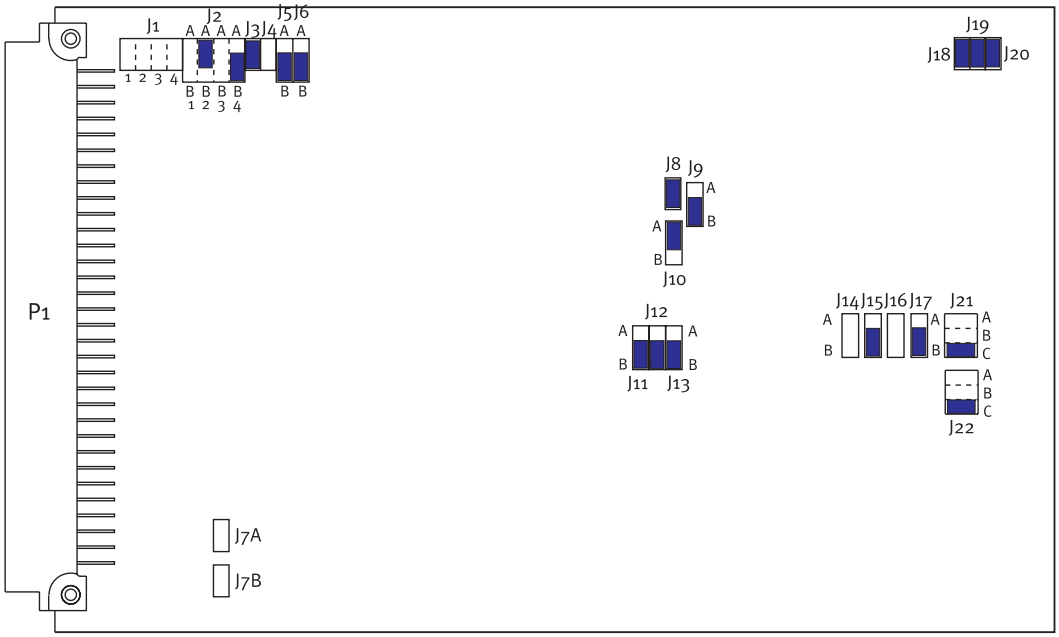
Section 4. Links and Options

In this section it is assumed that you are looking at the board with the Euroconnector to your left.

Note: '+' Indicates the standard jumpering , as supplied

'*' Indicates a signal is active low.

Link Positions



Link area J1. ATNRQOUT* destination

Selects which of the ATNRQ* lines the ATNRQOUT* line goes to.

J1-1	ATNRQOUT* to ATNRQ3*
J1-2	ATNRQOUT* to ATNRQ2*
J1-3	ATNRQOUT* to ATNRQ1*
J1-4	ATNRQOUT* to ATNRQ0*

Link area J1

0 0 0 0
1 2 3 4
0 0 0 0

Writing a 1 into bit 7 of the control latch and making one of these links asserts an active low ATNRQ* line on the STEbus.

Link area 2. /IRQ, /NMI, and /FIRQ sources

Selects which of the ATNRQ* lines are enabled as inputs to the SC09. Two lines may be selected, on for /IRQ, one for /NMI or /FIRQ.

J2A1	/NMI or /FIRQ from ATNRQ3*
+ J2A2	/NMI or /FIRQ from ATNRQ2*
J2A3	/NMI or /FIRQ from ATNRQ1*
J2A4	/NMI or /FIRQ from ATNRQ0*
J2B1	/IRQ from ATNRQ3*
J2B2	/IRQ from ATNRQ2*
J2B3	/IRQ from ATNRQ1*
+ J2B4	/IRQ from ATNRQ0*

Link area J2

0 0 0 0
A 1 2 3 4
0 0 0 0
B 1 2 3 4
0 0 0 0

For example the previous arrangement selects ATNRQ2* for /NMI or /FIRQ, and ATNRQ0* for /IRQ. This link causes the open collector outputs of IC7 to follow the chosen ATNRQ* lines. To allow these drivers to affect the 6809 interrupt lines links 4 and 5 must also be made.

Link areas 3 and 7. Reset Circuit

Making J3 enables the power-on reset circuit (IC6) to reset the STEbus as well as the SC09. Making J7A allows a reset signal on the STEbus to reset the SC09. Obviously both links can not be inserted at once or the SC09 will be held in a permanent reset state. You are recommended to make J3 and J7B, then connect a momentairy push-to-make switch access J7B. The switch can then reset both the SC09 and the STEbus.

Link area J7
0
A
0
0
B
0

+ J3 SC09 reset to STEbus

J7A SC09 reset from STEbus

J7B Connect push-to-make switch across here for reset switch

Link J4. /IRQ from ATNRQ*

Making J4 allows the ATNRQ* line selected by side B of link 2 to pull the 6809 /IRQ line low.

J4 ATNRQ* form J2 to /IRQ.

Link area 5. ATNRQ* Interrupt type.

J5A ATNRQ* form J2 to /NMI.

+ J5B ATNRQ* form J2 to /FIRQ.

Link area 6. Timeout/Transfer-error interrupt type.

J6A TIMOUT/TFRERR* to /NMI.

+ J6B TIMOUT/TFRERR* to /FIRQ.

Since the TIMOUT/TFRERR* line is not open collector /NMI or /FIRQ cannot be selected by both links. Omitting J6 prevents the 6809 being interrupted but does not disable the bus timeout circuitry. J5 and 6 should be omitted if the user has not written the code to handle these interrupts.

Link 8. SYSCLK source

Making J8 enables the 16 MHz SYSCLK signal to reach the STEbus backplane. One and only one source of SYSCLK is required so remove this link is another board is supplying this signal.

+ J8 16MHz clock to STEbus.

Link 9. IC22 present on reset

Link area 9
0
A
0
B
0

J9A IC22 mapped IN on reset
or if control latch bit 5 is LOW

+ J9B IC22 mapped OUT on reset but mapped in
when bit 5 of the control latch is HIGH.

This controls whether or not the bottom memory socket (IC22) is mapped in on

reset; if it isn't then STEbus (off board) memory is mapped in instead.

This link means that if the user has an external memory board then memory on that board is mapped in on reset with J9B, so IC22 can be omitted, alternatively if the user does not have an external memory board then setting J9A means IC22 is used on reset.

Link area 10. 6809 clock speed

+ J10A 2MHz processor clock

J10B 1MHz processor clock

NOTE: The SC09 has this link card hard wired in the A position, so if a 1 MHz system is desired the track on the back of the board must first be cut before inserting the link in the 1MHz position.

Link area 10

0
A
0
B
0

Links 11, 12 and 13. Standby power to RAMs

Select whether ICs 15, 20 and 22 use power from the +5V rail or from the +VSTBY line. The +VSTBY line should only be used if these sockets contain low power CMOS RAM chips and battery back-up is needed.

J11A +VSTBY to IC15
+ J11B +5V to IC15
J12A +VSTBY to IC20
+ J12B +5V to IC20
J13A +VSTBY to IC22
+ J13B +5V to IC22

Link areas 10 to 17

0
A
0
B
0

Link areas 14, 15, 16 and 17. IC20 and IC22 device type and sizes

Control whether sockets IC20 and 22 are 8, 16 or 32k.

J14A	IC20 pin 26	is A13	(16/32k EPROMs, 32k RAM)
J14B	IC20 pin 26	is VCC	(8k RAM/EPROM)
J15A	IC20 pin 1	is 5V	(EPROM)
+ J15B	IC20 pin 1	is A14	(32k RAM)

J16A	IC22 pin 26	is A13	(16/32k EPROMs, 32k RAM)
J16B	IC22 pin 26	is VCC	(8k)
J17A	IC22 pin 1	is 5V	(EPROM)
+ J17B	IC22 pin 1	is A14	932k RAM)

Links J18 and J19. 6840 PTM gate

Used to ground the gate inputs to timers 1 and 3 of the 6840. These links should be inserted for normal use of the timers. Removing them allows the user to send logic level signals in via connector P2. For further details of how to use the 6840 refer to the relevant data sheets.

+ J18 Counter 1 gate input grounded
+ J19 Counter 3 gate input grounded

Link 20. 1Hz tick enable for OS-9

+ J20 1Hz ticks enabled for OD-9

Link areas J21 and J22. IC20, 22 RAM/EPROM device type

J21A IC20 pin 27 is A14 (32k EPROM)
J21B IC20 pin 27 is 5V (8k/16k EPROM)
+ J21C IC20 pin 27 is /WR (8k/32k RAM)
J22A IC22 pin 27 is A14 (32k EPROM)
J22B IC22 pin 27 is 5V (8k/16k EPROM)
+ J22C IC22 pin 27 is /WR (8k/32k RAM)

Link Summary

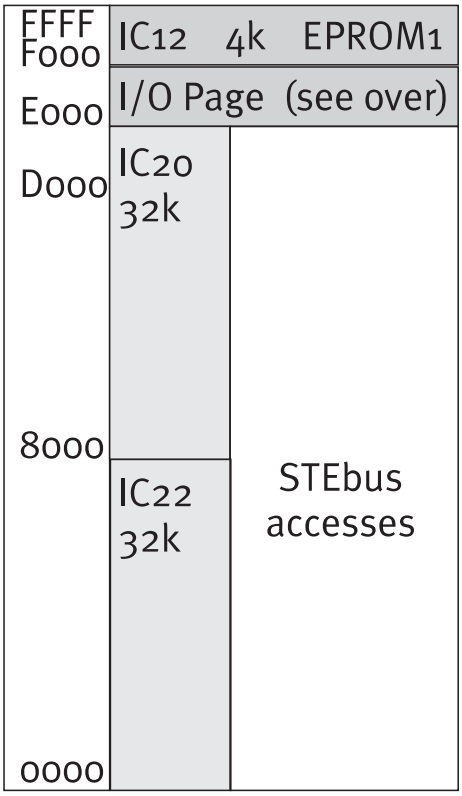
Device		IC20			IC22		
Size	Type	J14	J15	J21	J16	J17	J22
8k EPROM	2764	B	A	B	B	A	B
16k EPROM	27128	A	A	B	A	A	B
32k EPROM	27256	A	A	A	A	A	A
8k RAM	6264	B	B	C	B	B	C
32k RAM	62256	A	B	C	A	B	C

Section 5. Memory Map

The SC09 (boards V1 I2 or greater) can accept 32k RAM chips. In some cases this will allow the SC09 to act as a target system without an additional memory card.

Avoid switching memory from a program running in an area of memory which will be switched out, because the program will disappear as soon as the memory is switched!

The address that is put on the bus during memory bus access is the same as the 6809 address. There is no translation. The 6809 address is 16 bits, however, and the STEbus address is 20 bits. The extra four bits come from the control latch, and these should be set to the correct value before bus access is attempted.



Devices above E000 are always present

IC22 is mapped in if control latch bit 5 is LOW and J9A is made, or if bit 5 is HI and J9B is made.

If IC22 is disabled, accesses below 8000 are STEbus accesses.

If RAM/EPROMs amaller than 32k are used, they are echoed within the 32k space.

I/O page

I/O Page Address	Control Block register
EC00 - EFFF	1k RAM (IC5)
EA00 - EA01	6850 ACIA (IC17)
E800 - E807	6840 PTM (IC21)
E400	Control latch (IC25)
E000 - E3FF	1k STEbus I/O

Control Latch

The control latch (IC23, memory location &E400) is set to zero on reset. The latch is write only so the user should keep a copy of its contents in the RAM starting at &EC00, since this RAM is always in the memory map.

Bit	Function
0	STEbus A16
1	STEbus A17
2	STEbus A18
3	STEbus A19
4	IC 20 mapped in if LOW, if high then these locations are STE memory.
5	IC 22 appears in memory map if this bit is either LOW and J9A made, or HIGH and J9B made, otherwise STE memory.
6	Unused by SC09 at present.
7	Set HIGH to assert ATNRQ (selected by J1).

Section 6. Setting Up

To set up SC09 all that is needed is an STEbus backplane and terminator and a terminal. Other optional STEbus boards, for example memory or floppy disk controller may be added.

Connect the RS232 link from P3 to a terminal set to 4800 baud, and insert a boot EPROM into the SC09 (IC12). A machine code monitor with many useful routines is available for this purpose. Ensure the links are set correctly and switch on the power. If all is well the monitor prompt should appear on the terminal. Use the monitor to peek and poke memory STE locations to check the system is working correctly. Alternatively if you have an OS-9 system see the OS-9 manual for information on how to get going.

If the SC09 will not produce a prompt on reset first check that the terminal is set to 4800 baud and is not driving CTS (Pin24) on the 6850 high. If so remove the handshaking from the terminal . Check to see if the SC09 is HALTED (Pin 40 of 6809 low). If it is, investigate the levels of the BUSRQ* lines on the backplane to make sure that they are high. If they are held low for any reason then the SC09 will continuously grant the bus to a requesting master and will remain halted. Also ensure that the SC09 is the only permanent master on the bus. Finally to check see if Pins 3 and 4 of the 6850 have a clocking signal on them (76.8 kHz). If not then your program or the 6840 are not functioning correctly.

If the SC09 will not communicate with the STEbus, first check that the SYSCLK is present and is coming from only one source, and that the bus has a terminator. Then check to see whether DATACK* or TRFERR* signals are present. If not then make sure the linking on slave boards is correct and that the SC09 is not trying to access non-existent memory or I/O locations. If DATACK* signals are present then a slave board is replying, IF it does not send or accept data, check that the slave board is not a read only board.

Finally check the problems are not caused by a faulty backplane by putting the SC09 in another slot, and if available using another STE master to prove the slave board works.

Appendix A. Component List

Semiconductors

IC1, 2, 3, 5	LS245
IC4	LS240
IC6	TL7705
IC7	7406
IC8	68B09E
IC9, 10	PAL16R6 Logic Array
IC11	PAL16L8 Logic Array
IC12	2732
IC13	Ls02
IC14	74S04
IC15	6116
IC16	LS393
IC17	68B50
IC18	MC1488
IC19	MC1489
IC20, 22	6264, 2764 or 27128
IC21	68B40
IC23	LS273

Note: For 1MHz version omit ‘B’s in ICs 8, 17, 21
For 2MHz operation ICs 12, 15, 20, 22 should have access times of 350ns or better.

Resistors

R1, 2	470R
R3, 4, 5, 6, 7, 8	4k7
R9	1k5
R10, 11	330R
R12	8k2

Capacitors

C1, 2, 10, 18	10uF decoupling
C3, 4	180pF
C5	100nF
C6	22 uF
C7	Omitted
C8	100 nF
C9, 11-17	100nF decoupling

Miscellaneous

XL1	16MHz Crystal

Appendix B. Connections

All connectors are shown looking into the board, or onto the board with PL1 on the right.

P1. STEbus 64-way a/c DOM41612 (Shown looking into backplane).
(For suitable backplanes refer to current catalogue).

Pin		Row a	Row c	
1	GND	o	o	GND
2	+5V	o	o	+5V
3	D0	o	o	D1
4	D2	o	o	D3
5	D4	o	o	D5
6	D6	o	o	D7
7	A0	o	o	GND
8	A2	o	o	A1
9	A4	o	o	A3
10	A6	o	o	A5
11	A8	o	o	A7
12	A10	o	o	A9
13	A12	o	o	A11
14	A14	o	o	A13
15	A16	o	o	A15
16	A18	o	o	A17
17	CM0	o	o	A19
18	CM2	o	o	CM1
19	ADRSTB*	o	o	GND
20	DATACK*	o	o	DATSTB*
21	TFRERR*	o	o	GND
22	ATNRQ0*	o	o	SYSRST*
23	ATNRQ2*	o	o	ATNRQ1*
24	ATNRQ4*	o	o	ATNRQ3*
25	ATNRQ6*	o	o	ATNRQ5*
26	GND	o	o	ATNRQ7*
27	BUSRQ0*	o	o	BUSRQ1*
28	BUSAK0*	o	o	BUSAK1*
29	SYSCLK	o	o	VSTBY
30	-12V	o	o	+12V
31	+5V	o	o	+5V
32	GND	o	o	GND

P2. 10-way connector, 6840 Timers 1 and 3 inputs and outputs

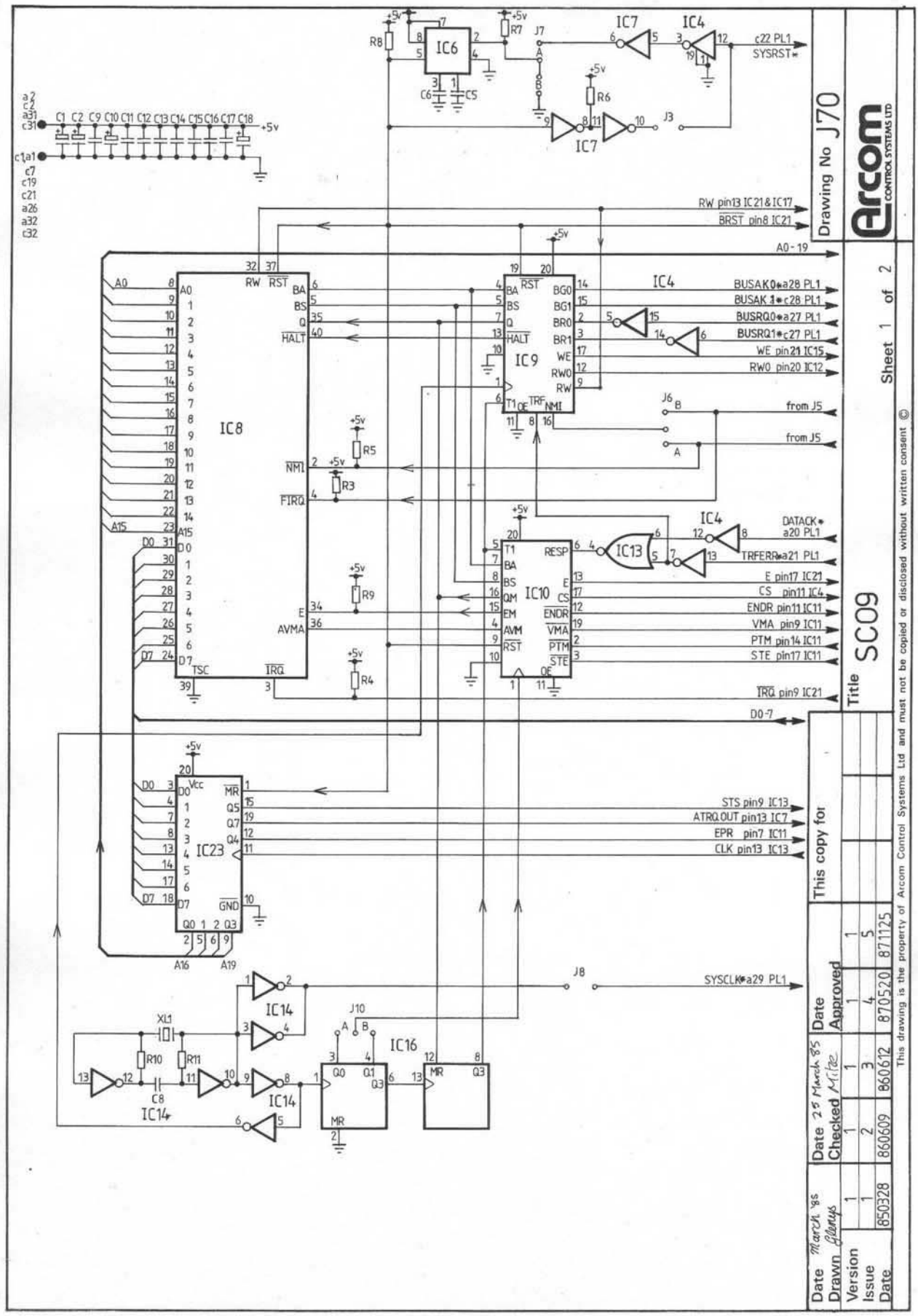
O1	1	O	O	2	O3
C1	3	O	O	4	GND
G1	5	O	O	6	GND
C3	7	O	O	8	GND
G3	9	O	O	10	GND

P3. RS232 Serial I/O connector (one channel)

TXD out	1	O	O	2	RXD in
RTS out	3	O	O	4	CTS in
GND	5	O	O	6	n/c
n/c	7	O	O	8	n/c
n/c	9	O	O	10	n/c

Appendix C. Specifications

Operating Temperature	5°C to 55°C (non-condensing)
Power Consumption (typ)	5V +/- 0.25V 1.1 A +12V +/- 1V 30 mA -12V +/- 1V 30 mA
Microprocessor	68B09E 2MHz
On-board memory capacity	64k RAM 64k ROM
Off-board memory capacity	1 Megabyte
On-board I/O	1 RS232 channel
	3 counter/timers
Off-board I/O	4096 locations
Bus	STEbus
Bus connector	64a/c DIN 41612
Format	Single Eurocard
Dimensions	173mm x 100mm x 15mm
Weight	160g


Drawing No J70
Arcom CONTROL SYSTEMS LTD
Sheet 1 of 2
Title SC09
This copy for
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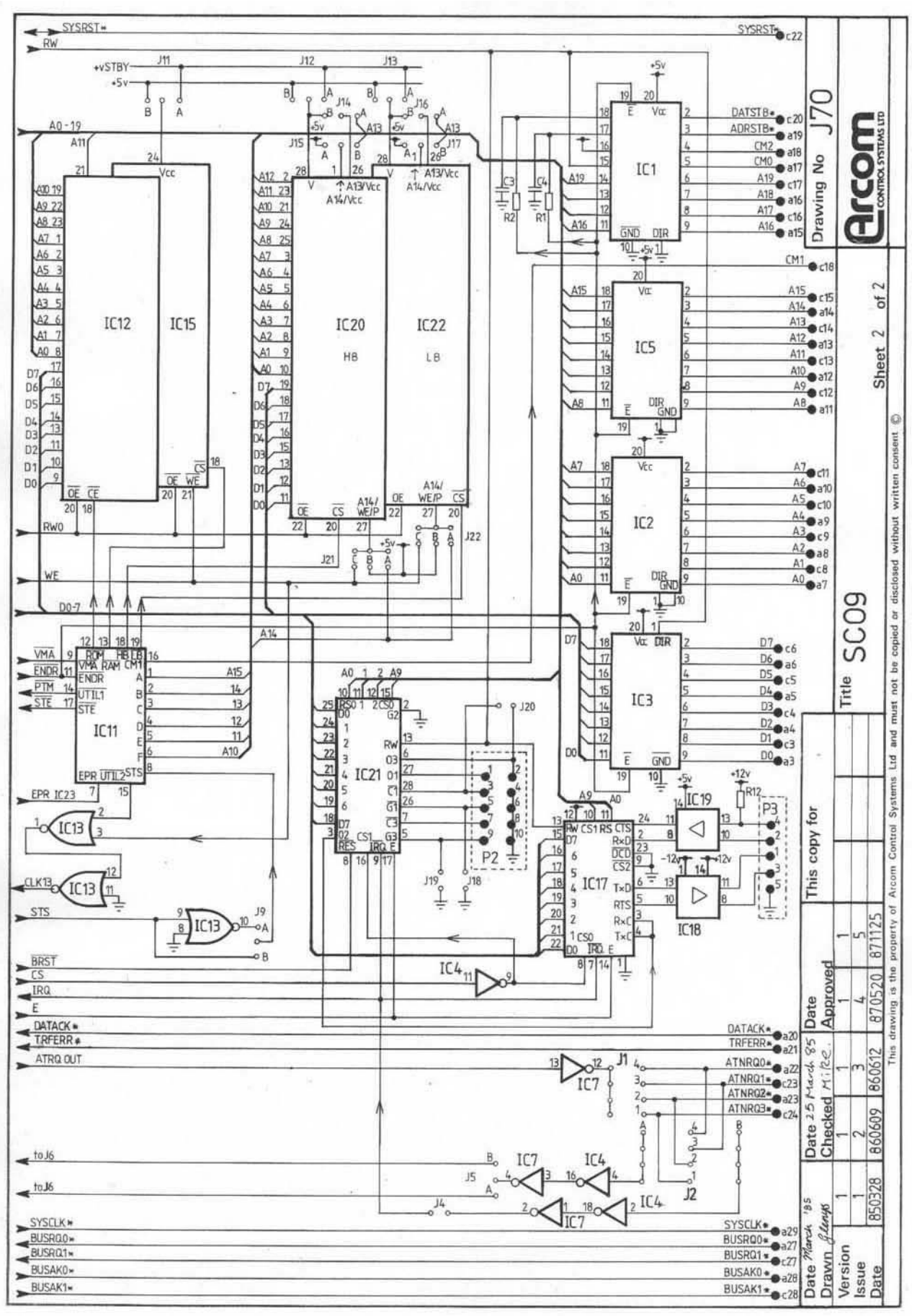
IC8
IC9
IC10
IC23
IC4
IC7
IC6
IC13
IC14
IC16
RW pin13 IC21 & IC17
BRST pin8 IC21
A0-19
BUSAK0*a28 PL1
BUSAK1*c28 PL1
BUSRQ0*a27 PL1
BUSRQ1*c27 PL1
WE pin21 IC15
RW0 pin20 IC12
from J5
from J5
DATACK* a20 PL1
TRFERR*a21 PL1
E pin17 IC21
CS pin11 IC4
ENDR pin11 IC11
VMA pin9 IC11
PTM pin14 IC11
STE pin17 IC11
IRQ pin9 IC21
D0-7
STS pin9 IC13
ATRQ OUT pin13 IC7
EPR pin7 IC11
CLK pin13 IC13
SYSCLK*a29 PL1
c22 PL1 SYSRST*
Date Drawn March '85 Glenys
Version 1 1 1 1
Issue 1 2 3 4 5
Date 850328 860609 860612 870520 871125
Date Checked 25 March 85 Mike
Date Approved


Drawing No J70
Title SC09
Sheet 2 of 2
Arcom CONTROL SYSTEMS LTD
This copy for
Date Approved
Date Checked
Date Drawn
Version
Issue
Date
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SYSRST*
RW
+vSTBY
+5v
A0-19
DATSTB*
ADRSTB*
CM2
CM0
CM1
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
IC1
IC2
IC3
IC5
IC11
IC12
IC15
IC17
IC18
IC19
IC20
IC21
IC22
IC4
IC7
IC13
P2
P3
J1
J2
J4
J5
J9
J11
J12
J13
J14
J15
J16
J17
J18
J19
J20
J21
J22
R1
R2
R12
C3
C4
RW0
WE
D0-7
VMA
ENDR
PTM
STE
EPR IC23
CLK13
STS
BRST
CS
IRQ
E
DATACK*
TRFERR*
ATRQ OUT
ATNRQ0*
ATNRQ1*
ATNRQ2*
ATNRQ3*
toJ6
toJ6
SYSCLK*
BUSRQ0*
BUSRQ1*
BUSAK0*
BUSAK1*
Date 25 March '85
Drawn
Checked Mike
Approved
870520
860612
860609
850328
871125