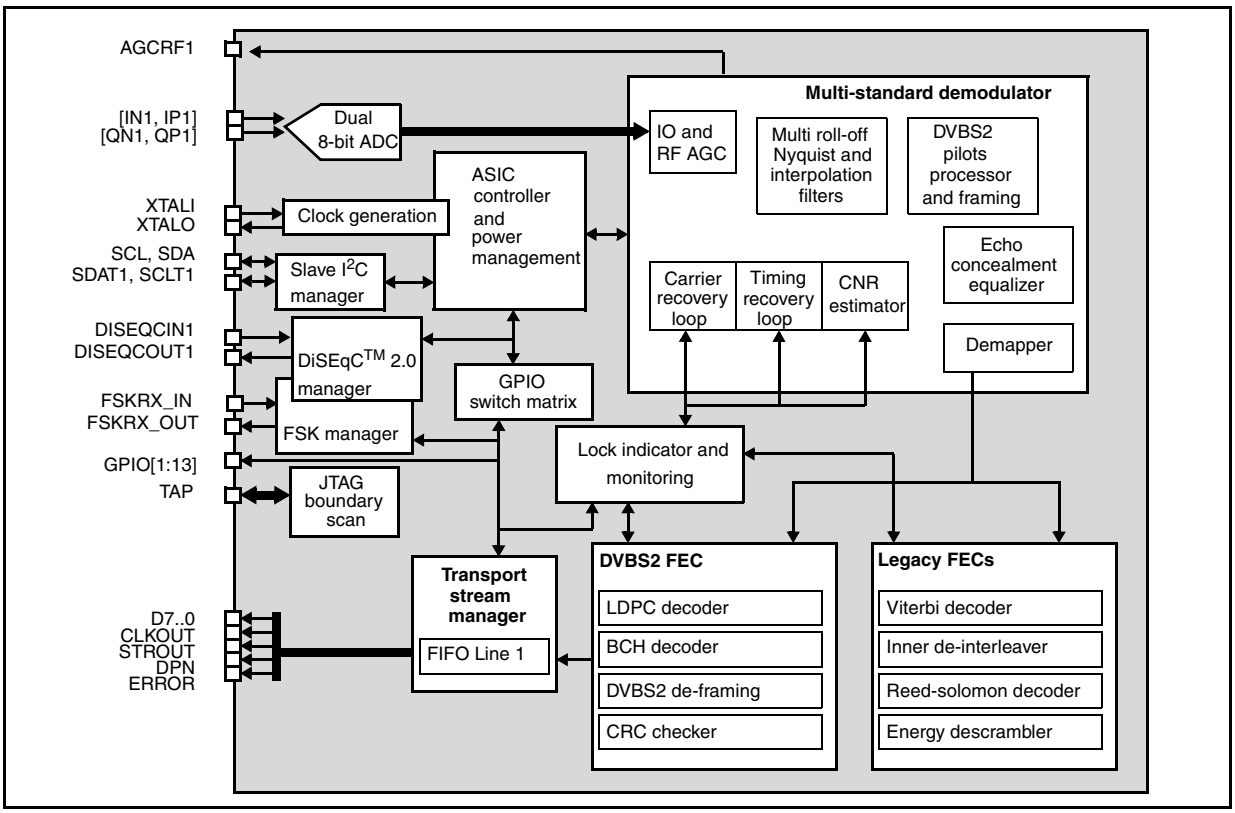
STV0903BAC

Multi-standard advanced demodulator for satellite digital TV set-top boxes

Features

- Multi-standard demodulation
  - Legacy DVBS and DirecTV™ QPSK
  - DVBS2 QPSK, 8PSK
  - Up to 45Msps DVBS, DSS, DVBS2 QPSK and 8PSK
  - Multi-tap equalizer for RF reflection removal
  - Wide range carrier frequency tracking loop for offset recovery
- Multi-standard decoding
  - DVBS or DirecTV™ legacy
  - DVBS2 FEC and framing
- Interfaces
  - Data to MPEG decoder
  - DVB common interface compliant
  - I^2C serial bus interface, including private repeater for tuner
  - JTAG interface for boundary scan
  - DiSEqC 2.x 22-kHz interfaces
  - FSK interface
  - Flexible GPIOs and interrupts
  - Bit error rate monitoring and reporting
- Technology
  - Multi supply: 1.0-V core, 2.5-V analog, 3.3-V digital interfaces
  - Power saving features
  - LQFP128-EP 14 x 14 mm^2 package, environmentally friendly



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1 Description

1.1 Overview

The STV0903 is a cost effective, high performance demodulator-decoder for advanced DVB satellite reception. The device supports DVB-S and DirecTV™ legacy transmission standards, as well as DVBS2 in QPSK and 8PSK.

The STV0903 features a high-speed DVB-S2 forward error corrector (FEC) which is designed to handle up to 190 channel-Mbit/s at its input. To feed the FEC the STV0903 implements a demodulator, capable of handling QPSK legacy and DVBS2 constant coding and modulation for satellite broadcast

The STV0903 integrates all the features needed to provide a low cost broadcast satellite receiver solution including: integrated crystal oscillator, DiSEqC controller, tuner I^2C repeater, FSK modem, ancillary DACs and ADCs and many unattributed general purpose input output ports for peripheral control.

A number of state machines and algorithms have been implemented to allow standard functions to be accessed easily and with a minimum of code overhead. Blind scan is implemented allowing an entire band to be searched automatically once a minimum of parameters have been provided. Cold and warm start acquisition and re-acquisition procedures are provided.

Advanced power saving features have been implemented, the LDPC stops once the solution is sufficiently converged and the various blocks of the IC (demodulator, LDPC, Legacy FEC etc.) may be completely shut down if not required.

A real-time constellation output is also available, allowing improved monitoring and debug during product development. Full error monitoring facilities are available and signal statistic are provided via I^2C. For example, antenna pointing may be assisted via the carrier to noise ratio metric or the electrical installation may be judged according to received RF level and equalizer tap readings (reflection intensity).

1.2 Versions

STV0903BAC - Broadcast -This Datasheet from rev F

STV0903BAB - Broadcast -This Datasheet up to rev E

1.3 Key features for broadcast applications

- Single-channel DVB-S / DVB-S2 demodulator/decoder
- Demodulator:
  - Two 8-bit ADCs
  - One ΣΔ digital RF AGC
  - QPSK, 8PSK
  - CCM
  - Automatic detection and configuration of:
  a) Modulation type
  b) Filter roll-off
  c) Symbol rate
  d) Pilot presence (on/off)
  e) Short or long frames (long frames only)
  - Cold or warm start
  - Blind recovery of symbol and carrier frequency
- Forward error correction:
  - Viterbi and reed-solomon dual decoder (DVBS)
  - LDPC + BCH dual decoder (DVBS2)
  - Error monitoring
- Transport stream interface:
  - Parallel or serial TS interface
  - Transport bit rate automatic regulation corresponding to transport clock
  - DVB common interface compliant
- DiSEqC 2.0 interface
- FSK interface
- I^2C repeaters
- JTAG interface.

The STV0903 has been extensively validated for the broadcast operating range of 1 to 45 Msymb/s in DVB-S2 (QPSK and 8PSK) and 1 to 62Msymb/s in DVBS (and DTV legacy). Full test results, reference designs and supporting software are provided.

For DVB-S2 the machinery exists and has been tested as functional from below 1 Msymb/s and up to the rates given in the table below.

Table 1. Maximum symbol rate limitations

Modulator	Msymb/s			
	Demod	LDPC	Theoretical	Design rating
QPSK	67.5	95	67.5	45
8PSK	67.5	63	63	45

Table 2. Transport stream output limitations

(with 50% duty cycles)	TS clock (MHz)	Max data rate (Mbit/s)
Single parallel	135/4=33.75	270
Serial (Div 1)	135	108
Serial (Div 2)	67.5	54

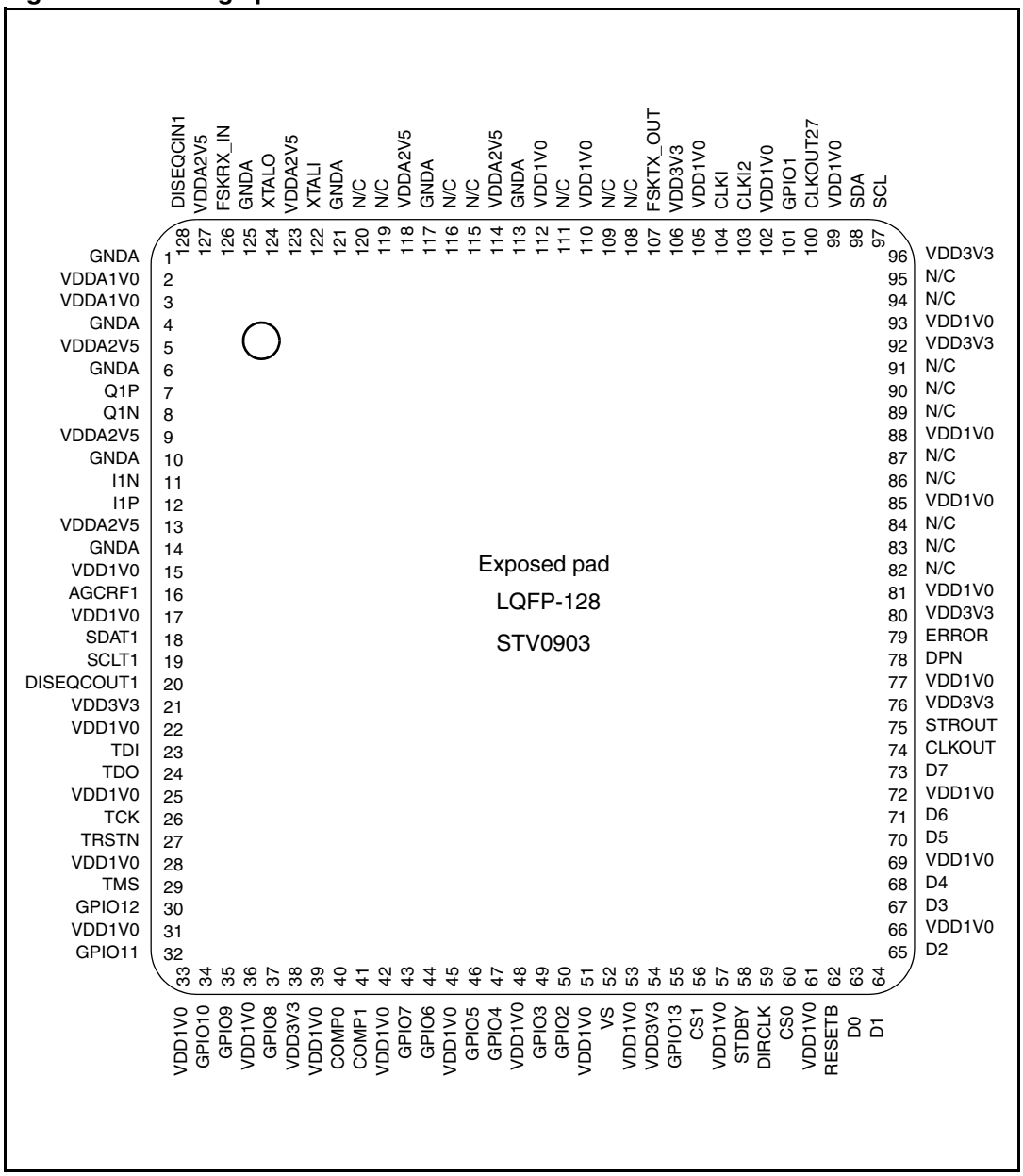
Table 3. DVB-S2 profile implemented and supported for the broadcast market

System configuration	Case	Supported
QPSK	1/4, 1/3, 2/5	No
	1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10	Yes
8PSK	3/5, 2/3, 3/4, 5/6, 8/9, 9/10	Yes
16APSK	2/3, 3/4, 4/5, 5/6, 8/9, 9/10	No
32APSK	3/4, 4/5, 5/6, 8/9, 9/10	No
CCM		Yes
VCM		No
ACM		No
FECFRAME(normal)	64800 (bits)	Yes
FECFRAME(short)	16200 (bits)	No
Single transport stream		Yes
Multiple transport stream		Yes
Single Generic Stream		Yes
Multiple generic stream		Yes
Combined single generic & single TS		Yes
Roll-off	0,35 0,25 0,20	Yes
ISSYI (input stream synchronizer)		Yes
Null packet deletion		No
Dummy frame insertion		Yes
RCS Specific		
SOF & NCR synchronization		No

2 Pin information

2.1 Pin connections

Figure 1. Package pin out



2.2 Pin description

Table 4. Pin list

Number	Name	Type	Voltage	Description / Comment
EPAD	GND	Ground	0	Digital core ground
1	GNDA	Ground	0	DiSEqC, FSK and Oscillator analog ground
2	VDDA1V0	Supply	1.0	DiSEqC, FSK and Oscillator analog supply
3	VDDA1V0	Supply	1.0	PLL analog supply
4	GNDA	Ground	0	PLL analog ground
5	VDDA2V5	Supply	2.5	PLL analog supply
6	GNDA	Ground	0	PLL analog ground
7	Q1P	Analog	-	ADC1 quadrature phase signal
8	Q1N	Analog	-	ADC1 quadrature phase signal
9	VDDA2V5	Supply	2.5	ADC1 analog supply
10	GNDA	Ground	0	ADC1 analog ground
11	I1N	Analog	-	ADC1 in phase signal
12	I1P	Analog	-	ADC1 in phase signal
13	VDDA2V5	Supply	2.5	ADC1 analog supply
14	GNDA	Ground	0	ADC1 analog ground
15	VDD1V0	Supply	1.0	Digital core supply
16	AGCRF1	I/O	3.3	Control signal for external AGC1
17	VDD1V0	Supply	1.0	Digital core supply
18	SDAT1	I/O	3.3	I^2C serial data repeater 1
19	SCLT1	I/O	3.3	I^2C serial clock repeater 1
20	DISEQCOUT1	I/O	3.3	DiSeqC 1 output
21	VDD3V3	Supply	3.3	Digital buffer supply
22	VDD1V0	Supply	1.0	Digital core supply
23	TDI	I	3.3	JTAG test data in
24	TDO	O	3.3	JTAG test data out
25	VDD1V0	Supply	1.0	Digital core supply
26	TCK	I	3.3	JTAG test clock
27	TRSTN	I	3.3	JTAG test reset
28	VDD1V0	Supply	1.0	Digital core supply
29	TMS	I	3.3	JTAG test mode
30	GPIO12	I/O	3.3	General purpose input output
31	VDD1V0	Supply	1.0	Digital core supply
32	GPIO11	I/O	3.3	General purpose input output

Table 4. Pin list

Number	Name	Type	Voltage	Description / Comment
33	VDD1V0	Supply	1.0	Digital core supply
34	GPIO10	I/O	3.3	General purpose input output
35	GPIO9	I/O	3.3	General purpose input output
36	VDD1V0	Supply	1.0	Digital core supply
37	GPIO8	I/O	3.3	General purpose input output
38	VDD3V3	Supply	3.3	Digital buffer supply
39	VDD1V0	Supply	1.0	Digital core supply
40	COMP0	Ground	0	IO reference compensation - ground
41	COMP1	Supply	-	IO reference compensation - Rext
42	VDD1V0	Supply	1.0	Digital core supply
43	GPIO7	I/O	3.3	General purpose input output
44	GPIO6	I/O	3.3	General purpose input output
45	VDD1V0	Supply	1.0	Digital core supply
46	GPIO5	I/O	3.3	General purpose input output
47	GPIO4	I/O	3.3	General purpose input output
48	VDD1V0	Supply	1.0	Digital core supply
49	GPIO3	I/O	3.3	General purpose input output
50	GPIO2	I/O	3.3	General purpose input output
51	VDD1V0	Supply	1.0	Digital core supply
52	VS	O	-	Digital core voltage sense
53	VDD1V0	Supply	1.0	Digital core supply
54	VDD3V3	Supply	3.3	Digital buffer supply
55	GPIO13	I/O	3.3	General purpose input output
56	CS1	I/O	3.3	Chip select for address selection
57	VDD1V0	Supply	1.0	Digital core supply
58	STDBY	I/O	3.3	Chip standby
59	DIRCLK	I/O	3.3	Chip clock path selection
60	CS0	I/O	3.3	Chip select for address selection
61	VDD1V0	Supply	1.0	Digital core supply
62	RESETB	I	3.3	Chip reset
63	D0	I/O	3.3	Transport stream data 0
64	D1	I/O	3.3	Transport stream data 1
65	D2	I/O	3.3	Transport stream data 2
66	VDD1V0	Supply	1.0	Digital core supply
67	D3	I/O	3.3	Transport stream data 3

Table 4. Pin list

Number	Name	Type	Voltage	Description / Comment
68	D4	I/O	3.3	Transport stream data 4
69	VDD1V0	Supply	1.0	Digital core supply
70	D5	I/O	3.3	Transport stream data 5
71	D6	I/O	3.3	Transport stream data 6
72	VDD1V0	Supply	1.0	Digital core supply
73	D7	I/O	3.3	Transport stream data 7
74	CLKOUT	I/O	3.3	Transport stream clock out
75	STROUT	I/O	3.3	Transport stream sync
76	VDD3V3	Supply	3.3	Digital buffer supply
77	VDD1V0	Supply	1.0	Digital core supply
78	DPN	I/O	3.3	Transport stream data parity
79	ERROR	I/O	3.3	Transport streamerror
80	VDD3V3	Supply	3.3	Digital buffer supply
81	VDD1V0	Supply	1.0	Digital core supply
82	N/C			Not connected - must be open circuit on board
83	N/C			Not connected - must be open circuit on board
84	N/C			Not connected - must be open circuit on board
85	VDD1V0	Supply	1.0	Digital core supply
86	N/C			Not connected - must be open circuit on board
87	N/C			Not connected - must be open circuit on board
88	VDD1V0	Supply	1.0	Digital core supply
89	N/C			Not connected - must be open circuit on board
90	N/C			Not connected - must be open circuit on board
91	N/C			Not connected - must be open circuit on board
92	VDD3V3	Supply	3.3	Digital buffer supply
93	VDD1V0	Supply	1.0	Digital core supply
94	N/C			Not connected - must be open circuit on board
95	N/C			Not connected - must be open circuit on board
96	VDD3V3	Supply	3.3	Digital buffer supply
97	SCL	I/O	3.3	I^2C serial clock
98	SDA	I/O	3.3	I^2C serial data
99	VDD1V0	Supply	1.0	Digital core supply
100	CLKOUT27	I/O	3.3	Clock loop through
101	GPIO1	I/O	3.3	General purpose input output
102	VDD1V0	Supply	1.0	Digital core supply

Table 4. Pin list

Number	Name	Type	Voltage	Description / Comment
103	CLKI2	I/O	3.3	Optional clock input 2 (not for operating modes)
104	CLKI	I	3.3	Optional clock input
105	VDD1V0	Supply	1.0	Digital core supply
106	VDD3V3	Supply	3.3	Digital buffer supply
107	FSKTX_OUT	I/O	3.3	FSK modem output
108	N/C			Not connected - must be open circuit on board
109	N/C			Not connected - must be open circuit on board
110	VDD1V0	Supply	1.0	Digital core supply
111	N/C			Not connected - must be open circuit on board
112	VDD1V0	Supply	1.0	Digital core supply
113	GNDA	Ground	0	Analog ground
114	VDDA2V5	Supply	2.5	Analog supply
115	N/C			Not connected - must be open circuit on board
116	N/C			Not connected - must be open circuit on board
117	GNDA	Ground	0	Analog ground
118	VDDA2V5	Supply	2.5	Analog supply
119	N/C			Not connected - must be open circuit on board
120	N/C			Not connected - must be open circuit on board
121	GNDA	Ground	0	Oscillator analog ground
122	XTALI	Analog	-	Oscillator in
123	VDDA2V5	Supply	2.5	Oscillator analog supply
124	XTALO	Analog	-	Oscillator out
125	GNDA	Ground	2.5	DiSEqC analog ground
126	FSKRX_IN	Analog	-	FSK modem input
127	VDDA2V5	Supply	2.5	DiSeqC analog supply
128	DISEQCIN1	Analog	-	DiSeqC 1 input

3 I²C interface

3.1 Introduction

The I²C implementation in the STV0903 follows the *I²C bus specification, version 2.1, January 2000* as edited by Philips Semiconductors.

The STV0903 internal registers have widths of 8 to 64 bits which are accessed using a device master address of 8 bits combined with an internal address of 16 bits.

3.2 I²C chip addresses

The four I²C (device master) addresses are chosen as shown in *Table 5*.

CS0 and CS1 refer to the logic levels applied to the pins CS0 and CS1 at power up or after recovering from a reset.

Table 5. I²C addresses

Access mode	CS1 / CS0			
	0/0	0/1	1/0	1/1
Write	D0	D2	D4	D6
Read	D1	D3	D5	D7

3.3 Identification register

The identification register (*MID*) allows the release version of the IC to be established through the I²C bus:

- IC with release 1.0 returns a value of 0x10
- IC with release 2.1 returns a value of 0x21.

3.4 Register access

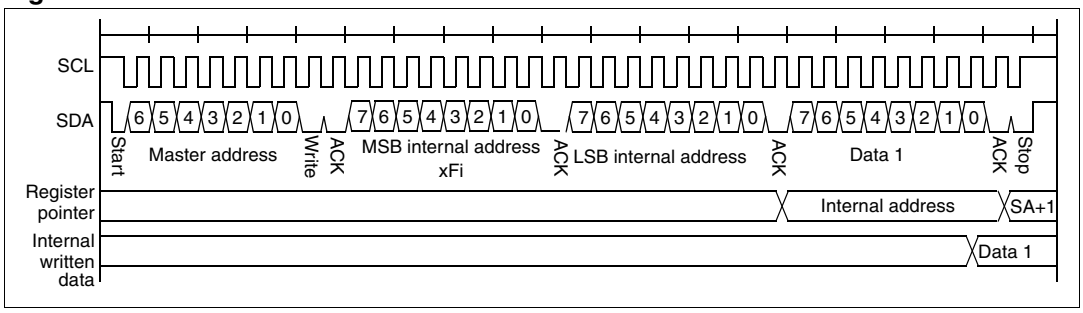
The internal address is passed on a 2-byte field of 16 bits.

3.4.1 Write operation

The byte sequence is:

1. The first byte gives the device master address plus the direction bit (RW = 0).
2. The second byte contains the most significant part of the internal address of the first register to be accessed.
3. The third byte contains the least significant part of the internal address of the first register to be accessed.
4. The next byte is written in the internal register. Following bytes (if any) are written in successive internal registers.
5. The transfer lasts until stop conditions are encountered (SDA and SCL high).
6. The STV0903 acknowledges every byte transfer. The I²C controller puts the SDA line into high impedance after each byte transmitted and the STV0903 drives the line low to acknowledge reception.

Figure 2. 16-bit address write access



3.4.2 Read operation

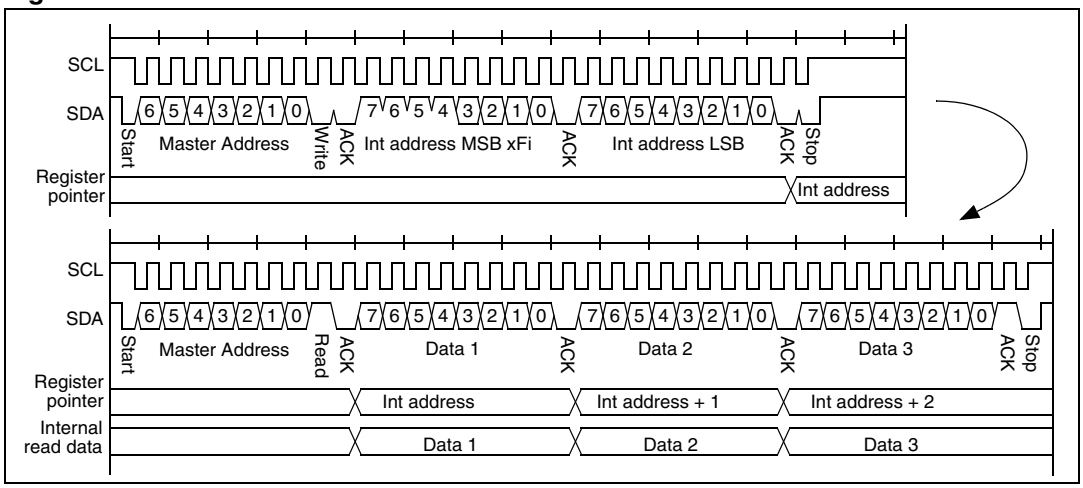
The address of the first register to be read is programmed in a write operation without data. This positions the internal pointer:

1. The first byte gives the device master address plus the direction bit (RW = 0).
2. The second byte contains the most significant part of the internal address of the first register to be accessed.
3. The third byte contains the least significant part of the internal address of the first register to be accessed.
4. A STOP is then sent.

A new start is then followed by the device master address and RW = 1. All following bytes are now data read at successive positions starting from the last write internal address.

5. The first byte gives the device master address plus the direction bit (RW = 1).
6. The second byte is the first byte of data read out (The I²C controller is in high impedance state and the STV0903 drives the SDA line).
7. Subsequent bytes are then read out until a STOP is reached.

Figure 3. 16-bit address read access



3.4.3 Example

Object: to write to device D0, registers F300 to F303 with AA, BB, CC, DD.

CS0 and CS1 are held low, which, from *Table 5*, dictates a write address of D0 and a read address of D1.

Figure 4. Example of normal mode read and write operation

Write registers F300 to F303 with AA, BB, CC, DD and I²C chip address 0xD0

Start	Device addr D0	ACK	Reg addr F3	ACK	Reg addr 00	ACK	Data 0xAA	ACK	Data 0xBB	ACK	Data 0xCC	ACK	Data 0xDD	ACK	Stop

Read registers F302 and F303

Start	Device address, write 0xD0	ACK	Register addr 0xF3	ACK	Register addr 0x02	ACK	Stop
Start	Device address, read 0xD1	ACK	Data read 0xCC	ACK	Data read 0xDD	ACK	Stop

3.4.4 Advanced modes

The I²C bus transactions (clock and data) are oversampled to ascertain their true logic values in a robust manner. The oversampling rate may be varied depending on design goals (rapidity vs. robustness). The fast mode is selected when register bit *I2CCFG*.I2C_FASTMODE is set to high, in this mode a bit is detected using an average of 16 samples. When I2C_FASTMODE is low, averaging is over 41 samples. The sample rate is M_clk (default 135 MHz)

The transactions given in the examples above were made using the address pointer increment set to +1. This is useful for reading or writing to banks of consecutive registers. For DiSEqC FIFO and other similar transactions it may be useful to set the increment to zero thereby accessing the same register each read or write cycle. Bit *I2CCFG*.I2CADDR_INC controls this function.

3.5 Standby mode

In standby modes, the I²C bus stays active and the chip can still be awakened by I²C write in the *SYNTCTRL*.STANDBY register field (see *Section 4.4.2: Standby on page 25*).

3.6 I²C bus repeater

The STV0903 integrates an I²C bus repeater. It, by default, use pins SDAT1 and SCLT1 though any of the GPIO pins can be configured for the function. See *Chapter 11: General purpose I/O (GPIO) on page 60*.

In some applications, signal pollution generated by the SDA/SCL lines of the I²C bus may significantly degrade tuner performance. To avoid this problem, the STV0903 offers an I²C bus repeater so the SDAT-SCLT1 are activated only when necessary and muted otherwise. They are configurable by the register *I2CRPT*.

Both SDAT and SCLT pins are set to high impedance at reset. When the microprocessor writes 1 into register bit *I2CRPT*.I2CT_ON, the next I²C message on SDA and SCL is repeated on the SDAT and SCLT pins respectively. There are two options for controlling I²C bus transactions (selectable through *I2CRPT*.STOP_ENABLE). The first (STOP_ENABLE high) causes the I²C repeater to turn off automatically as soon as the next stop bit is encountered. Any size of byte transfer is allowed, regardless of the address, until the stop conditions are detected. If STOP_ENABLE is low the exchanges on the main I²C bus continue to be forwarded on to the I²C repeater bus until the I2CT_ON bit is set low.

To write to the tuner, the external microprocessor must perform the following sequence for each tuner message:

1. Program 1 in *I2CRPT*.I2CT_ON to enable messages to be carried from main I²C bus to the repeater.
2. Send the message to the tuner.
3. If STOP_ENABLE was set high then I2CT_ON will automatically be set to zero on the first stop signal encountered (turning off the I²C repeater); no further action is necessary. If I2CT_ON was low then I2CT_ON must be programmed to zero to disable the repeater line.

Transfers are fully bidirectional. The *I2CRPT*.STOP_SDAT2SDA bit allows return messages from the tuner to be blocked from propagating to the main I²C bus.

The I²C bus repeater is a bidirectional bus. As such the conditions for oscillation on the SDAT line exist. In order to overcome this a sophisticated circuit requiring some tuning has been implemented to allow fast I²C bus transactions without oscillation.

The stability of the I²C repeater depends strongly on residual capacitance and thus on the board layout and may vary from tuner to tuner. Consult tuner datasheet for maximum allowable rise times on I²C bus lines. R, C values may need to be adjusted accordingly.

Stability is obtained by introducing a programmable delay in the SDA line. The same delay may also be introduced in the SCL line if necessary (though not for reasons of stability).

The sampling period is controlled via register *I2CRPT* fields ENARPT_LEVEL and SCLT_DELAY. ENARPT_LEVEL sets the division ratio which controls the delay inserted on the SDAT line. SCLT_DELAY activates the same delay on the SCLT line; this makes the delay equal on both SDAT and SCLT but implements the delay with respect to the main I²C bus.

It is advised to vary empirically the ENARPT_LEVEL around the recommended value to ensure stability in the final application. If further support is required please contact ST field application engineers.

The START, ACK and STOP conditions must be respected.

START condition:

SDA must fall a half clock period prior to SCL falling.

Data: 8-bit data are presented on SCL falling edge and read in (to the tuner) on SCL rising edge.

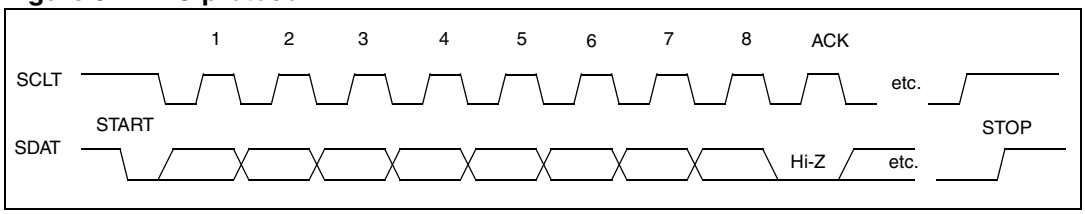
ACK condition:

A ninth SCL pulse with SDA set high-Z is sent. The master then reads that the line has been pulled low by the tuner to complete the acknowledge.

STOP condition:

SCL must rise a half clock period prior to SDA rising.

Figure 5. I²C protocol



If for any reason the master detects the SDA rising whilst SCL is high the transaction will be aborted.

If not used for the I²C repeater, both SDAT and SCLT can be used as general purpose input/output ports. See *Chapter 11: General purpose I/O (GPIO) on page 60*.

4 Clock generation

4.1 Frequency synthesis

The internal clocks are generated by a PLL. The PLL is based on a charge pump, phase detector and VCO which takes its reference from either the XTALI pin of the internal oscillator (normally fed from the tuner reference clock) or the CLKI pin. The CLKI pin is an ancillary clock input (not advised in normal applications).

The default reference frequency is 27 MHz; all electrical characteristics in the specification are specified only for this frequency.

ST does not guarantee electrical performance at clock frequencies other than 27 and 30 MHz, however some flexibility does exist should conditions require it. The frequency for this reference must be in the range 4 to 30 MHz.

The PLL operating frequency is given by the equation:

$$f_{pll} = f_{xtal} * (MDIV + 1)$$

Where f_{xtal} is the crystal oscillator frequency and MDIV are the field bits of register *NCOARSE* register. The output dividers of the PLL can also be changed; this may be useful when low symbol rates are required or very low power operation. The selection is done by the bit SELX1RATIO of the register *SYNTCTRL*.

Table 6 summarizes recommended MDIV values for best performance. Programming MDIV out of these ranges is allowed but will degrade the PLL performance.

Table 6. MDIV recommended values

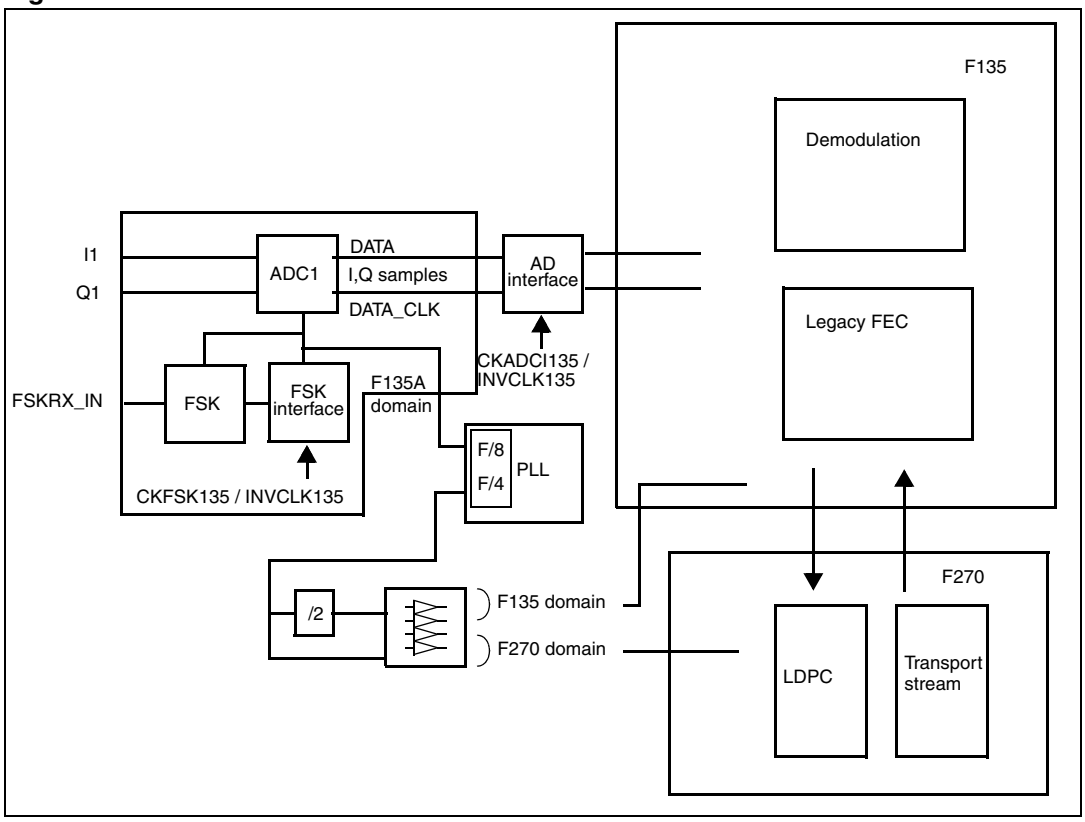
Quartz frequency (MHz)	Minimum F / 6 = 140 MHz F / 12 = 70 MHz	Typical F / 4 = 270 MHz F / 8 = 135 MHz	Maximum F / 4 = 284 MHz F / 8 = 142 MHz
27	SELX1RATIO = 0 MDIV = 0x1E	SELX1RATIO = 1 MDIV = 0x13	SELX1RATIO = 1 MDIV = 0x29

Clock domains

There are three clock domains in the STV0903:

- F270 is used by the transport stream, the LDPC decoder and its interfaces.
- F135A is used in the clocked analog blocks (ADCs and FSK). This clock stays in the analog part of the chip to ensure better noise immunity.
- F135 is used everywhere else for:
  - demodulation
  - legacy forward error correction
  - I^2C register control.

Figure 6. Clock domains



Power management

Separating the clock tree into several distinct blocks allows advanced power management features to be used. Through the *STOPCLK1* and *STOPCLK2* registers, clock domains can be activated or shut down as required.

4.2 Starting PLL, power up sequence

Configure pins:

DIRCLK = 0: clock is taken from XTALI. This activates the internal oscillator circuitry, the reference clock is taken from XTALI and routed to the PLL. The PLL is active and generates the appropriate internal clocks.

STANDBY = 1: starts with PLL and clock off but I^2C interface active. The I^2C operates with a sample clock frequency of f = f(XTALI).

Then RESETB should transit from low to high (at least 3 ms after last power supply has stabilized).

The clock registers (such as NCOARSE) should be configured and the demodulator disabled in software. An appropriate start up sequence is given in the low level application drivers.

Finally set STANDBY = 0, this starts the PLL and switches on the clocks. The preprogrammed register values take effect. The I^2C sample rate is now governed by Mclk.

4.3 Starting PLL using external clock source (engineering mode)

Pin DIRCLK is set high. This turns off the internal oscillator circuitry, the reference clock is taken from CLKI and routed to the PLL. At this time the PLL is turned off and bypassed. Register *SYNTCTRL* fields BYPASSPLLCORE, BYPASSPLLAD, BYPASSPLLFSK and STOPPLL, must all be written to zero to enable the PLL and connect it to the internal clock trees.

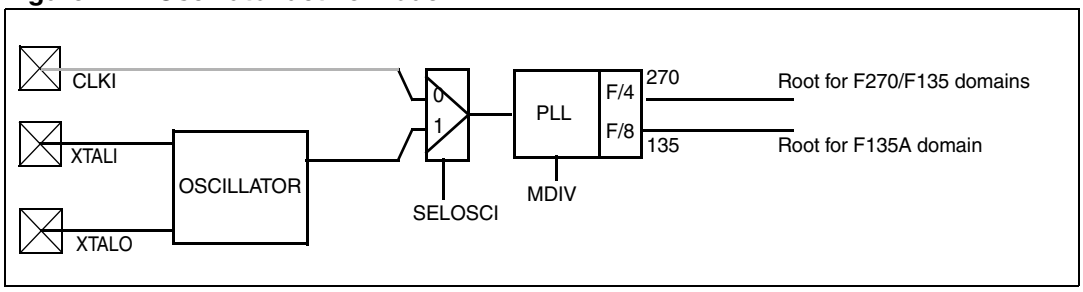
4.4 Clock sources

4.4.1 Clock source choice

The source of the reference clock is selected through register SYNTCTRL.SELOSCI. At reset and power up SELOSCI depends on the logic level on the DIRCLK pin (see *DIRCLK on page 24* for explanations).

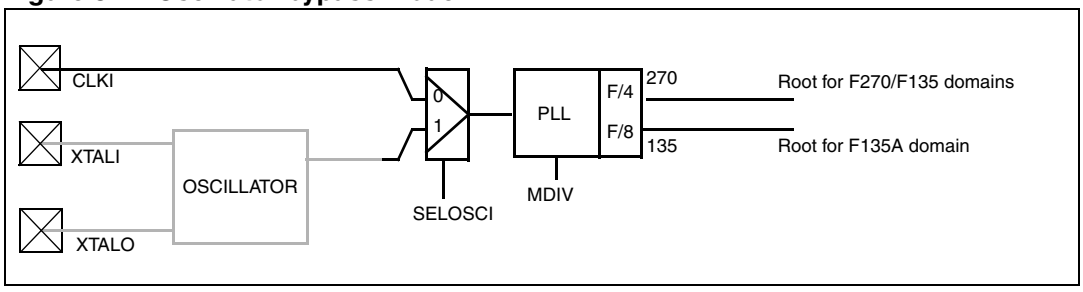
When SELOSCI is high the internal oscillator is switched on and the PLL draws its reference from this oscillator.

Figure 7. Oscillator active mode



The oscillator can be switched off and bypassed by writing zero to SELOSCI or by setting DIRCLK high and making a reset.

Figure 8. Oscillator bypass mode



PLL bypass

Two modes of bypass exists, controlled by the bit BYPASS_APPLI of register *FILTCTRL*.

- When BYPASS_APPLI = 1, the clock source is from the output of the SELOSCI multiplexer, that is, from CLKI or XTAL. The clock goes straight to the F270 clock domains and passes through a divider by 2 for the F135/F135A clock domains. This mode allows the master clock to be taken from an external source, this may be useful for very low baud rate applications. See *Figure 9*.
- When BYPASS_APPLI = 0, the F270 clock is sourced from the pin CLKI, and the F135/F135A clocks are sourced from pin CLKI2. This configuration is reserved for test purposes. See *Figure 10*.

Figure 9. PLL bypass application mode

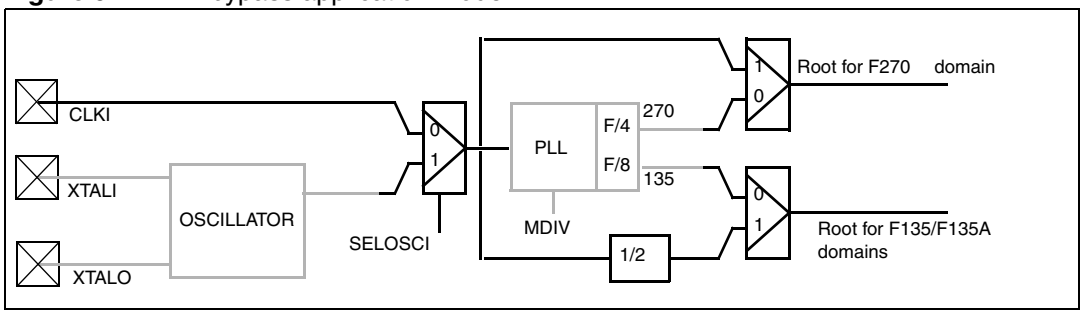
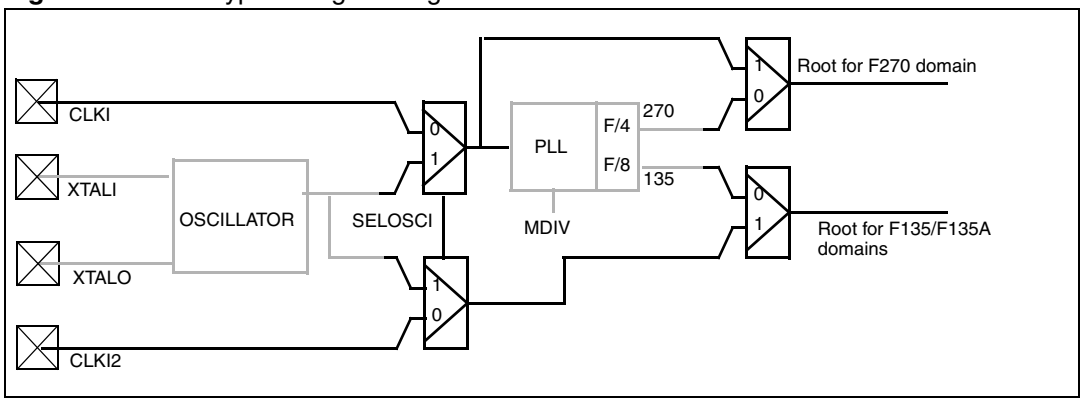


Figure 10. PLL bypass engineering mode



DIRCLK

When setting the DIRCLK pin, one of two clock paths are chosen. DIRCLK is sampled when recovering from a reset. A reset must be generated after power-up.

- When sampled as 0, the oscillator is active, the PLL is active and the clock is sourced as per *Figure 7*.
- When sampled as 1, the PLL is turned off, the oscillator is turned off, the PLL is bypassed and the clock is taken from the CLKI as a PLL bypass application mode (see *PLL bypass on page 24*). The *SYNTCTRL* register fields BYPASSPLLCORE, BYPASSPLLAD, BYPASSPLLFSK and STOPPLL, must all be written to zero to enable the PLL and connect it to the internal clock trees.

4.4.2 Standby

Standby mode permits enhanced power saving.

The device enters standby mode when:

- the device powers up and the STDBY pin is tied to VDD
- the device recovers after a reset and the STDBY pin is tied to VDD
- the STANDBY bit in *SYNTCTRL* is set using the I^2C bus.

In standby mode all the main functions are stopped except for the I^2C bus which remains active awaiting new commands. When standby mode is invoked all clocks are turned off except the I^2C clock. All pads retain their last programmed configuration. This means that any pin configured as push pull will continue to drain current. It is recommended to put the GPIOs in high-impedance state during standby.

4.4.3 Summary

Table 7 summarizes the clock control registers.

Table 7. Clock generation registers

Function	Register	Field
Stops all clocks except I^2C	*SYNTCTRL*	STANDBY
Allows external clocks to access digital clock tree		BYPASSPLLCORE
Allows external clocks to access ADCs clock tree		BYPASSPLLADC
Allows external clocks to access FSK clock tree		BYPASSPLLFSK
Turns off PLL and VCO		STOPPLL
Selects reference input between CLKI and XTALI		SELOSCI
Sets PLL division ratio	*NCOARSE*	MDIV
Selects reference input between CLKI and the couple CLKI/CLKI2	*FILTCTRL*	BYPASS_APPLI
Stop individual clock trees	*STOPCLK1*	See register description
Stop individual clock trees	*STOPCLK2*	See register description
Goes high if PLL is locked	*PLLSTAT*	PLLLOCKED
ADC interface clock inversion (debug only)	*FILTCTRL*	INVCLK135
FSK interface clock inversion (debug only)	*FILTCTRL*	INVCLKFSK

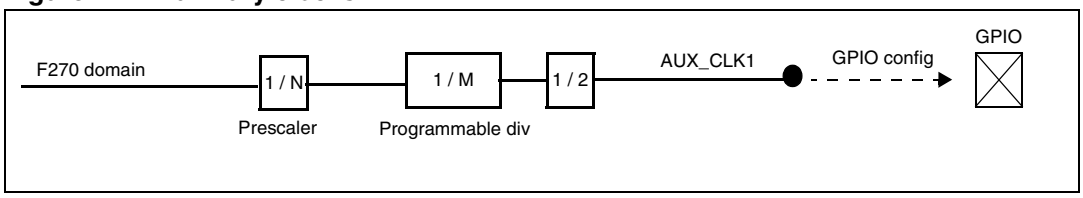
4.5 CLKOUT27

CLKOUT27 is a pin which replicates the clock generated or re-generated through XTALI. It is a GPIO port and may be reconfigured. However, reconfiguration is not recommended.

The output is designed to minimise phase noise degradation and is compatible with driving MPEG decoder ICs. This pin is active as soon as power is applied and, if it has not been reconfigured, is unaffected by a hardware (or software) reset. In this way the system is protected from entering a deadlock state and may safely be used to drive the backend decoder.

4.6 AUX_CLK

Figure 11. Auxiliary clocks



There ia a programmable auxiliary clock. The source frequency is taken from the F135 domain then prescaled, divided and gated before being output though any of the programmable GPIO pins. The prescaler register *ACRPRESC* controls the prescaler.

Programmable divider

Table 8. Prescaler ratios

Prescaler code (ACR_PRESC)	Division ratio (presc_div_ratio)
000	Reserved
001	2
010	16
011	128
100	1024
101	8192
110	65536
111	524288

Table 9. Divider ratios

Divider code (ACR_DIV)	Main divider (main_div_ratio)
0x00	256
0x01	1
0x02	2
...	...
0xFC	252
0xFD	253
0xFE	254
0xFF	255

Register *ACRDIV* field 7:0 is used for AUX_CLK1.

f_{aux} = F135 / (*presc_div_ratio * main_div_ratio*)

Frequencies in the range 1 kHz to 135 MHz are achievable.

5 Demodulation

The demodulator block performs QPSK and 8PSKdemodulation according to DVB-S, legacy DirecTV^{TM} and DVB-S2 specifications.

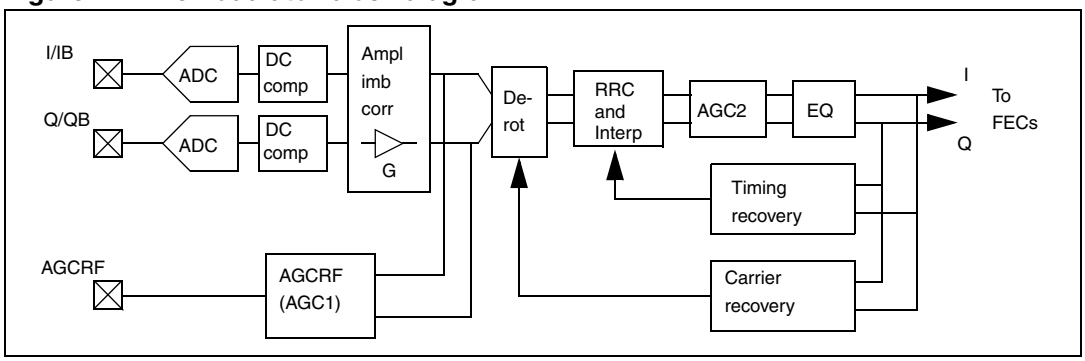
The input signal from the tuner is A-to-D converted on 8 bits. The DC offset, amplitude mismatch and quadrature error are corrected and the AGC signal level to the tuner is calculated. The carrier frequency offset is corrected. Then the signal is subsampled and Nyquist root filtered. The signal amplitude is controlled through the second stage (AGC2) block.

The headers are processed on a bloc by bloc basis, configuring the demodulator on-the-fly and giving the FEC information appropriate to the coding scheme. The pilots, when present, are used to help phase lock to the symbol stream. The signal is equalized, descrambled, and passed to the FEC.

An internal state machine controls the automatic acquisition of a channel with various entry points, including warm start (known symbol frequency, small carrier offset), cold start (known symbol frequency and large carrier frequency offset), and blind search (all parameters unknown).

It is possible to observe the internal IQ signal constellation with *ISYMB* and *QSYMB* controlled by *IQCONST*.IQSYMB_SEL.

Figure 12. Demodulator block diagram



5.1 ADCs

The channel is digitally converted with an 8 bit dual ADC, working at least twice the symbol frequency, typically at 135 MHz.

The input is typically 2 V p-p differential for STB6100 tuner and 1Vp-p for STV6110A tuner.

5.2 DC offset compensation, IQ mismatch and quadrature error correction

The applied DC offset correction may be read in register bits *IDCCOMP*.IAVERAGE_ADJ and *QDCCOMP*.QAVERAGE_ADJ. The maximum correction range is ±63 LSBs.

The bitfield*AGC1AMM*.AMM_VALUE represents the value of the amplitude mismatch, and*AGC1QUAD*.QUAD_VALUE quadrature error angle.

The amplitude correction capability is ±3.5 dB, and the angle correction capability is ± 14 degrees. The amplitude correction applied is Q = I * (1 - alpha) where -0.5 < alpha < +0.5. Alpha corresponds to the signed value of AMM_VALUE. The corrections are applied to the RMS average.

These correction functions may be controlled through register *AGC1CFG on page 117*:

- DC compensation: bits DC_FROZEN and DC_CORRECT
- amplitude compensation: bits AMM_FROZEN and AMM_CORRECT
- quadrature compensation: bits QUAD_FROZEN and QUAD_CORRECT.

For each function, there are 3 possible modes:

- no correction
- frozen (parameter updating stopped but correction still applied)
- running (normal mode, reset default state).

5.3 AGC1 tuner level control

The tuner AGC reference value is set via *AGC1REF*.AGCIQ_REF. This field represents the magnitude of the signal on 8 unsigned bits.

AGCIQ_REF = sqrt((I^2 + Q^2)/2)

The AGC time constant is set via *AGC1CN*.AGCIQ_BETA, legal values are 1 (slowest) to 7 (fastest); 0 freezes the operation of the loop, that is, stops the AGC value from being updated (useful during debug).

The gain may be read in registers *AGCIQIN0* and *AGCIQIN1* (16 bits).

The AGC polarity may be inverted through the two registers *AGCRF1CFG*.

The output is pulse density modulated, and must be externally filtered with an appropriate low-pass filter before driving the tuner AGC input.

5.4 Spectrum inversion

In order to facilitate hardware design, the IQ spectrum may be inverted at the input of the IC. This is useful for correcting IQ signal inversions between the tuner and STV0903. For example:

- *TMGCFG*.TUNER_IQSWAP = 1 (swapped)
- *TMGCFG*.TUNER_IQSWAP = 0 (no correction applied).

When demodulating DVBS2 signals, spectrum inversion is automatically managed by the control state machine. The state of the spectrum inversion may be interrogated via *PLHMODCOD*.SPECINV_DEMOD.

When demodulating DVBS1/DirecTV signals the spectrum inversion is managed by the FEC state machine. The state of the spectrum inversion can be found by interrogating *FECM*.IQINV.

Spectrum inversion can be manually forced with*DEMOD*.SPECINV_CONTROL.

5.5 Roll-off factor

The roll-off factor may be configured automatically or programmed manually. This selection is made via Px_DEMOD.MANUALSX_ROLLOFF (1 bit) for DVB-S1 and DTV and Px_DEMOD.MANUALS2_ROLLOFF for DVB-S2

If manual mode is selected the roll-off factor selected in ROLLOFF_CONTROL is used.

If automatic mode is chosen the following happens. The roll-off is selected in ROLLOFF_CONTROL[1:0] and used during the acquisition of the signal. Once the modulation type has been resolved the Nyquist filter is automatically switched according to:

- DVB-S2, the roll-off factor is read from the MAtype field of the BBHeader and may be observed in register *MATSTR1* and *MATSTR0* and Px_TMGOBS.Px_ROLLOFF_STATUS (this is the definitive indicator).
- DVB-S, the roll-off factor is set to 35%.
- DIRECTV legacy, the roll-off factor is set to 20%.

5.6 AGC2 signal amplitude control

The AGC2 reference value is set via *AGC2REF*.AGC2_REF. This field represents the magnitude of the signal on 8 unsigned bits.

AGCIQ_REF = sqrt(I^2 + Q^2)

The AGC2 time constant is set via *AGC2I0*.AGC2_COEF, legal values are 1 (slowest) to 7 (fastest); 0 freezes the operation of the loop, that is, stops the AGC value from being updated.

The gain may be read in bit AGC2_INTEGRATOR of registers *AGC2I1*-0.

5.7 Timing loop

The timing loop core is a second order PLL controlled by two parameters, alpha and beta.

The timing loop has three states: coarse acquisition, fine acquisition and tracking. The execution through these modes when acquiring is controlled via a powerful state-machine described in *Section 5.13 on page 32*.

- Coarse acquisition: The coarse (and fine) search range may be specified in absolute frequency (manual mode) as defined in *SFRUP1*-0, (upper bound) and *SFRLOW1*-0 (lower bound). Alternatively, SFRUP and SFRLOW may be calculated (automatic mode) from *SFRINIT1*, *SFRINIT0*, SFRUPRATIO and SFRLOWRATIO. The scan mode (automatic/manual) is set in bit 7 of *SFRUP1* and *SFRLOW1*. The boundary conditions depend on the algorithm chosen, see *Section 5.13: Algorithmic entry points (AEP) on page 32*. When a border is reached, the scanning is inverted or stopped; an interrupt may be raised when this occurs.
- Fine acquisition: a scanning range is defined automatically as a result of the coarse search. The fineness or speed of the scanning is controlled by parameter *SFRSTEP*.SFR_SCANSTEP. During the initial search the DVBS alpha and beta parameters are used. The search step size is defined in register SFRINC.
- Tracking: once the modulation type has been identified the state-machine enters tracking mode loading the appropriate loop parameters. For tracking performance reasons separate alphas and betas are required for DVBS and DVB-S2. They are bits TMGALPHA_EXP and TMGBETA_EXP in registers *RTC* for DVBS/DirecTV and bits TMGALPHAS2_EXP and TMGBETAS2_EXP in registers *RTCS2* for DVBS2.

When the state-machine has achieved lock the timing offset may be found in registers *TMGREG2*, *TMGREG1*, *TMGLOCK0*.

A further function allows the timing offset to be cancelled, that is, the value in registers TMGREG2-0 is set to zero and that in registers SFR2-0 is adjusted accordingly.

5.8 Timing lock detector

The timing lock indicator (register *DSTATUS*) is a value which is maximized when the timing is locked. Once locked it is a function of the C/N ratio and the roll-off factor of the transmitted signal, thus the timing lock thresholds need adjusting to optimize lock stability.

The timing lock indicator is filtered with a programmable time constant (register bit *TMGCFG*.TMGLOCK_BETA) and is compared to two thresholds, *TMGTHRISE*.TMGLOCK_THRISE and *TMGTHFALL*.TMGLOCK_THFALL, in order to issue TMGLOCK_QUALITY[1:0], a 2-bit lock indicator with hysteresis (register *DSTATUS*).

Lock is achieved when TMGLOCK > TMGLOCK_THRISE (MSBs of TMGLOCK_QUALITY), lock loss is declared when TMGLOCK falls below TTMGLOCK_THFALL (LSBs of TMGLOCK_QUALITY).

5.9 Carrier loop

The carrier frequency and phase are corrected by a second order PLL when in tracking mode. During acquisition frequency detection is used:

The carrier loop has three states (same states as the timing loop): coarse acquisition, fine acquisition and tracking. The execution through these modes when acquiring is controlled via a powerful state-machine described in *Section 5.13 on page 32*.

- Coarse acquisition: a coarse frequency offset is identified. The speed and precision of the search is controlled via register *CARFREQ*. The limits of the coarse frequency search are defined in *CFRUP1*-0 and *CFRLOW1*-0. The search step is set in *CFRINC1*-0.
- Fine acquisition: the fine frequency offset is determined using a frequency offset detector. The timer constant of the frequency offset detector is defined in *CARFREQ*.BETA_FREQ. Once the frequency has been determined a phase tracking loop is engaged. The loop parameters are *ACLC* and *BCLC*. If a DVB-S signal is not resolved, a reading of the DVB-S2 header is conducted. The state machine then goes on to fine tune the DVB-S2 acquisition by averaging the frequency offset over many headers. The register *CARHDR*.K_FREQ_HDR controls this process.
- Tracking: for tracking performance reasons separate alphas and betas are required for DVBS and DVB-S2.
  - DVBS and DirecTV: loop coefficients are alpha on register *ACLC* and beta on register *BCLC*.
  - DVBS2: loop coefficients are alpha and beta in registers*ACLC2S2Q*, *ACLC2S28* respectively, for QPSK (data, pilots and PLHeader symbols), and 8PSK.

5.10 Carrier lock detector (DVBS/DirecTV only)

A lock indicator is provided for DVBS and DirecTV modes only. The lock indicator is based on an accumulator which is maximized when locked to a QPSK signal. The accumulator value may be found in registers *LDI*. This level depends on the current CNR as well as the lock state. Thus, settings adapted for specific code-rates may be required. This value is permanently compared to a programmable threshold set in registers *LDT* (the lock acquired threshold) and *LDT2* (the lock lost threshold). The result is given in *DSTATUS*.CAR_LOCK flag.

When the CAR_LOCK flag is set, the frequency detector is automatically disabled and the demodulator starts phase tracking.

5.11 Equalizer

An equalizer allows for the compensation of echoes on the cable, and/or imperfect channel filtering.

The equalizer converges and tracks (updates) automatically. No operator intervention is required. The equalier is divided into 2 parts DFE and FFE.The update speed of the DFE part is determined in register

Px_EQUALCFG.PX_MU_EQUALDFE. The equalizer may be switched on or off with bit Px_EQUAL_ON, or may be frozen with bitfield PX_MU_EQUALDFE = 0.

The update speed of the FFE part is determined in register Px_FFECFG.PX_MU_EQUALFFE. The equalizer may be switched on or off with bit Px_EQUALFFE_ON, or may be frozen with bitfield PX_MU_EQUALFFE = 0.

5.12 Tuner control

The favoured method of tuner operation is via external driver; ST supplied low level ‘application (LLA) drivers or STTUNER software are available on request.

The I2C repeater bus must be configured as described in *Chapter 3.6 on page 19*.

5.13 Algorithmic entry points (AEP)

The demodulator is managed by a powerful but flexible state machine. The basic method of usage is to initialize the necessary parameters and then start the state machine at the appropriate point. These starting points are known as the algorithmic entry points (AEPs).

Register field *DMDISTATE*.I2C_DEMOD_MODE is used to set the AEP which determines the type of search to be used, the material to be involved and hence the parameters that have to be initialized. Most of the initial parameters will be retained after the completion of an acquisition cycle and need only be set once. Refer to *Section 5.7: Timing loop* and *Section 5.9: Carrier loop* for setting the loop coefficients and search boundaries.

When using the state-machine the two most important parameters are:

- *CFRINIT1*-0: initial carrier offset
- *CFRINIT1*-0: initial symbol rate.

Once these parameters are set up, the acquisition may be launched by writing the appropriate AEP value to *DMDSTATE*.I2C_DEMOD_MODE.

The symbol rate search limits may be set either automatically or defined manually.

The automatic mode is invoked by default after a reset.

In automatic mode the symbol rate boundaries are expressed as a percentage of the initial symbol rate (+/- 25% at reset). The symbol rate range boundaries may be finely adjusted by programming SFRUPRATIO (0xF455) and SFRLOWRATIO (0xF456).

In manual mode the boundaries are expressed as absolute symbol rate values. Manual symbol rate search is invoked by setting *CFRUP1*:AUTO_GUP (0xF460[7]) = 0 and *SFRLOW1*:AUTO_GLOW (0xF462[7]) = 0

The hard symbol rate boundaries may then be programmed in

CFRUP1-0:SFRUP (0xF460,0xF461[14:0]) and

CFRLOW1-0:SFRLOW (0xF462,0xF463[14:0]).

The AEP (I2C_DEMOD_MODE) values:

Blind Scan

Symbol rate, carrier offset and modulation unknown; demodulator will lock to the nearest channel:

- 0x00: zero offset start:
  - Required values are *CFRINC1*-0.
  - *CFRINC1*-0 is the carrier frequency step size used in the carrier frequency search algorithm. Register *SFRINIT1*-0 is automatically loaded with the value of *CFRINC1*-0. *CFRINIT1*-0 is automatically set to zero offset at the start of the search.
  - Demodulator will then attempt to find the symbol rate, carrier offset, modulation type (DVBS2, DVBS or DirecTV) and code rate.
  - If the demodulator does not find a signal at that frequency the state-machine re-starts with a new value of *CFRINIT1*-0 and expands, with step given by register *CFRINC1*-0, from the initial frequency using a zig-zag algorithm until a signal is found or the boundaries reached. The value of *CFRINC1*-0 must be small to capture narrow channels.
- 0x01: best guess start:
  - Same as 0x00 except *CFRINIT1*-0 and *SFRINIT1*-0 are given as approximate start values.

Cold start:

Carrier offset unknown, symbol rate known:

- 0x15: zero offset start:
  - PROGRAM *SFRINIT1*-0.
- 0x05: best guess start:
  - Same as 0x15 but current SFR used as start point.

Warm start

Carrier offset known, symbol rate known:

- 0x18: zero offset start:
  - SFR and CFR are used as start point. *CFRINIT1*-0, *SFRINIT1*-0 are required to set limits.

Others

- 0xA: As per 0x18 but for DVBS1/ legacy DIRECTV only
- 0xB: As per 0x18 but for DVBS2 only
- 0x1C: demod stop
- 0x1F: reset demod state-machine
- 0x14: next channel:
  - Nothing to program before launching.
  - The demodulator finds the next channel (or preceding channel according to selected search direction). The search is linear (not zig-zag). Direction of search is given by *CFRICFG*.NEG_CFRSTEP.
- 0x11: bandwidth scan:
  - Analogue tuner bandwidth is searched for channels (useful for low symbol rates).

5.14 Results FIFO

It is possible to observe final and intermediate working results in the demodulator. After each channel is acquired, results are stacked in a FIFO (accessed by registers *DMDRESDATA7..0*). These registers contain all of the important data found by the demodulator:

- symbol rate
- carrier offset
- tuner frequency
- modulation type / code (DVBS2, DVBS or DirecTV with their roll-off, mapping, puncture rate and spectrum inversion) or tag “Undecodable Channel” (giving important data to correct any problem).

“Undecodable Channel” tag indicates that there is clearly something at this position but the demodulator could not determine its code (too much noise or unknown code). For instance, analog channels are tagged “Undecodable Channel”.

The FIFO is used by the auto-scan AEP (0x11 and 0x1B, see below) to stack its results.

There are up to 15 results (current number given by *DMDRESDATA7..0*.DMDRES_RESNBR) so, the stacked results must be regularly de-stacked.

A facility exists to pause the demodulator when the stack becomes full.

5.15 Interrupt controller

The demodulator can generate interrupt signals for the host processor for the following events:

- AGC1, AGC2, carrier offset and/or symbol rate overflow -> no signal
- no signal after coarse search (blind search)
- undecodable channel (timing lock but impossible to determine if it is a DVBS2, DVBS or DirecTV signal)
- undecodable channel (no timing lock)
- DVBS2 lock
- DVBS2 delock
- DVBS/DirecTV lock
- DVBS/DirecTV delock
- autoscan done
- carrier offset is out of *CFRUP1*-0 to *CFRLOW1*-0 limit and/or symbol rate is out of *SFRUP1*-0 and *SFRLOW1*-0 limit
- results FIFO is full
- results FIFO is almost full.

The cause of the last interrupt is given on field *DMDFLYW*.I2C_IRQVAL. Previous interrupt events are overwritten.

5.16 Noise indicators

Two methods of measuring noise are available:

- Data: measures the absolute noise on all data symbols (but not on pilots, PLHeader or DummyPL frames). This is the only relevant measurement for a DVBS/DirecTV signal. The value of the indicator is a monotonic function of the noise, and must be corrected by look-up table in the host. This method is compatible with ST legacy demodulators.
- Header: measures the noise on the pilot/header and DummyPL frames (if any). The measurement needs to be averaged over a large number of blocs to be precise. The value is directly proportional to the noise power. This method is more accurate when measuring DVB-S2 signals.

A number of methods of reading the noise value are provided. They include the raw noise magnitude, the noise power, noise normalized to the signal level and a quadratic value where the square of the noise level is ratioed with the signal power (equivalent to CNR). The measurements may be found in the following registers:

- *NOSDATAT1*-0: absolute raw noise level measured on data only
- *NOSDATA1*-0: square of the raw noise level (noise power) measured on data only
- *NOSPLHT1*-0: absolute raw noise level measured on headers only
- *NOSPLH1*-0: square of the raw noise level (noise power) measured on headers only
- *NNOSDATAT1*-0: normalized noise level (raw computed value divided by agc2_ref) measured on data only
- *NNOSDATA1*-0: normalized square of the raw noise level (noise power divided by $agc2\_ref^2$) measured on data only (CNR)
- *NNOSPLHT1*-0: normalized noise level (raw computed value divided by agc2_ref) measured on headers only
- *NNOSPLH1*-0: normalized square of the raw noise level (noise power divided by $agc2\_ref^2$) measured on headers only (CNR).

6 DVB-S forward error correction

6.1 FEC modes, status and error reporting

By default the appropriate FEC (DVB-S1 or DVB-S2) is automatically selected by the demodulator (observable and controllable by register bit *DMDCFGMD*.DVBS1_ENABLE) depending on the mode discovered during acquisition.

The viterbi decoder is configured through register *FECM*. By default it automatically switches between DVB-S and legacy DirecTV™ modes (result observed with bit DSS_DVB). This automatic feature may be disabled if bit DSS_SRCH is reset, DSS_DVB becoming the control bit. As an option (only for special uses), the sync byte search can be de-activated (with SYNCVIT) and IQ swap can be enforced (register bit *DEMOD*.SPECINV_CONTROL).

The read-only registers *VSTATUSVIT* report the viterbi status (active, locked, sporadic delock events). Register bitfields *VITCURPUN*.VIT_CURPUN report the puncture rate found. The modulation scheme is always QPSK.

Register bitfields *VERROR*.REGERR_VIT report a ratio of the average number of bit errors the viterbi decoder has found and corrected over a predefined interval. The number of bits used for averaging can be programmed through the *VAVSRVIT*.SNVIT field. A maximum mode (*VITSCALE*.VERROR_MAXMODE set) reports the maximum REGERR_VIT (register *VERROR)* value (the peak) encountered.

When decoding DirecTV legacy signals which are highly loaded by null packets (more than around 50%), a feedback from the reed-solomon decoder is invoked. This feedback may be disabled through *VITSCALE*.DIS_DTV67_FLOCK.

For information, viterbi decoder mode results (puncture rate, DVBS/DirecTV, IQ swap status) are stacked in the results FIFO of the demodulator.

6.2 Viterbi decoder

The convolution codes are generated by the polynomial G_x = 171 bytes and G_y = 133 bytes in both DVB-S and legacy DirecTV modes.

The viterbi decoder computes the metrics of the four possible paths for each symbol, proportional to the square of the euclidian distance between the received I and Q and the theoretical symbol value.

The following puncture rates have been implemented in both DVB-S and legacy DirecTV modes:

- 1/2
- 2/3
- 3/4
- 5/6
- 6/7
- 7/8.

To optimize search time the allowed rates can be enabled or disabled by programming register *PRVIT*.

Note: To minimize the viterbi search time, the puncture rates 3/4, 5/6, 7/8 can be disabled in legacy DirecTV *mode. In DVB-S mode, the puncture rate 6/7 can be disabled.*

A search algorithm acquires the puncture rate and phase, the resulting signal path error rate is compared to a programmable threshold. If it is greater than this threshold, another phase (or another rate) is tried until an acceptable error rate is obtained. Therefore the search algorithm steps through phases and puncture rates until an error rate below the threshold is found. The error threshold can be set for each puncture rate (registers *VTH12, VTH23, VTH34, VTH56, VTH67, VTH78*).

The viterbi software decision processing can be scaled through registers *KDIV12, KDIV23, KDIV34, KDIV56, KDIV67, KDIV78*. It is recommended to use the reset values unless STMicroelectronics recommends other values.

6.3 Synchronization

The DVB packet length, after inner decoding, is 204 bytes. The sync word is the first byte of each packet. Its value is 0x47, but this value is complemented (inverted) every eight packets. In the legacy DirecTV system, the packet length is 147 bytes and the sync word a constant, 0x1D.

When the puncture rate and its phase have been found, a sync word search is started. An up/down sync counter counts whenever a sync word is recognized with the correct timing, and counts down during each missing sync word. This counter is bounded by a programmable maximum (register bitfield *VAVSRVIT*.HYPVIT). When this value is reached, bit *VSTATUSVIT*.LOCKEDVIT is set. When the event counter counts down to 0, this flag is reset.

The time-out period for this sync word search is selectable through register bitfield *VAVSRVIT*.TOVVIT.

This lock definitively locks the demodulator.

6.4 Convolutive de-interleaver

In DVBS mode, the convolutive de-interleaver is 17 x 12. The period of 204 bytes per sync byte is retained. In the legacy DirecTV system the convolutive de-interleaver is 146 x 13, and also a period of 147 bytes per sync byte. The de-interleaver can be bypassed (see register bit *TSSTATEM*.TSDIL_ON).

6.5 Reed-solomon decoder and descrambler

The input blocks are 204 bytes long with 16 parity bytes in DVB mode. The sync byte is the first byte of the block. Up to eight byte errors can be fixed.

The code generator polynomial is:

$$g(x) = (x - \omega^0)(x - \omega^1)...(x - \omega^{15})$$

over the galois field generated by:

$$x^8 + x^4 + x^3 + x^2 + 1 = 0$$

Energy dispersal descrambler (DVBS only) and output energy dispersal descrambler generator:

$$x^{15} + x^{14} + 1$$

The polynomial is initialized every eight packets with the sequence 100 1010 1000 0000. The sync words are unscrambled. The descrambler activity is controlled by register bit *TSSTATEM*.TSDESCRAMB_ON. Descrambler is activated (or de-activated) only if the regular presence of an inverted sync word each 8 packets is detected.

The reed-solomon decoder correction is controlled through bit *TSSTATEM*.TSRS_ON.

Finally the demodulated and decoded data is presented to the transport stream manager.

7 DVB-S2 forward error correction

7.1 Introduction

This block includes three main functions:

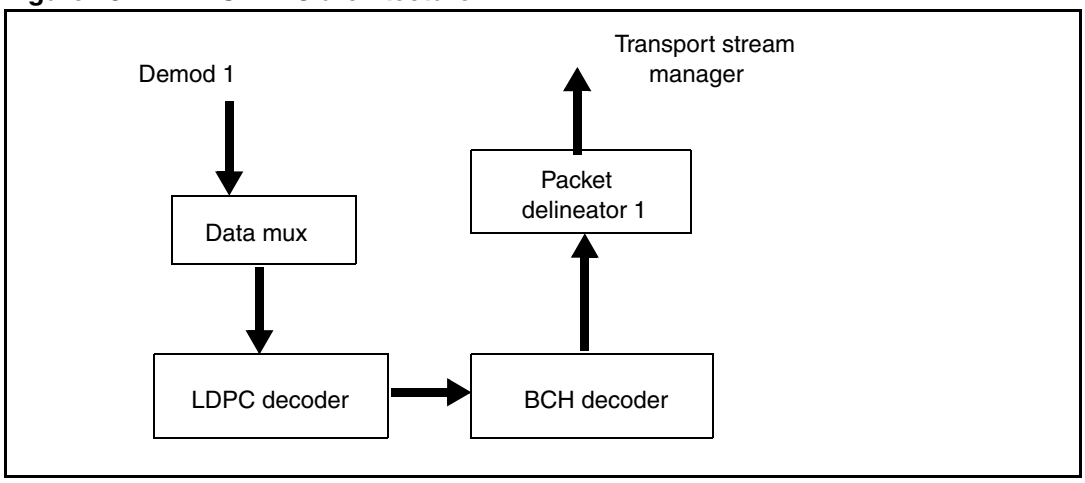
- LDPC decoder
- BCH decoder
- packet delineator.

The DVBS2 LDPC/BCH decoder has an input interface and a single output interface. The data coming from the single demodulator is multiplexed and decoded by the LDPC engine. After decoding, the packet delineator does DVBS2 de-framing before sending data to the output transport stream manager.

The architecture is such that, for a given clock frequency, the maximum input bandwidth is equal to, approximately, 70% of the clock frequency, in bits/s. Thus, for a 270 MHz clock, we may present a maximum of 190 Mbit/s at the entry of the FEC decoder.

7.2 Architecture

Figure 13. DVB-S2 FEC architecture



7.3 Features summary

- LDPC/BCH decoder

  The DVB-S2 FEC block can decode an input stream. When a frame is ready, it is processed in the LDPC decoder, then in the BCH decoder and finally output to the transport stream.
- LDPC decoder

  The LDPC decoder can decode normal frames (normal frame = 64800 bits) and 8 code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10).
- BCH decoder

  In addition the BCH decoder is able to correct up to 12 bits for code rates where more than 192 redundancy bits are available. As such, correction is only possible up to 10 bits for 2/3 and 5/6 code rates, and only up to 8 bits for 8/9 and 9/10 code rates.
- Packet delineator

  The packet delineator is used for descrambling, checking the integrity of BBFrame headers, processing the cache and data fields and providing a lock indicator.

7.3.1 Single input functional description

- normal FEC frame (64800 bits) with 11 different code rates
- de-interleaving on 8PSK, with inversion for 8PSK 3/5
- bit rate up to 190 Mbit/s.

7.4 LDPC/BCH decoder

This FEC is capable of decoding DVB-S2 CCM signals. It performs:

- bit de-interleaving
- inner code decoding (LDPC)
- outer code decoding (BCH).

7.4.1 Supported MODCODs

The LDPC decoder supports MODCOD 4 to MODCOD 17 in normal FEC frame (64800 bits).

Table 10. MODCOD encoding

Mode	MOD COD	Mode	MOD COD	Mode	MOD COD	Mode	MOD COD
QPSK 1/4	1_D	QPSK 5/6	9_D	8PSK 9/10	17_D	32APSK 4/5	25_D
QPSK 1/3	2_D	QPSK 8/9	10_D	16APSK 2/3	18_D	32APSK 5/6	26_D
QPSK 2/5	3_D	QPSK 9/10	11_D	16APSK 3/4	19_D	32APSK 8/9	27_D
QPSK 1/2	4_D	8PSK 3/5	12_D	16APSK 4/5	20_D	32APSK 9/10	28_D
QPSK 3/5	5_D	8PSK 2/3	13_D	16APSK 5/6	21_D		
QPSK 2/3	6_D	8PSK ¾	14_D	16APSK 8/9	22_D		
QPSK 3/4	7_D	8PSK 5/6	15_D	16APSK 9/10	23_D		
QPSK 4/5	8_D	8PSK 8/9	16_D	32APSK 3/4	24_D		

7.4.2 Iteration control

The number of iterations carried out by the LDPC can be scaled up or down to optimize throughput, decoder performance, and power dissipation for a given application, depending on the operating frequency.

The number of iterations are programmed by the registers *NBITER_NFx*. The trailing number of the register name is the MODCOD number (see *Table 10*).

7.4.3 Input gain

For each modulation (QPSK, 8PSK) and each code rate (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10), it is possible to change the input gain applied on the input software decision values of the LDPC. This is programmable by the registers *GAINLLR_NFx* and. Reset values correspond to a gain equal to 1. The 7-bit register value allows a gain between 0 and 4 (that is, from 0 to 127 / 32).

7.5 Packet delineator

This block manages the interface between the DVBS2 channel and the transport stream output.

The control and monitoring registers of this block are in the address range 0xF550-0xF56F. The control registers are *PDELCTRL1*-2 and the block status can be monitored with registers *PDELSTATUS1*-2.

The main functions are:

- Descrambling: recovery of BBFRAME.
- Base band frame header (BBH) integrity checking: cyclic redundancy checksum (CRC 8 bits) validation.
- Lock monitoring: consecutive valid blocks are detected and compared with threshold registers with lock hysteresis.
- Header processing and transport stream filtering: BBH fields are stored and communicated to the transport stream block.
- Data field processing: this process extracts and generates standard user packets. Payload CRC computation and sync byte insertion are made on the fly.
- SYNCD estimation: in the case of corrupted BBHEADER the SYNCD is calculated.

7.5.1 Descrambling

The complete DVBS2 BBFRAME received from the FEC decoder is de-scrambled. The descrambling sequence is synchronous with the BBFRAME, starting from the MSB and ending after Kbch bits.

The (de) scrambling sequence is generated by the feed-back shift register. The polynomial for the pseudorandom binary sequence (PRBS) generator is:

$$1 + X14 + X15$$

Loading of the sequence (100 1010 1000 0000) into the PRBS register, is initiated at the start of every BBFRAME.

7.5.2 Baseband frames header (BBH) integrity checking

The useful part of the incoming stream (excluding the sync byte) is processed by a systematic 8-bit CRC encoder. The generator polynomial is:

$$g(X)= (X5 + X4 + X3 + X2 + 1)(X2 + X + 1)(X + 1) = X8 + X7 + X6 + X4 + X2 + 1$$

The CRC encoder output is computed as: CRC = remainder [X8 u(X): g(X)] where u(X) is the input sequence (data, 8 bits) to be systematically encoded.

The number of erroneous frames is available in *BBFCRCKO1*-0.

7.5.3 Lock monitoring

This block uses the BBHEADER CRC check result to dive an up/down counter. The counter counts up whenever a CRC check is correct, and counts down if not correct. If this counter is above *HYSTTHRESH*.DELIN_LOCK_THRESHOLD, *PDELSTATUS1*.PKTDELIN_LOCK is set. If it goes below *HYSTTHRESH*.UNLOCK_THRESHOLD, it is reset.

The *PDELSTATUS1*.FIRST_LOCK register is simpler. Once its value has been reached it is set and indicates that the packet delineator has started to treat frames.

7.5.4 Header processing and transport stream filtering

A dedicated mechanism identifies the incoming streams based on the MATYPE information. A fixed length base-band header (BBHEADER) of 10 bytes is inserted in front of the data field, describing its format. The MATYPE can be found in the read-only register *MATSTR1*-0.

MATYPE (2 bytes) describes the input stream format, the type of mode adaptation and the transmission roll-off factor. All the stream information fields are stored in registers *MATSTR1*-0, *UPLSTR1*-0, *DFLSTR1*-0, *SYNCSTR* and *SYNCDSTR1*-0.

SIS/MIS (1 bit) describes whether there is a single input stream or multiple input streams. If SIS/MIS = multiple input stream, then the second byte is the input stream identifier (ISI), otherwise the second byte is reserved.

In the case of multiple input streams, ISI filtering can be activated. In this case only BBFRAMES with the correct ISI will be forwarded to the transport stream.

7.5.5 Data field processing

The packets are assembled into groups of the appropriate byte length (including sync bytes). For example, MPEG packets are assembled into groups of 188 bytes.

A CRC is computed for each packet which provides the ERROR signal on the transport stream output.

7.5.6 SYNCD estimator

In case of failure of BBHEADER CRC check it is assumed the BBHEADER is corrupted. This means the SYNCD value must be considered as potentially wrong. In this case SYNCD is estimated. The object being to ensure the integrity of the shared packet between the previous BBFRAME and current (corrupted) BBFRAME.

7.5.7 BCH check

A final frame verification, based on the BCH check result, has been implemented. If one single arror occurs anywhere in the frame the entire frame willbe rejected. This service was made available because occasionally errors may occur in the BB header that fool the relatively weak CRC check.

For BCH check on: PDELCTRL2[bit 0]=1, PDELCTRL3[bit 5]=1.

For BCH check off: PDELCTRL2[bit 0]=0, PDELCTRL3[bit 5]=0.

8 Transport stream interface

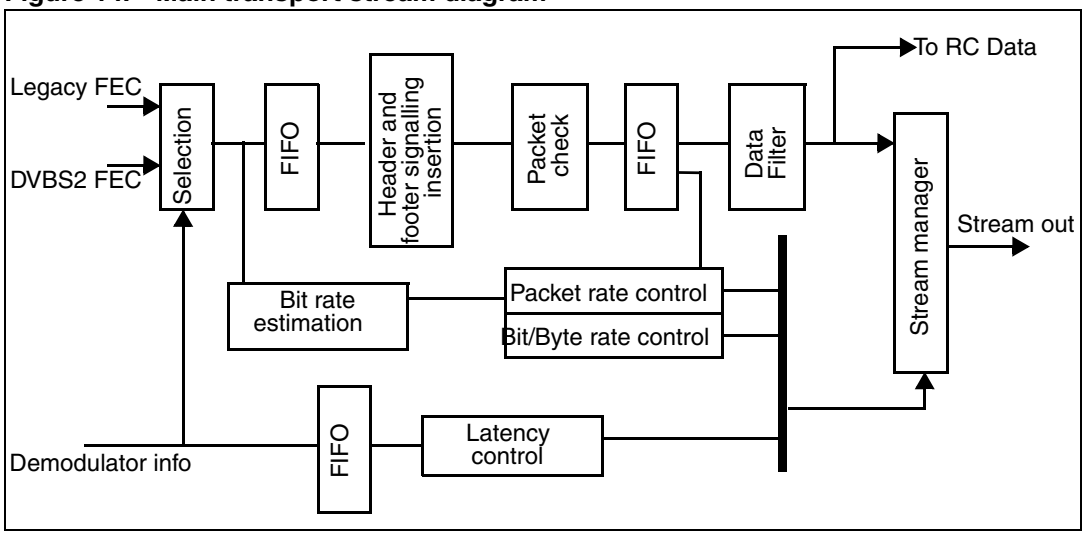
The transport stream (TS) interface takes data from the DVB-S2 or legacy reed-solomon forward error correctors and formats the data for transmission to the back-end decoder.

Only TS3 is supported. TS3 can be configured in serial or parallel mode.

8.1 Transport stream overview

The block diagram of the TS block is shown in *Figure 14* below.

Figure 14. Main transport stream diagram



8.2 Transport stream output processing

The stream may be formatted with or without sync bytes or header bytes and the output rate may be controlled manually or adjusted automatically.

Register *TSINSDELH* allows the sync and header bytes in an MPEG packet to be removed. This is useful when using external bit error rate test equipment.

The TS line is configured by *TSCFGH*/M/L registers.

The TS interface is DVB-CI compliant but also supports some extended behavior.

8.2.1 General

The transport bus is made of the following pins: CLKOUT, STROUT, DPN, ERROR and D7 to D0 in parallel mode or only D7 in serial mode.

After a hardware reset, the transport bus is set to high impedance (disabled) and must be configured to low impedance (enabled) by programming register *OUTCFG*. TS3 can be serial or parallel. For TS3, there are two control bits to configure the pins; one for the serial part (control signals + data 7) and one for the data bits 6:0.

The transport stream is activated when one of the FEC decoders outputs valid data. The transport stream remains active until lock loss is detected.

The DPN (data valid / parity negated) pin is high when payload data is being output from the FEC. The DPN signal is low when redundant data is present (redundant data can be the parity data or rate regulation stuffing bits).

Data is regulated by both CLKOUT and DPN. There are two regulation modes known as ‘data valid’ and ‘envelope’. The data valid mode uses a continuous clock and selects valid data on DPN. The envelope mode indicates the periods of valid data on DPN and then uses a punctured clock for rate regulation. The regulation mode is selected by register bit *TSCFGH*. TSFIFO_DVBCI (1 for a data valid mode, 0 for the envelope mode)

The polarity of the TS signal is selected with bit XOR of corresponding IO configuration register. It makes sense to invert the polarity only for the CLKOUT signals, so the change can be done with bit CLKOUT3_XOR of the register *CLKOUT27CFG*. CLKOUT_XOR = 0 the output signals are valid on the rising edge of the CLKOUT signal (on the falling edge if CLKOUT_XOR = 1).

8.2.2 Data rate control

The TS interface controls the output data rate. Padding bits are generated automatically according to the instantaneous bit rate and actual output data rate. The configuration is set in field TSFIFO_MANSPEED. Four modes are provided, three of them are fully automatic and the fourth allows manual control of the regulation. The fully automatic mode is recommended, see *Table 11*.

Table 11. TSFIFO_MANSPEED configuration

TS Rate Control Mode	TSFIFO_MANSPEED
Manual	11
Fully automatic	00
Conservative automatic	01
Dynamic automatic	10

For all configurations, the output data rate is:

- serial interface, data rate = bit rate = Mclk * 32 / TSFIFO_OUTSPEED
- parallel interface, data rate = byte rate = Mclk * 4 / TSFIFO_OUTSPEED

where Mclk = 135 MHz, and TSFIFO_OUTSPEED is the field of the register *TSSPEED*. The speeds allowed are summarized in *Table 14*. If the value of TSFIFO_OUTSPEED is less than allowed, it will be clipped to the minimum allowed value.

Table 12. TS allowed speeds

TS mode	Min rate	Max rate
Serial	17 MHz TSFIFO_OUTSPEED = 0xFF	135 MHz TSFIFO_OUTSPEED = 0x20
Parallel	4.25 MHz TSFIFO_OUTSPEED = 0xFF	67.5 MHz TSFIFO_OUTSPEED = 0x08

Some TSFIFO_OUTSPEED values can create a clock with a duty cycle not equal to 50%. To ensure a clock duty cycle of 50%, the bit TSFIFO_DUTY50 of the register *TSCFGH* can be set. It will constrain TSFIFO_OUTSPEED to be:

- a multiple of 32 in serial mode
- a multiple of 4 in parallel mode.

Automatic mode (recommended)

In this case, the chip computes TSFIFO_OUTSPEED from these data:

- packet rate
- header and footer (if any) signalling rate
- reed-solomon parity (if any) rate.

The packet rate equations are

DVBS1, packet rate = SR * mapping * PR / UPL

DVBS2, packet rate = SR * DFL * (NPDav + 1) / (PLFL * UPL)

where:

SR = symbol rate

Mapping = 2 for QPSK, 3 for 8PSK, etc.

PR = puncture rate

UPL = packet length in bit (for example, 204x8 in DVBS1)

DFL = datafield length

PLFL = PLFrame length

NPDav = mean value of NPD byte if MATYPE/NPD = 1 or 0 if MATYPE/NPD = 0.

In automatic mode the chip recomputes TSFIFO_OUTSPEED after any change in one parameter involved in the equations.

Other automatic modes

- Not recommended.

Manual mode

In manual mode, the user sets the desired speed with by programming the TSFIFO_OUTSPEED register. Should the required data rate exceed the capacity, the start of the next packet will overwrite the end of the current packet.

8.2.3 Latency Control

In the STV0903 the total latency from the signal entering the pins IQ to the output on one of the transport stream bus is controlled, fixed and known, see *Table 13*.

Table 13. Chip total latency

Mode	Total latency(1)
Legacy DVBS1/DTV	26675 symbols
DVBS2	73332 symbols

1. these values might change slightly.

8.3 Serial output modes

In serial mode the data is output MSB first. The serial mode supports both rate regulation modes in the following way.

- Serial output mode with pin DPN used as data valid signal for discriminating between wanted data and "*don't care*" bits, *Figure 16* and *Figure 18*.

  In this mode, the CLKOUT clock signal is continuous. The desired rate is obtained by skipping the unwanted data using the DPN signal. The 'holes' in DPN signal are automatically inserted with regards to both the actual data payload rate (including the parity bits when present) and the CLKOUT frequency.

- Serial output mode uses the DPN signal as an envelope for the valid data section of the transport stream; the CLKOUT signal is then interrupted ('punctured' in order to skip the unwanted data *Figure 17* and *Figure 19*.

  In this mode, the DPN data valid signal is used as an envelop to the useful data, excluding the parity bits. The CLKOUT signal is used to reach the actual payload rate: holes are automatically inserted in the regular periodic clock signal to adjust the mean frequency to the desired payload rate.

The STROUT pin is high during the first bit of the packet payload.

The rate compensation mode (TSCFGH:TSFIFO_DVBCI bit) is set as in *Table 14*

Table 14. Rate compensation mode settings

	Serial1 mode = data valid	Serial2 mode = envelope
TSFIFO_DVBCI	1	0

Figure 15. Serial output interface (CLKOUT_XOR = 1), data valid

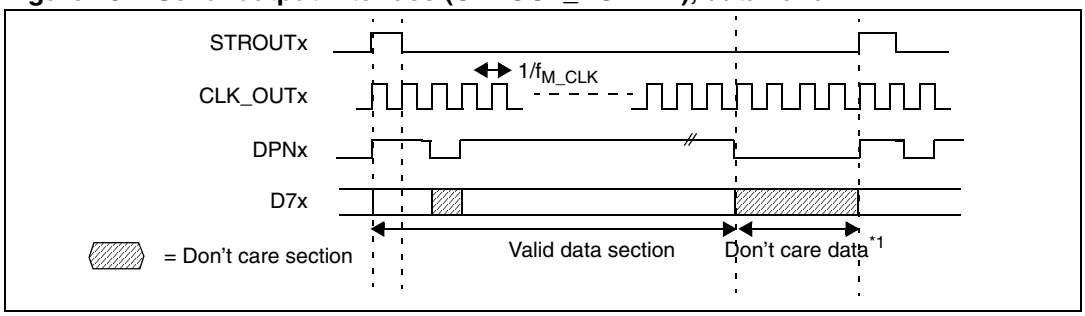


Figure 16. Serial mode options in valid data section (CLKOUT_XOR = 0), data valid

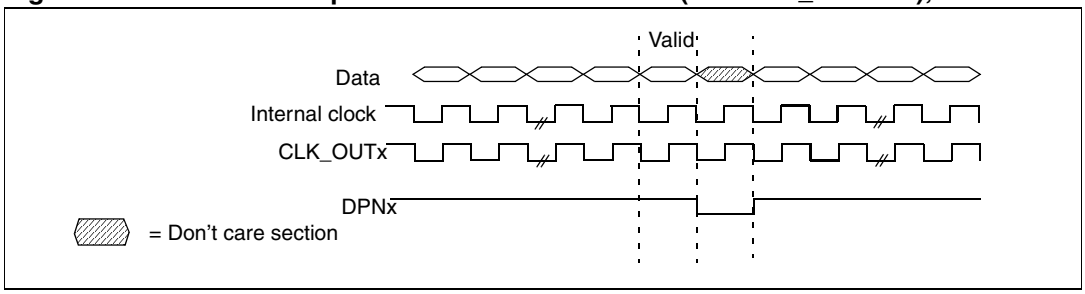


Figure 17. Serial output interface (CLKOUT_XOR = 1), envelope

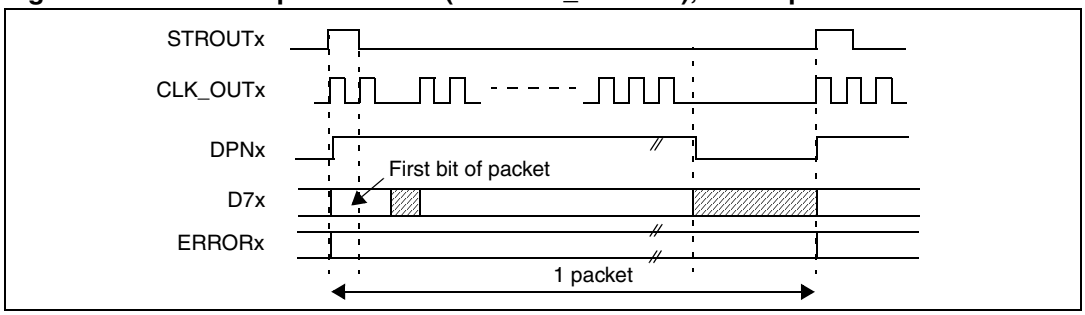
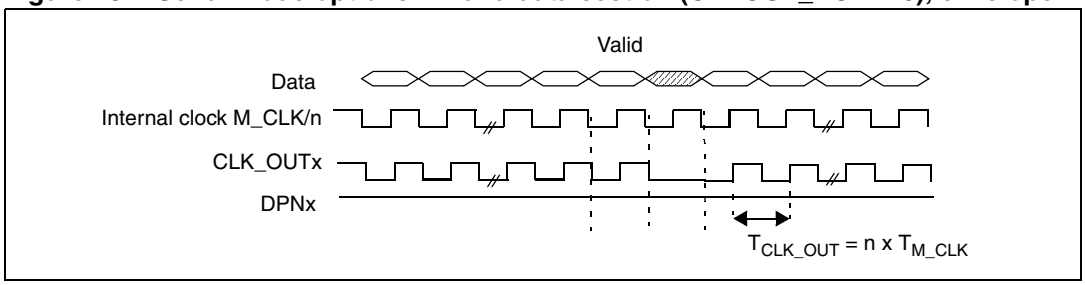


Figure 18. Serial mode options in valid data section (CLKOUT_XOR = 0), envelope



8.4 Parallel output modes

The STV0903 features two different parallel output modes.

- ST back-end (recommended mode). CLKOUT is held high or low (depending on register bit *TSCFGH*.TSFIFO_DVBCI) for unknown data sections, see *Figure 19 on page 49* and *Figure 21 on page 50*.
- DVB-CI. Where DPN is held high or low (depending on register bit *CLKOUT27CFG*.CLKOUT_XOR) for unknown data sections, see *Figure 20 on page 50* and *Figure 22 on page 50*.

In both parallel output modes, the STROUT pin is high during the first byte of the packet.

The rate compensation mode (*TSCFGH*.TSFIFO_DVBCI bit) is set as in *Table 15*.

Table 15. Rate compensation mode settings

	DVB-CI	ST Back-end
TSFIFO_DVBCI	1	0

Figure 19. ST back-end output interface (CLKOUT_XOR = 0)

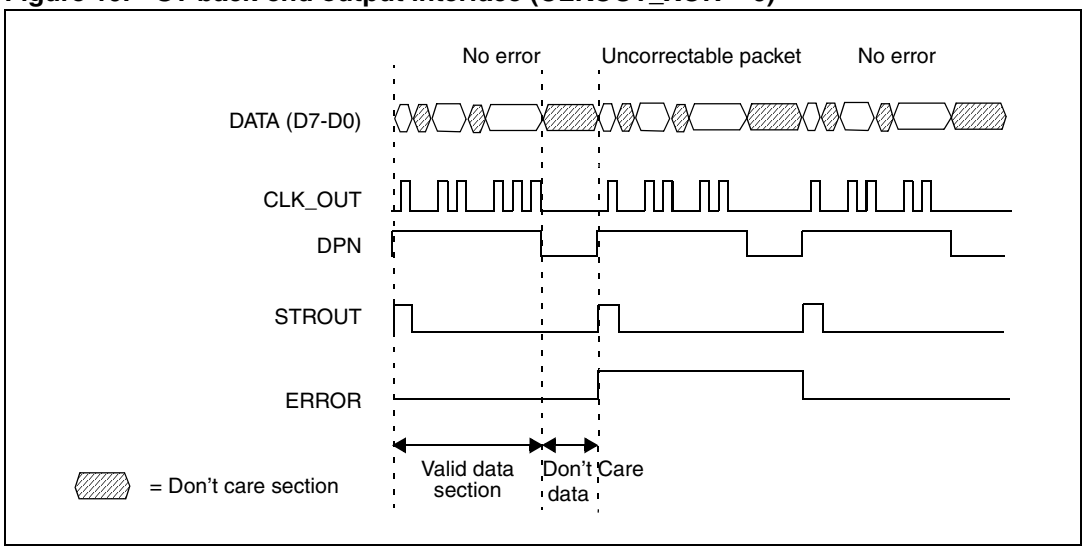


Figure 20. DVB-CI output interface (CLKOUT_XOR = 0)

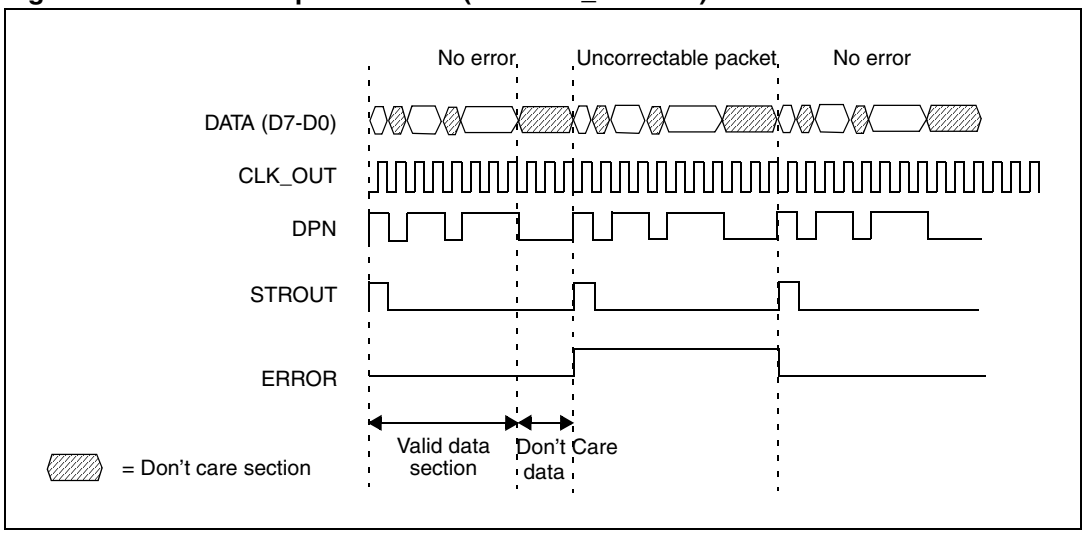


Figure 21. ST back-end in valid data section (CLKOUT_XOR = 0 example)

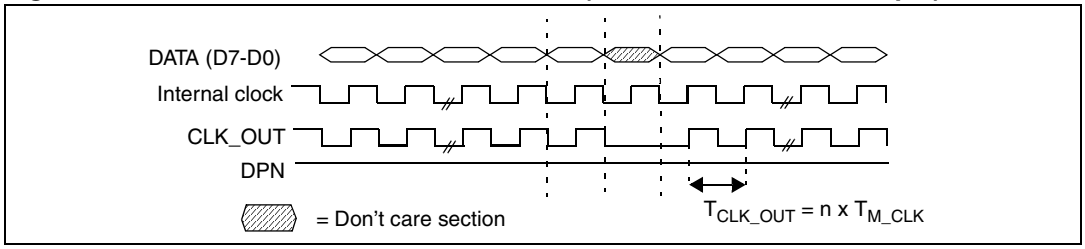
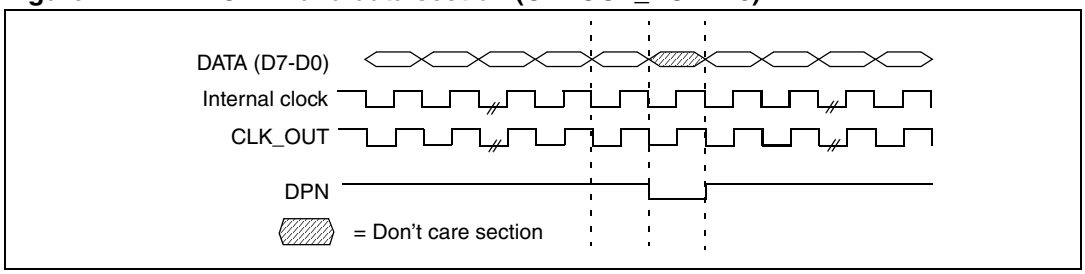


Figure 22. DVB-CI in valid data section (CLKOUT_XOR = 0)



9 DiSEqC 2.x interface

9.1 Introduction

The STV0903 integrates one DiSEqC 2.x interface to communicate to an LNB.

9.2 Transmit DiSEqC interface

The transmit DiSEqC interface simplifies the real-time dialog between the microprocessor and the LNB. Using the I^2C bus, the microprocessor fills an 8-byte FIFO (register *DISTXDATA*), and then transmits the data by modulating the DiSEqC transmit clock. The transmit clock frequency is set via register *F22TX*.

Three status signals are available on the I^2C bus (register *DISTXSTATUS*):

- TX_IDLE (transmitter is waiting)
- TXFIFO_BYTES (remaining bytes in FIFO)
- FIFOFULL - FIFO full.

9.2.1 Typical byte transfer loop

1. DIS_PRECHARGE is set to 1 (register *DISTXCTL*) to put the transmitter in a wait state.
2. One to eight bytes can be transferred by writing to the FIFO.
3. DIS_PRECHARGE is set to 0 and the transmitter begins sending data.
4. To transfer more than eight bytes, the FIFO must not be full: FIFOFULL = 0. Use the equation
   (8 - TXFIFO_BYTES) to calculate the number of bytes that can be stored.

Note: 1 Before starting, the FIFO is empty (TX_IDLE = 1, TXFIFO_BYTES = 0, FIFOFULL = 0) and is in an idle state.

2 If DIS_PRECHARGE is set to 0, transfer begins as soon as a byte is written to the FIFO. TX_IDLE = 0 during the transmission.

3 After the last transmitted byte, the interface returns to an idle state (TX_IDLE = 1.)

9.2.2 Transmit format

There are two modes for DiSeqC output; modulated and envelope. The mode is selectable from register bit *DISTXCTL*.DISTX_MODE. In the modulated mode the output is a gated 22 kHz square wave signal. In the envelope mode the tone is replaced by a logic high, A logic low replaces ‘no tone’.

When the modulation is active, the DiSEqC output is forced alternatively to V_{DD} and V_{SS} levels.

Byte format

- Idle state: no modulation is present at the output.
- Byte transmission: the byte is sent (MSB first) and is followed by an odd parity bit.
  A byte transmission is therefore a 9-bit serial transmission with an odd number of ones.

Each bit lasts 33 periods of F22 and the transmission is PWM-modulated.

Transmission of ones

During the transmission of ones, modulation is active for 11 pulses, then inactive for 22 pulses (1/3 PWM).

Transmission of zeros

There are two sub modes controlled by register bit *DISTXCTL*.DISTX_MODE:

- DISTX_MODE =010: modulation is active for 22 pulses, then inactive for 11 pulses (2/3 PWM)
- DISTX_MODE =011: modulation is active for 33 pulses (3/3 PWM)
- DISTX_MODE =100: modulation is active for 22 pulses, then inactive for 11 pulses (2/3 PWM) in envelop mode
- DISTX_MODE =101: modulation is active for 33 pulses (3/3 PWM) in envelop mode.

Figure 23. Schematic showing bit transmission (modulated mode)

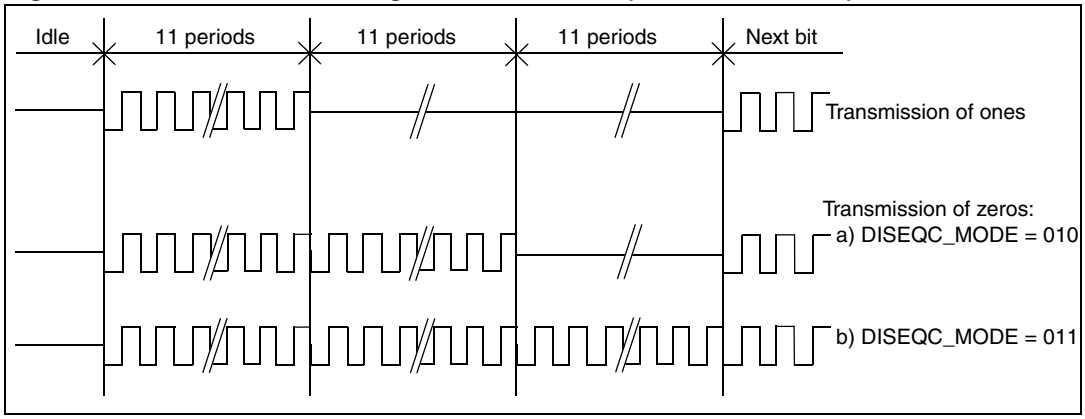
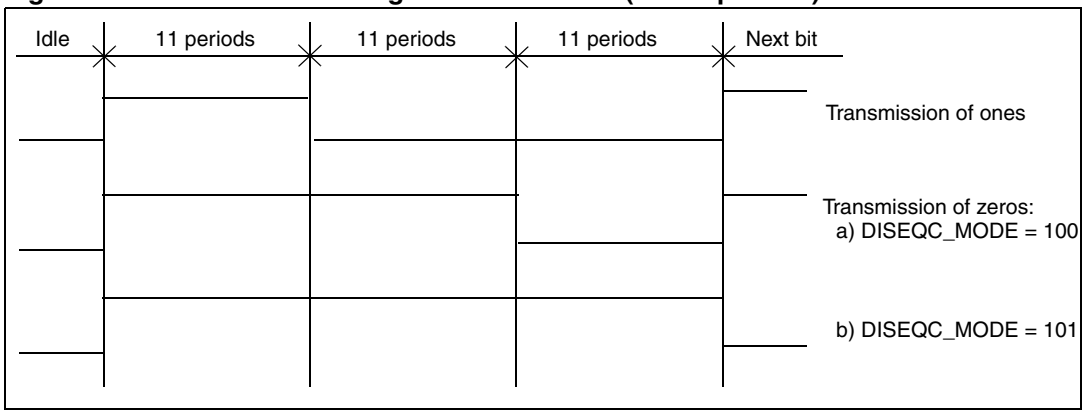


Figure 24. Schematic showing bit transmission (envelop mode)



9.2.3 DiSEqC modes SA, SB and continuous

- Mode SA: unmodulated tone burst. Set DISTX_MODE = 011 and write one byte of value 0x00 to the Tx FIFO. The parity bit is automatically set to 1. As a result, the output signal is a continuous tone of 12.5 ms.
- Mode SB: modulated tone burst. Set DISTX_MODE = 010 and write one byte of value 0xFF to the Tx FIFO. The parity bit is automatically set to 1. As a result, the output signal is nine 0.5 ms bursts, separated by eight 1 ms intervals.
- Continuous mode**:** continuous tone burst. Set DISTX_MODE to 000.

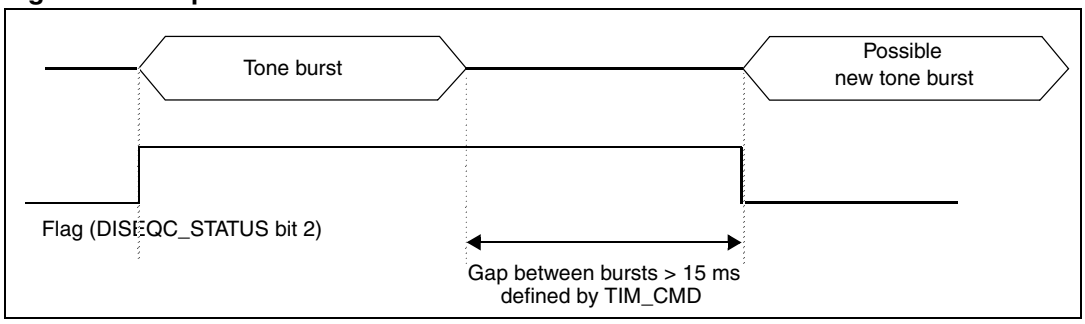
9.2.4 Transmit burst gap control

The backward compatibility of DiSEqC requires a 15 ms gap after a tone burst sequence. To meet this a programmable gap between busts is implemented.

To enable the gap timer set *DISTXCTL*.TIM_OFF (timing offset) to 1.

Gap between bursts

Figure 25. Gap between bursts



Register *DISTXSTATUS*.GAP_BURST flag is set at the beginning of the transmission and remains high until the gap timer has expired.

The length of the gap between busts is defined by *DISTXCTL*.TIM_CMD:

TIM_CMD (DISEQC[5:4]): 00: number of 22 kHz periods = 330 = 15 ms
01: number of 22 kHz periods = 440 = 20 ms
10: number of 22 kHz periods = 550 = 25 ms
11: number of 22 kHz periods = 660 = 30 ms

9.3 Receive DiSEqC interface

The DiSEqC receive interface is composed of:

- an analog input with bypassable 1-bit analog-to-digital conversion
- digital filtering for envelope detection
- digital processing providing received byte extraction and stacking in FIFO, status management.

Figure 26. DiSEqC Rx analog part, running mode

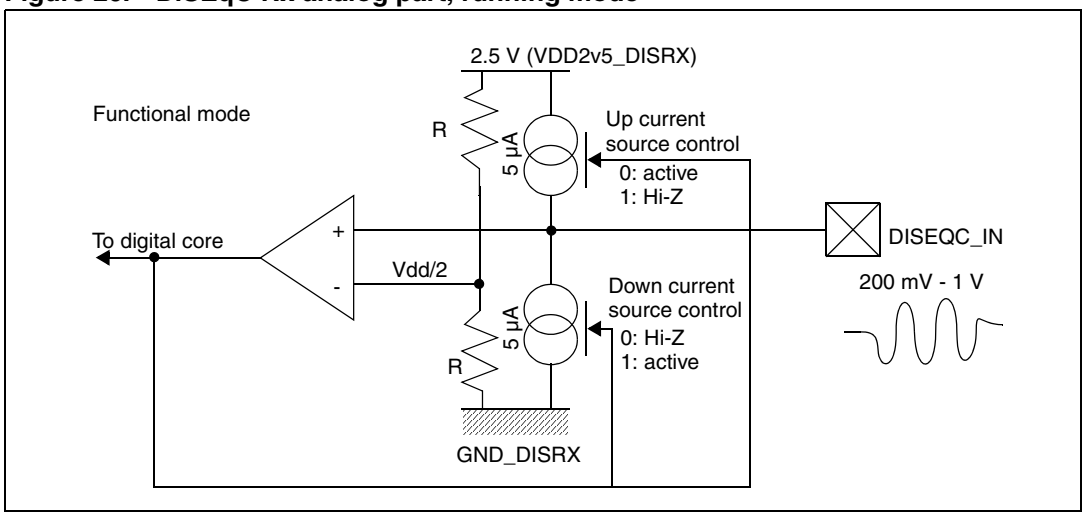
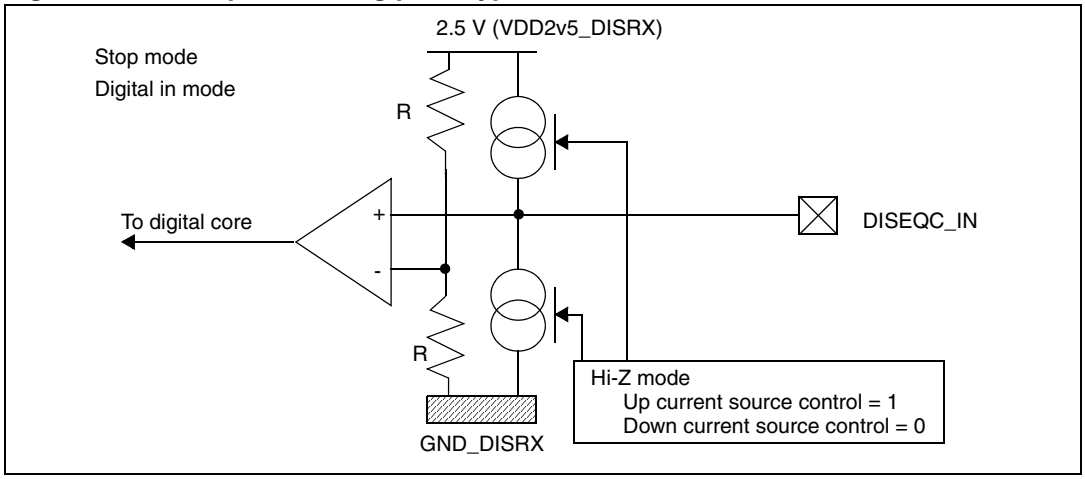


Figure 27. DiSEqC Rx analog part, bypassed mode



The DiSEqC receiver is switched on by setting bit *DISRXCTL*.RECEIVER_ON to 1.

An external filter conditions the analogue input signal which is sampled via a 1 bit DAC. The signal is then filtered digitally. The digital filter frequency is set in register *F22RX*.

Register bit *DISRXCTL*.EXT_ENVELOP enables the analog bypass (invoking the envelope mode) depicted in *Figure 27* otherwise the configuration of *Figure 26* is used (default).

The digitized bits are then assembled into bytes, checked for parity and stacked in the FIFO. The FIFO is eight bytes deep.

The DiSEqC input may be selected via the PIN_SELECT bits to be the DISEQCIN1-2 pins (default) or the GPIO1-4 pins. The input may be inverted (should the envelope mode require it).

A test mode allows the DiSEqC Tx to be looped back into the Rx (accessible though bit *DISRXCTL*.ONECHIP_TRX).

The received bytes are stacked in the receiver FIFO (register *DISRXDATA*). The status registers (*DISRX_ST0*, *DISRX_ST1*) provide information concerning the state of the receiver:

- reception ended
- receiver active
- continuous tone detected
- 4 bytes ready for reading
- FIFO empty
- reception failed
- parity error detected
- wrong number of bits to make a byte detected
- FIFO overflow
- number of bytes in FIFO.

In addition to the above status registers there are interrupt flags (in register *DISRXDATA*):

- To generate an interrupt at the end of a receive block.
- To generate an interrupt if there are 4 or more bytes in the FIFO ready for reading.

10 FSK interface

10.1 Introduction

The STV0903BAC integrates a flexible FSK modem for on-cable communication. A wide range of carrier, deviation and modulation frequencies are supported.

The design has been optimized with respect to the bill of materials to allow an economical implementation of the FSK function.

The transmitter consists of a digital oscillator which is modulated by a digitally generated deviation frequency. The output is then shaped by a single-bit sigma-delta DAC. The system has been designed to meet spectral suppression requirements in conjunction with a simple external filter.

The receiver is also implemented using a sigma-delta converter, allowing efficient linear filtering whilst minimizing the external bill of materials. Thus, the IC can support relatively high adjacent channel impairments.

The associated registers are detailed in *Section 17.3: FSK register descriptions on page 103*.

10.2 FSK activation

The FSK function is shared with the second DiSEqC. So, some work must be done to enable the FSK function in the STV0903BAC. Firstly, a 1 must be written in register bit *TSTTNR0*.SEL_FSK. Secondly, some GPIOs must be reprogrammed to output the FSK control signals:

- FSKTX_OUT, FSK transmitter output
- FSKTX_IN, FSK transmitter in
- FSKTX_EN, FSK transmitter enable
- FSKRX_DETECT, FSK receiver detect flag
- FSKRX_OUT, FSK receiver out.

See *Chapter 11: General purpose I/O (GPIO) on page 60* on how to configure the GPIOs.

10.3 FSK transmitter

The transmitter (modulator) outputs an instantaneous frequency depending on the digital value (one or zero) on pin FSKTX_IN. The modulator output is on pin FSKTX_OUT and has three states:

- off: high impedance, one or zero
- low frequency: the carrier frequency (fc) minus the deviation frequency (Δf)
- high frequency: the carrier frequency (fc) plus the deviation frequency (Δf).

The transmitter may be activated by a hardware pin (FSKTX_EN) or by register control in register bit *FSKTCTRL*.FSKT_MOD_EN.

Both transmitter control pins (FSKTX_EN and FSKTX_IN) may have their sense inverted through the appropriate bits in register *FSKTCTRL*.

The input bit rate (the rate at which pin FSKTX_IN is toggled) is unknown to the modulator and is not limited.

All frequency values are derived from the master clock f_{MCLK}. The carrier frequency is programmable from 0 to f_{MCLK} / 4 in steps of f_{MCLK} / 2^{20}.

The RF output is implemented using a standard digital pin with three possible signal conversion schemes.

- 1-bit sigma-delta converter with second order loop: this gives the best signal to noise ratio around the carrier frequency. It needs an external low pass filter to remove high frequency components.
- 1-bit sigma-delta converter with first order loop: the signal to noise ratio is worse but the amplitude of the wanted signal may be higher.
- 1-bit converter: the output is the modulated carrier quantized in two frequencies, fc+Δf and fc-Δf. The amplitude is at its maximum, but the signal spectrum contains lots of spurious frequencies. This scheme may be used for low carrier frequencies (below 1 MHz).

When using the delta-sigma schemes, the amplitude may be controlled by register bitfield *FSKTCTRL*.FSKT_KMOD according to the *Table 16* below.

Table 16. Modulator gain values

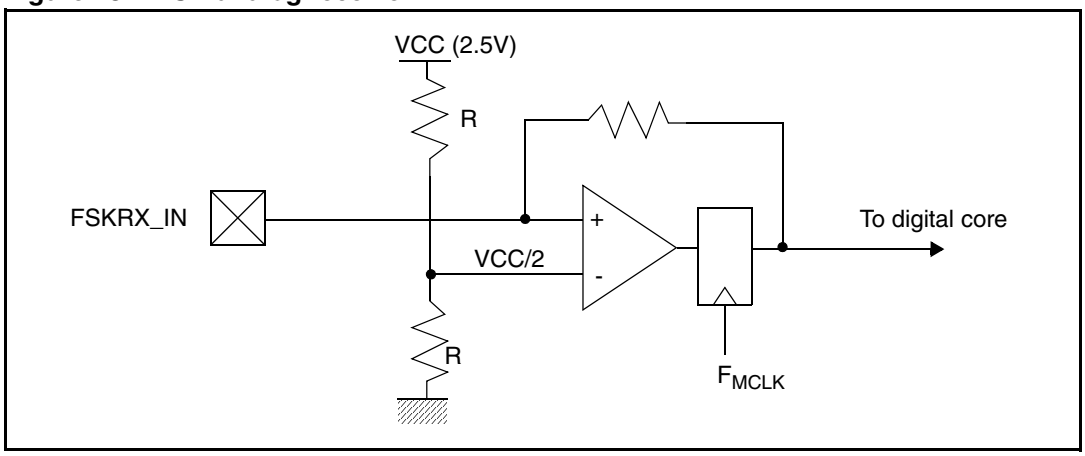
	Max gain value FSKT_KMOD	Max pk to pk level (after LPF)	Typical CNR at 0.04 * f_{MCLK}
Delta-sigma 2nd order	32 (TBC)	0.22 VCC (TBC)	35 dB (TBC)
Delta-sigma 1st order	63 (TBC)	0.44 VCC (TBC)	30 dB (TBC)
1-bit DAC	NA	1.4 VCC (TBC)	14 dB (TBC)

10.4 FSK receiver

The input RF input is applied to the input pin FSKRX_IN via an external RC integrator. The average input voltage (on pin FSKRX_IN) is maintained constant by internal feedback (a resistor switched to ground or VCC). This RC configuration with feedback implements a 1^{st}-order sigma-delta converter.

As per the transmitter, the receiver (demodulator) centre frequency is programmable from 0 to f_{MCLK} / 4 in steps of f_{MCLK} / 2^{20}.

Figure 28. FSK analog receiver



The input RF signal range is from 2 mV to VCC.

After conversion, the signal is filtered by a 2^{nd}-order filter centered on the carrier with programmable bandwidth defined by k1 and k2:

$k1 = 2^{20} * 8 * \pi * BW / f_{MCLK}$

$k2 = 2^{20} * (8 * \pi * BW / f_{MCLK})^2$

Where BW is the single sided bandwidth of the external filter, typically equal to the expected frequency deviation plus half the baud rate, and k1 and k2 are defined by pseudo floating point values in registers FSKRK1 and FSKRK2:

$k1 = fskr\_k1\_mant * 2^{8+fskr\_k1\_exp}$

where fskr_k1_mant = 1 to 31 and fskr_k1_exp = 0 to 5

$k2 = fskr\_k2\_mant * 2^{fskr\_k2\_exp}$

where fskr_k2_mant = 1 to 31, fskr_k2_exp = 0 to 7.

A signal AGC maintains the output level to the programmed reference level in register bit *FSKRAGC*.FSKR_AGC_REF with six possible time constants in powers of 2. Value 0 corresponds to the longest time constant. The AGC accumulator may be read in register *FSKRAGC*, its content is an image of the in-band signal amplitude, this may serve as an FSK received strength indicator.

The instantaneous frequency deviation is then extracted by a PLL, compared with a threshold and the result made available on the output pin FSKRX_OUT. The output only changes if the absolute value of the deviation is above a programmable threshold FSKR_PLL_THRESH, thus providing some protection against noise. The unit of the threshold is f_{MCLK} / 2^{20}.

The PLL is a second order loop, with damping factor (ξ) and natural frequency (*fnat*) depending on parameters α and β:

$$fnat = 7\times10^{-6} \cdot fo \cdot \sqrt{\beta \cdot FSKR\_AGC\_REF}$$

$$\xi = 88\times10^{-6} \cdot \alpha \cdot \sqrt{\frac{FSKR\_AGC\_REF}{\beta}}$$

where:

$\alpha = 256 * (4 + fskr\_alpha\_m) * 2^{fskr\_alpha\_exp}$

$\beta = 2^{fskr\_beta}$

The recommended settings correspond to a damping factor close to 0.8 to 1 and a natural frequency up to 100% above the baud rate.

The presence of an FSK signal is detected by register bitfield FSKR_CARDET_ACCU (made up of two registers *FSKRDETx*). This indicates a value representative of the average absolute value of the frequency deviation. It is compared to two thresholds to declare the lock state or the lost state of the PLL (FSKR_CARDET_THRESH, FSKR_CARLOSS_THRESH). The unit is $f_{MCLK} / 2^{20}$.

The recommended values (TBC) are:

fskr_cardet_thresh = 3/4 Δf

fskr_carloss_thresh = 1/4 Δf

where Δf is the frequency deviation.

The carrier detection depends on a statistical analysis controlled by FSKR_STEP_PLUS and FSKR_STEP_MINUS.

The parameters step_plus and step_minus defined in pseudo floating point by:

$step\_plus = fskr\_step\_plus[4:0] * 2^{fskr\_step\_plus[7:5]}$

$step\_minus = fskr\_step\_minus[4:0] * 2^{fskr\_step\_minus[7:5]}$

As a first approximation it is recommended to set these values to:

$step\_plus = 80000 * \Delta f / f_{MCLK}$

step_minus = 4 * step_plus

The result of the carrier detection can be routed on any GPIO pin configured as FSKRX_DETECT (see *Chapter 11: General purpose I/O (GPIO) on page 60*). The sign of this output is also programmable in register *FSKTCTRL*, bit FSKT_EN_SGN.

11 General purpose I/O (GPIO)

11.1 Overview

The flexible GPIO implementation allows simple, in-depth debug and allows digital signals to be routed to the most convenient pin (facilitating board layout and test).

All digital pins pass via the GPIO bus and may be configured via the GPIO registers. 27 GPIO pins are defined at reset to the functions given below in *Section 11.2*. Other GPIO pins (GPIO01 to GPIO13) are unallocated and may be programmed at will. *Section 11.3* shows the possible functions which can be allocated to these 13 GPIOs using registers GPIO01CFG to GPIO13CFG. Since the behavior of these registers is identical they are described under the single register name *GPIOxCFG on page 96*, where n is the GPIO number (GPIOn).

The syntax for programming all the GPIO registers is shown in the bitfield below.

7	6	5	4	3	2	1	0
Open drain	Configuration value						XOR

Bit 7 is for open drain. When high it configures the pin in open-drain (current sink, high impedance or input); when low it configures the pin as a classical push-pull (output).

Bits [6:1] configure the value. See *Table 18 on page 61*.

Bit 0 selects XOR to invert the signal selected (by applying an XOR operation with the value of bit 7).

The 13 GPIO pins are configured by default to 0x82 which implies they are set to open drain, logic 1 (that is, high impedance).

Refer to the *GPIOxCFG* registers to configure these pins for application-specific requirements.

11.2 Pre-programmed GPIOs

The pins in *Table 17* are pre-assigned GPIOs but can be reconfigured by accessing the corresponding configuration registers.

Table 17. Pre-defined GPIOs

Pin name	Configuration register
SDAT1	SDAT1CFG
SCLT1	SCLT1CFG
AGCRF1	AGCRF1CFG
CKOUT27	CKOUT27CFG
DISEQCOUT1	DISEQCO1CFG
ERROR	ERRORCFG
DPN	DPNCFG
STROUT	STROUTCFG
CLKOUT	CLKOUTCFG
DATA7	DATA7CFG
CLKI2	CLKI2CFG
DIRCLK	DIRCLKCFG(1)
STDBY	STDBYCFG(1)
CS0	CS0CFG(1)
CS1	CS1CFG(1)

1. It is not recommended to reprogram these pins as they are tested on power-up and recovery from reset and configure the state of the IC.

11.3 Unallocated GPIO functions

Use registers GPIOnnCFG to program the desired function to GPIOnn (nn = 01 to 13).

Table 18. GPIO configuration

Config value	Definition	Description
0	0	Forces output to logical 0
1	1	Forces output to logical 1
2	STREAM_STATUS1	Stream Status 1
3	STREAM_STATUS2	Stream Status 2
4	STREAM_STATUS3	Stream Status 3
5	STREAM_STATUS4	Stream Status 4
6	STREAM_STATUS5	Stream Status 5
7	STREAM_STATUS6	Stream Status 6
8	DEMOD_AGCIQ_OUT1	Demodulator 1 I or IQ control output of AGC

Table 18. GPIO configuration (continued)

Config value	Definition	Description
10	DISEQCOUT1	DiSEqC1 2.0 output
12	FSKTX_OUT	FSK transmitter output
13	FSKRX_DETECT	FSK receiver detect flag
14	FSKTX_IN	FSK transmitter input
15	FSKTX_EN	FSK transmitter enable
16	FSKRX_OUT	FSK receiver output
17	OUT_BIT1	Output test out bit 1
18	OUT_BIT2	Output test out bit 2
19	DAC_OUT	DAC is output
20	IRQ	Interrupt request flag
23	VALID_SIM3	FEC spy 3 valid simulation flag
24	SDAT1	Tuner 1 dedicated SDA signal
25	SCLT1	Tuner 1 dedicated SCL signal
28	I2C_MAP0	Out register bit 1
29	I2C_MAP1	Out register bit 2
30	SDA2_OUT	SDA auxiliary output
31	SCL2_OUT	SCL auxiliary output
42	DPN	Transport stream dp/n
43	STROUT	Transport stream strout
44	ERROR	Transport stream error
45	CLKOUT	Transport stream clockout
46	D7	Transport stream serial data
47	SDD1_SOF	Stream 1 serial data description start of frame
48	SDD1_ENA	Stream 1 serial data description clock enable
49	SDD1_DATA	Stream 1 serial data description data
59	AUX_CLK1	Auxiliary clock 1
60	AUX_CLK2	Auxiliary clock 2
61	CLK270	Clock 270 MHz
62	CLK135	Clock 135 MHz
63	XTAL_IN	Clock crystal

The Stream Status signals can be configured by the 3 registers STRSTATUS1..3 and be configured to route these signals to a GPIO.

Table 19. STREAM_STATUS1..6 configuration

Config value	Definition	Description
0	DEMOD_SYMIQ1	Demodulator 1 detected an IQ symmetry
1	DEMOD_LOCKED1	Demodulator 1 locked flag
2	DEMOD_FAIL1	Demodulator 1 failed flag
3	PKTDEL_LOCKED1	Packet Delineator 1 locked flag
4	PKTDEL_ERROR1	Packet Delineator 1 error flag
5	VITERBI_PRF1	DVBS1 Viterbi 1 puncture rate found flag
12	STREAM_LOCKED1	Stream 1 (return channel) locked flag (up to transport)

12 Interrupt request (IRQ)

12.1 Overview

Interrupts can be generated by the STV0903.

The interrupt lines can be routed on a GPIO pin by using the GPIO configuration registers (see *Chapter 11: General purpose I/O (GPIO) on page 60*).

Each IRQ source can be masked via one of the registers *IRQMASKx on page 91* and the status on the source of the IRQ can be read on the corresponding register *IRQSTATUSx on page 89*.

12.2 IRQ configuration

Table 20. List of IRQs

IRQ name	IRQ #	Description
DiSEqC1 TX RE	0	Transmission IRQ rising edge: one of fifo-full, ...
DiSEqC1 RX RE	1	Reception IRQ rising edge
BCH block incorrectable IRQ	4	The BCH decoder detected an unreliable BCH block.
DEMOD1 IRQ RE	5	Rising edge of demod IRQ. A Status is available to indicate what is the interrupt source
DEMOD1 LOCKED RE	6	Rising edge of demod locked
DEMOD1 LOCKED FE	7	Falling edge of demod locked
EXT PIN 1 RE	11	Rising edge on external input port
EXT PIN 1 FE	12	Falling edge on external input port
EXT PIN 2 RE	13	Rising edge on external input port
EXT PIN 2 FE	14	Falling edge on external input port
PKTDEL1 LOCK RE	15	Rising edge on packet delineator lock
PKTDEL1 LOCK FE	16	Falling edge on packet delineator lock
PKTDEL1 ERROR RE	17	Rising edge on packet delineator error
FECSPY1 ENDSIM	21	FECSPY end of simulation rising edge
VITERBI 1 PRF RE	24	Puncture rate found rising edge
STREAM1 LOCK RE	26	Stream lock rising edge
PLL LOCK RE	29	PLL lock rising edge

13 JTAG interface

The JTAG is compliant with the JTAG IEEE1149.1 standard, also called the boundary scan standard.

JTAG allows a control state-machine to be accessed through its test access port (TAP) to manage production boundary scan tests.

The STV0903 cut 2.0 JTAG identifier is 0xAD438041

The STV0903 cut 2.0 JTAG identifier is 0x9D438041

The STV0903 cut 1.x JTAG identifier is 0x0D438041.

The following mandatory IEEE instructions are available:

- bypass
- extest
- sample/preload.

Also, IDcode (and private register) is an additional recommended instruction.

Table 21. TAP control signals

Test signal names	Active	Description
TRSTN	L	Asynchronous TAP reset
TCK	H	Positive edge clock for TAP
TMS	-	Input TAP state-machine control
TDI	-	Scan input for instruction or data
TDO	-	Scan output for instruction or data: negative edge of TCK

Warning: Pin TRSTN must be tied low during normal operation. Allowing this pin to float or be pulled high causes the JTAG state machine to operate, causing anomalous behavior of the IC.

14 Electrical specifications

14.1 Absolute maximum ratings

Table 22. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{dd_1v0}	DC supply voltage	-0.1, +1.26	V
V_{dd_2v5}	DC supply voltage	-0.25, +2.75	V
V_{dd_3v3}	DC supply voltage	-0.3, +3.63	V
V_{in}	Voltage on input pins	-0.3, $V_{dd\_3.3}$ +0.3	V
t_{oper}	Operating ambient temperature	-10, +70	°C
t_{stg}	Storage temperature	-40, +150	°C
t_j	Junction temperature	+125	°C

14.2 Thermal data

Table 23. Thermal data

Symbol	Parameter	Maximum value	Unit
$r_{th(j-a)}$	Thermal resistance (junction-ambient)	23(1) 37(2)	°C/W °C/W
$r_{th(j-c)}$	Thermal resistance (junction-case)	2	°C/W

1. Four-layer PCB
2. Two-layer PCB

14.3 DC electrical specifications

Table 24. DC electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
v_{dd_1v0}	Digital core supply voltage	0.95	1.00	1.05	V
v_{dd_3v3}	Digital pads supply voltage	3.00	3.30	3.60	V
v_{dda_1v0}	Analog supply voltage	0.95	1.00	1.05	V
v_{dda_2v5}	Analog supply voltage	2.25	2.50	2.75	V
I/Os					
v_{il} v_{ih}	Input logic low Input logic high	-0.5 2.0		0.8 3.6	V V
v_{ol} v_{oh}	Output logic low Output logic high	-0.5 2.4		0.3 3.6	V V
i_{lk}	Input leakage current (v_{in} = 0 V to 3.3 V)	-15		+15	µA
i_{ol}	Output sink current			4	mA

Note: The 3.3-V digital I/Os comply to the JEDEC standard JESD8b.

Note: No constraint is placed on power supply power up sequence. However, Pin RESETB, the chip reset, must remain active (low) until at least 3 ms after the last power supply has stabilized (to 90% of its final value).

14.4 AC electrical specifications

The specifications given in *Table 25* below are valid for the operating conditions Tamb = 25° C and V_{dd_1v0} = 1.0 V, unless otherwise specified

Table 25. AC electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	CLK_IN or XTAL frequency	4	27/30	30	MHz
$I_{dd\_1v0\_rsta}$	Digital core supply current when reset pin active		13(1)		mA
$I_{dd\_1v0\_rst}$	Digital core supply current after reset		40		mA
$I_{dd\_1v0\_stb}$	Digital core supply current when in standby		40		mA
$I_{dd\_1v0\_1s1}$	Digital core supply current, DVBS active		0.3		A
$I_{dd\_1v0\_1s2}$	Digital core supply current, DVBS2 active		0.5	0.6(2)	A
$I_{dd\_1v0\_pk}$	Digital core supply current, peak			1.8(3)	A
I_{dd_3v3}	Digital pads supply current		30	40	mA
I_{dda_1v0}	Analog supply current		10	20	mA
I_{dda_2v5}	Analog supply current		70	80	mA
P_{max}	Maximum power			1.0	W
Vclk_i	CLK_I input amplitude(4)	2.25		3.6	Vpp
Vxtal_i	XTAL_I input amplitude(5)	2.2	2.5	2.8	Vpp

1. The crystal oscillator and clock output pin (to backend) are still active. All other circuits are shut down. This mode may be considered as the ultimate standby mode. The standby mode below does not shut down the main PLL or analogue functions allowing a rapid recovery from standby. Activiation from hardware reset takes a little longer.
2. Mean current consumption in DVB-S2 mode using ST software, lower throughput rates and noise conditions consume significantly lower current. The maximum indicates the maximum average (DC) current. The thermal constrains should be designed according to this figure.
3. Peak current consumption in DVB-S2 mode at FEC maximum throughput rate (190Mbits/s) and worse case noise conditions. The maximum indicates the maximum peek current called from the regulator. The regulator should be dimensioned to provide this maximum instantaneous value.
4. There is no phase noise requirement on CLK_I.
5. XTAL_I must have a low phase noise signal. This may come from a quartz driven by XTAL_O or an external source such as the STB6100, STV6110 or similar 8PSK compatible tuner. The OSC_I input is expected to be the reference for the internal PLL.

14.5 Dual ADC 8-bit specifications

Table 26. ADC specifications

Symbol	Parameter	Min	Typ	Max	Unit
	Resolution		8		bits
DC specifications					
DLE	Differential linearity error	-1.0		1.0	LSB
ILEpp	Integral linearity error, peak to peak	-4		4	LSB
	Gain error	-5		5	%FSR
Analog input					
	Differential input voltage mode 2 Vpp(1)			2.0	Vpp
	Differential input voltage mode 1 Vpp(1)			1.0	Vpp
	Input common mode voltage	1.0	1.25	1.5	V
	ADC differential input impedance (internal) Required external termination load		50 1		kΩ kΩ
	Input capacitance		2	3	pF
	Analog bandwidth	65		200	MHz
Switching performance					
	Maximum conversion rate	65	135	135	MHz
	Aperture uncertainty			2	ps RMS
	Duty cycle sampling clock			55	%
Dynamic performance					
ENOB	Effective number of bits	6.5	7.2	8	bits
SINAD	Signal-to-noise ratio with distortion	-44	-47		dB

1. The input range may be set through register bit TSTTRN1.ADC1_INMODE (F1E0[0]) (0 = 1 Vpp, 1 = 2 Vpp

14.6 Transport stream timing specifications

Table 27. Transport stream timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	CLK_IN or XTAL frequency (dispersion including thermal drift and aging)	-100 ppm	27	+100 ppm	MHz
Parallel output D[7:0], D/PN, CLKOUT, STROUT, ERROR output characteristics					
Bit CLKPOL = 0. Refer to *Figure 29*.					
t_{cksu}	Outputs stable before CLKOUT rising edge	5.0			ns
t_{ckh}	Outputs stable after CLKOUT rising edge	5.0			ns
Bit CLKPOL = 1. Refer to *Figure 29*.					
t_{cksu}	Outputs stable before CLKOUT falling edge	5.0			ns
t_{ckh}	Outputs stable after CLKOUT falling edge	5.0			ns
Serial output D[7] or D[0], D/PN, CLKOUT, STROUT, ERROR output characteristics					
Bit CLKPOL = 0 Refer to *Figure 30*.					
t_{cksu}	Outputs stable before CLKOUT rising edge	3.0			ns
t_{ckh}	Outputs stable after CLKOUT rising edge	3.0			ns
Bit CLKPOL = 1. Refer to *Figure 30*.					
t_{cksu}	Outputs stable before CLKOUT falling edge	3.0			ns
t_{ckh}	Outputs stable after CLKOUT falling edge	3.0			ns

Figure 29. Parallel output timing diagram

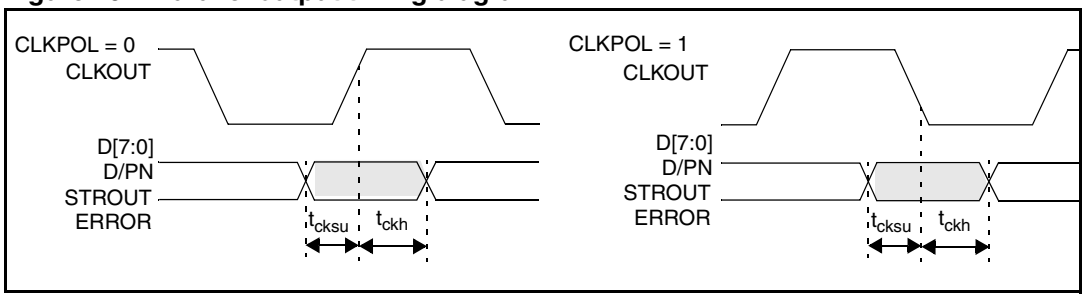
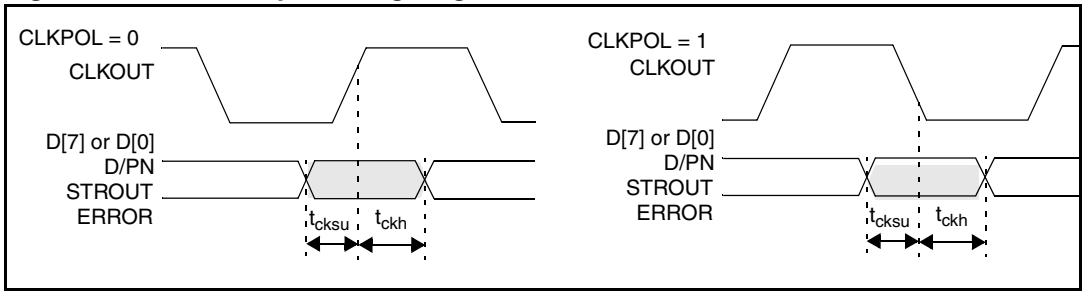


Figure 30. Serial output timing diagram

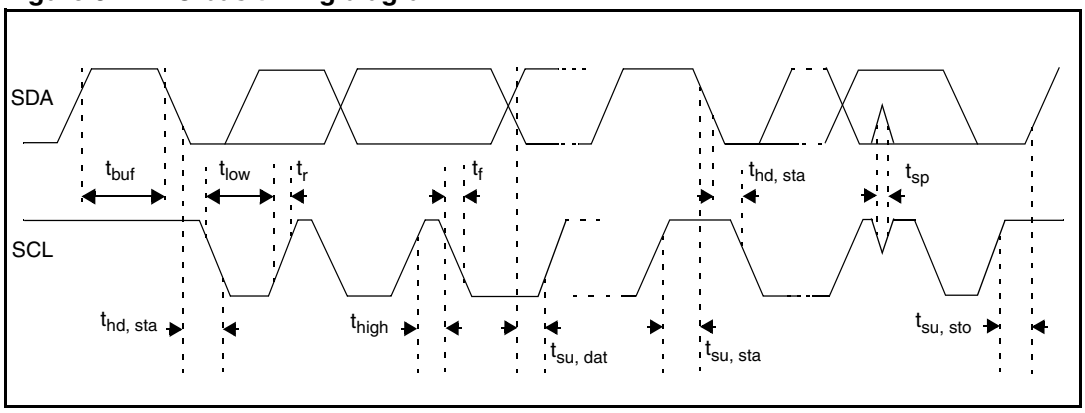


14.7 I²C bus specifications

Table 28. I²C bus specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{scl}	SCL clock frequency	Normal mode	0		400	kHz
t_{buf}	Bus free time between a stop and start condition		1.3			µs
$t_{hd, sta}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.		0.6			µs
t_{low} t_{high}	Low period of the SCL clock High period of the SCL clock		1.3 0.6			µs µs
t_r	Rise time for SDA and SCL signals	Fast mode			300	ns
t_f	Fall time for SDA and SCL signals	Fast mode			300	ns
$t_{su, sta}$	Setup time for a repeated start condition		0.6			µs
$t_{su, sto}$	Setup time for stop condition		0.6			µs
$t_{su, dat}$	Data setup time		100			ns
t_{sp}	Pulse width of spikes to be suppressed by input filter	Fast mode	0		50	ns

Figure 31. I²C bus timing diagram



14.8 Crystal oscillator specifications

Table 29. Crystal oscillator specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
A_{xtal_i}	Amplitude of signal on XTALI		0.8	1.3	1.5	V
A_{xtal_o}	Amplitude of signal on XTALO		1.0	1.7	2	V
t_{start}	Start-up time		0.4	0.47	1	ms
G_{mo}	Transconductance of oscillator		25	33	46	mA/V
R_{neg}	Negative impedance		140	230	260	Ω
G_{xtal_osc}	Crystal oscillator gain		9.5	13	14.4	dB

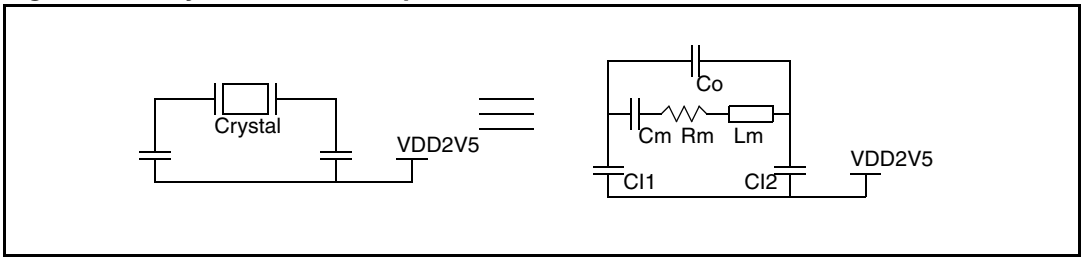
In order to guarantee start-up, the worst case transconductance of the oscillator (G_{mo}) must be at least 3 times greater than the critical transconductance (gm_crit) given by the quartz parameters. This must be verified before choosing a crystal. This figure can be calculated with the following formula (given CI1 = CI2 = CI):

$$gm\_crit = Rm * \omega^2 * (2 * Co + CI)^2$$

For design purposes a worst case crystal oscillator was assumed with the following parameters, as defined below in *Figure 32*:

Rm = 50 Ω
Lm = 5.69 mH
Cm = 4.95 fF
Co = 7 pF, parasitic capacitance of quartz package)
CI1 = CI2 = 38 pF (33 pF + 5 pF parasitics), capacitance on each resonator pad.

Figure 32. Crystal oscillator equivalent model



The crystal oscillator has been verified with the crystals in *Table 30* below to provide usage examples.

Table 30. Tested crystals and their parameters

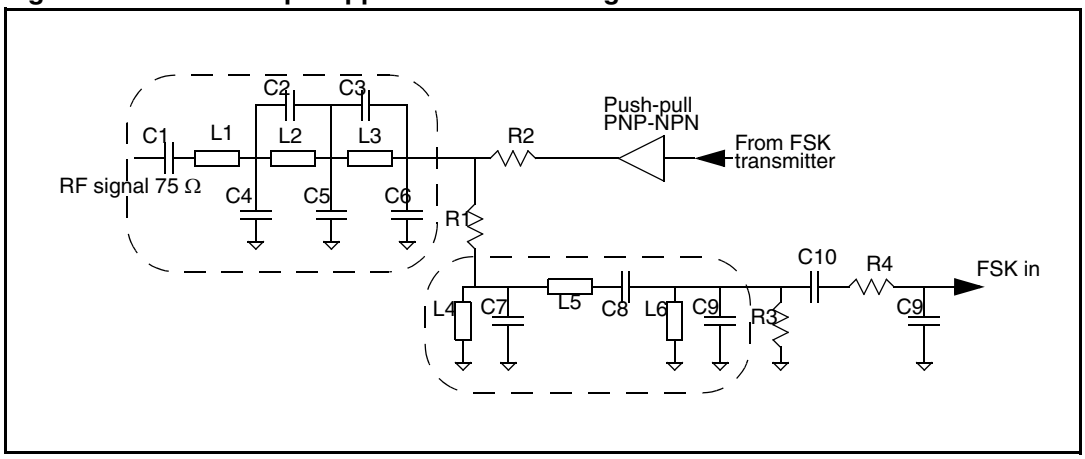
Supplier	Rm (Ω)	Lm (mH)	Cm (fF)	Co (pF)	Q (K)
Epson (E31821)	9.26	5.9	4.8	1.7	119
Raltron (R3000)	9.6	2.6	3.5	3.5	45
KSS (KSS3KF)	5	3.2	2.7	2.7	121

14.9 FSK receiver, transmitter specifications

Table 31. FSK specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{o_fsk}	Carrier frequency		1		7	MHz
Δf_fsk	Deviation frequency		8		250	kHz
Rx_{p_fsk}	Receive power	75 Ω	10		48	dBmV
Rx_{p_fsk}	Transmit power					dBmV

Figure 33. FSK example application circuit diagram



15 Package mechanical data

The package is an LQFP 14x14-128 lead (low profile flat pack) (14 x 14 x 1.4 mm^3) with exposed pad down. The JEDEC / EIAJ reference is JEDEC MS-026-AED-HD.

Table 32 on page 75 gives the values of the dimensions indicated in *Figure 34* below.

Figure 34. LQFP-128 EP package outline

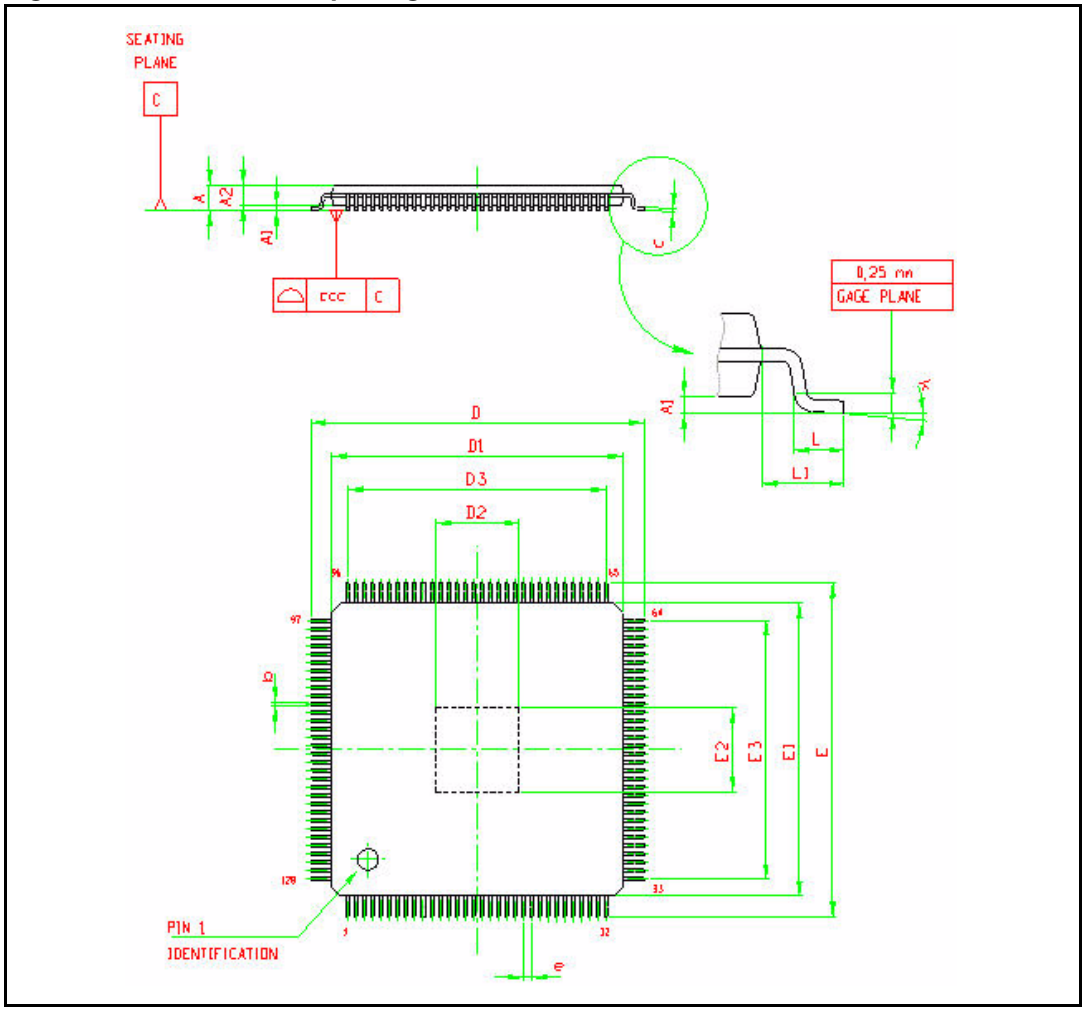


Table 32. LQFP-128 EP package dimensions

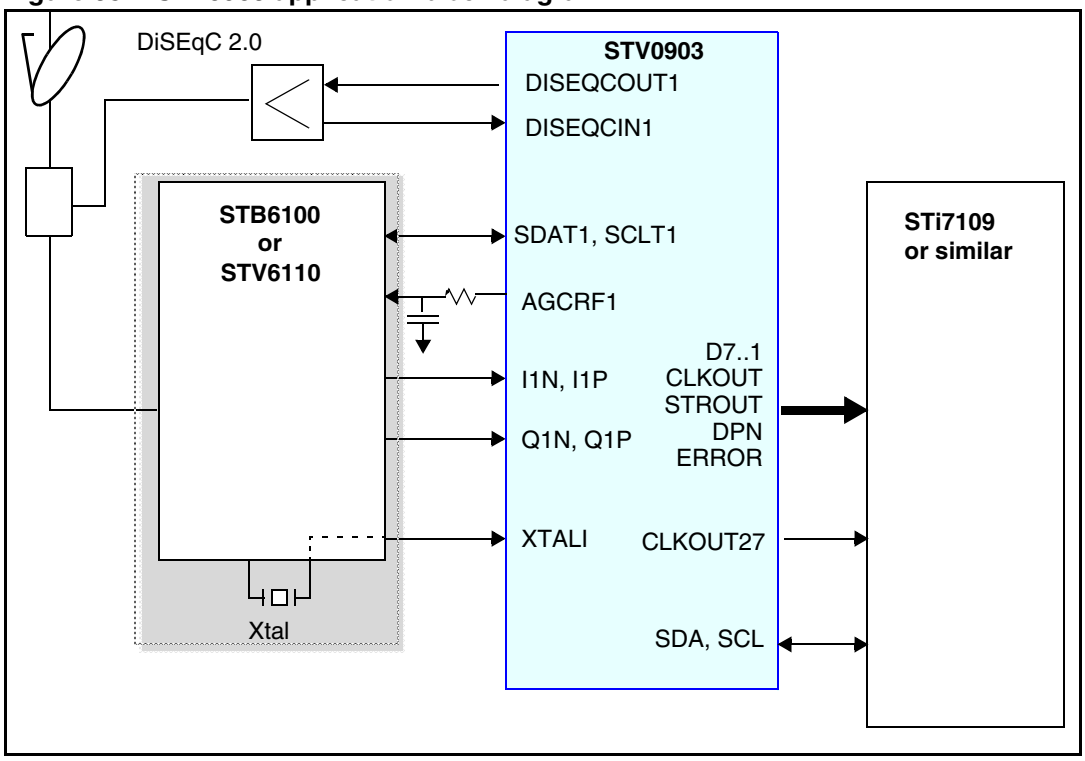
Reference	Dimensions (mm)		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09		0.20
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
D2	5.6	5.7	5.8
D3		12.40	
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
E2	5.6	5.7	5.8
E3		12.40	
e		0.40	
L	0.45	0.60	0.75
L1		1.00	
k	0	3.5	7
ccc			0.08

15.1 Environmentally-friendly packaging

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

16 Applications block diagram

Figure 35. STV0903 application block diagram



DVBS, DIRECTV legacy or DVBS2 decoding with serial or parallel TS output.

17 Registers

17.1 Register Summary

Table 33. SYS register list

Address	Register name	Description	Page
0xF100	MID	Chip identification	page 87
0xF113:0xF114	DACRx	DAC control	page 87
0xF11C	OUTCFG	Transport stream output configuration	page 88
0xF120:0xF123	IRQSTATUSx	Interrupt request status	page 89
0xF124:0xF127	IRQMASKx	Interrupt request mask	page 91
0xF129	I2CCFG	I2C bus configuration	page 92
0xF12A	I2CRPT	I2C bus repeater control	page 93
0xF138:0xF13E	IOPVALUEx	IO pin monitoring	page 94
0xF140	CLKI2CFG	CLKI2 IO control	page 95
0xF141:0xF14D	GPIOxCFG	General purpose IO control	page 96
0xF14E:0xF14F	CSxCFG	CSx IO control	page 96
0xF150	STDBYCFG	STANDBY IO control	page 97
0xF151	DIRCLKCFG	DIRCLK IO control	page 97
0xF152	AGCRF1CFG	AGCRF IO control	page 97
0xF153	SDAT1CFG	SDAT IO control	page 98
0xF154	SCLT1CFG	SCLT IO control	page 98
0xF155	DISEQCO1CFG	DISEQCO IO control	page 98
0xF15A	CLKOUT27CFG	CLKOUT27 IO control	page 99
0xF165	ERROR3CFG	ERROR IO control	page 99
0xF166	DPN3CFG	DPN IO control	page 100
0xF167	STROUT3CFG	STROUT IO control	page 100
0xF168	CLKOUT3CFG	CLKOUT IO control	page 100
0xF169	DATA73CFG	DATA7 IO control	page 101
0xF16A:0xF16C	STRSTATUSx	Stream status	page 101
0xF1B3	NCOARSE	Analog PLL divider control	page 102
0xF1B6	SYNTCTRL	Frequency synthesis control	page 102
0xF1B7	FILTCTRL	Filter control	page 103
0xF1B8	PLLSTAT	System clock status	page 103
0xF1C2	STOPCLK1	Stop clock control 1	page 104
0xF1C3	STOPCLK2	Stop clock control 2	page 104

Table 33. SYS register list

Address	Register name	Description	Page
0xF1DF	TSTTNR0	FSK analog cell test and configuration	page 105
0xF1E0	TSTTNR1	ADC 1 test and configuration	page 105
0xF1E1	TSTTNR2	DiSEqC 1 test and configuration	page 105
0xF1E2	TSTTNR3	ADC 2 test and configuration	page 106
0xF1E3	TSTTNR4	DiSEqC 2 test and configuration	page 106

Table 34. FSK register list

Address	Register name	Description	Page
0xF170:0xF172	FSKTFCx	FSK transmitter gain and carrier frequency	page 107
0xF173:0xF174	FSKTDELTAFx	FSK transmitter frequency deviation	page 107
0xF175	FSKTCTRL	FSK transmitter control	page 108
0xF176:0xF178	FSKRFCx	FSK receiver carrier frequency	page 109
0xF179	FSKRK1	FSK receiver K1	page 109
0xF17A	FSKRK2	FSK receiver K2	page 110
0xF17B	FSKRAGCR	FSK receiver AGC reference	page 110
0xF17C	FSKRAGC	FSK receiver AGC status	page 110
0xF17D	FSKRALPHA	FSK receiver alpha coefficient	page 111
0xF17E:0xF17F	FSKRPLTHx	FSK receiver beta coefficient and PLL threshold	page 111
0xF180:0xF181	FSKRDFx	FSK receiver frequency deviation	page 112
0xF182	FSKRSTEPP	FSK receiver positive step	page 112
0xF183	FSKRSTEPM	FSK receiver negative step	page 112
0xF184:0xF185	FSKRDETx	FSK receiver detection status	page 113
0xF186:0xF187	FSKRDTHx	FSK receiver carrier detection and loss threshold	page 113
0xF188	FSKRLOSS	FSK receiver carrier loss threshold	page 114

Table 35. DIS register list

Address	Register name	Description	Page
0xF1A0	DISTXCTL	DiSEqC transmitter control	page 115
0xF1A1	DISRXCTL	DiSEqC receiver control	page 116
0xF1A4	DISRX_ST0	DiSEqC receiver status0	page 117
0xF1A5	DISRX_ST1	DiSEqC receiver status1	page 117
0xF1A6	DISRXDATA	DiSEqC receiver FIFO	page 118
0xF1A7	DISTXDATA	DiSEqC transmitter FIFO	page 118
0xF1A8	DISTXSTATUS	DiSEqC transmitter status	page 118
0xF1A9	F22TX	DiSEqC 22 kHz transmitter frequency tone control	page 119
0xF1AA	F22RX	DiSEqC 22 kHz receiver frequency tone control	page 119

Table 35. DIS register list

Address	Register name	Description	Page
0xF1AC	ACRPRESC	Auxiliary clock control	page 119
0xF1AD	ACRDIV	Auxiliary clock division control	page 120

Table 36. DMD register list

Address	Register name	Description	Page
0xF400	IQCONST	Constellation editor configuration	page 121
0xF401	NOSCFG	Configuration of noise indicators	page 121
0xF402	ISYMB	Constellation editor I track	page 122
0xF403	QSYMB	Constellation editor Q track	page 122
0xF404	AGC1CFG	IQ mismatch control	page 123
0xF406	AGC1CN	AGC1 control	page 124
0xF407	AGC1REF	AGC1 reference	page 124
0xF408	IDCCOMP	DC compensation on I	page 125
0xF409	QDCCOMP	DC compensation on Q	page 125
0xF40A	POWERI	Power measured on I	page 125
0xF40B	POWERQ	Power measured on Q	page 126
0xF40C	AGC1AMM	Amplitude compensation of Q with respect to I	page 126
0xF40D	AGC1QUAD	Quadrature compensation of Q with respect to I	page 126
0xF40E	AGCIQIN1	AGC1 accumulator	page 127
0xF40F	AGCIQIN0	AGC1 accumulator	page 127
0xF410	DEMOD	General register for demodulator main functions	page 128
0xF411	DMDMODCOD	Override register for MODCOD&TYPE	page 129
0xF412	DSTATUS	Demodulator status 1	page 130
0xF413	DSTATUS2	Demodulator status 2	page 131
0xF414	DMDCFGMD	Demodulator configuration 1	page 132
0xF415	DMDCFG2	Demodulator configuration 2	page 133
0xF416	DMDISTATE	AEP launch register	page 133
0xF417	DMDT0M	Coarse carrier & symbol time constant	page 134
0xF41B	DMDSTATE	Step currently in progress in the demodulator general state machine	page 134
0xF41C	DMDFLYW	Demodulator status	page 135
0xF41D	DSTATUS3	Demodulator status 3	page 136
0xF41E	DMDCFG3	Demodulator configuration 3	page 136
0xF41F	DMDCFG4	Demodulator configuration 4	page 137
0xF420	CORRELMANT	Differential correlator limit mantissa	page 137
0xF421	CORRELABS	Absolute correlator limit mantissa	page 137

Table 36. DMD register list

Address	Register name	Description	Page
0xF422	CORRELEXP	Relative and absolute correlation limit exponents	page 138
0xF424	PLHMODCOD	Current MODCOD&TYPE, only DVBS2	page 139
0xF425	DMDREG	Various special cases	page 139
0xF42C	AGC2O	AGC2 configuration	page 140
0xF42D	AGC2REF	Demodulator general reference	page 140
0xF42E	AGC1ADJ	AGC1 set point	page 140
0xF436	AGC2I1	AGC2 accumulator	page 141
0xF437	AGC2I0	AGC2 accumulator	page 141
0xF438	CARCFG	Carrier 1 configuration	page 141
0xF439	ACLC	Alpha DVBS1/legacy DTV	page 142
0xF43A	BCLC	Beta DVBS1/legacy DTV	page 142
0xF43D	CARFREQ	Loop carrier 1 coefficients	page 143
0xF43E	CARHDR	PLHeader delta F coefficient in DVBS2	page 143
0xF43F	LDT	Positive edge of carrier lock detector	page 143
0xF440	LDT2	Negative edge of carrier lock detector	page 144
0xF441	CFRICFG	CFRINIT management configuration	page 144
0xF442	CFRUP1	Upper limit of carrier offset	page 144
0xF443	CFRUP0	Upper limit of carrier offset	page 145
0xF446	CFRLOW1	Lower limit of carrier offset	page 145
0xF447	CFRLOW0	Lower limit of carrier offset	page 145
0xF448	CFRINIT1	Carrier offset init value	page 146
0xF449	CFRINIT0	Carrier offset init value	page 146
0xF44A	CFRINC1	Carrier offset increment	page 146
0xF44B	CFRINC0	Carrier offset increment	page 147
0xF44C	CFR2	Current carrier offset (unit: samples)	page 147
0xF44D	CFR1	Current carrier offset (unit: samples)	page 147
0xF44E	CFR0	Current carrier offset (unit: samples)	page 148
0xF44F	LDI	Carrier lock indicator accumulator	page 148
0xF450	TMGCFG	Timing loop configuration	page 149
0xF451	RTC	Timing loop DVBS1/legacy DTV	page 149
0xF452	RTCS2	Timing loop specific to DVBS2	page 150
0xF453	TMGTHRISE	Postitive edge of timing lock detector	page 150
0xF454	TMGTHFALL	Negative edge of timing lock detector	page 150
0xF455	SFRUPRATIO	Ratio to calculate SFRUP	page 151
0xF456	SFRLOWRATIO	Ratio to calculate SFRLOW	page 151

Table 36. DMD register list

Address	Register name	Description	Page
0xF458	KREFTMG	Reference level for the symbol rate part of the coarse steps	page 151
0xF459	SFRSTEP	Scan and centering increment steps	page 152
0xF45A	TMGCFG2	Timing loop additional configuration	page 152
0xF45B	KREFTMG2	Coarse symbol rate reference frequency	page 153
0xF45E	SFRINIT1	Symbol rate init value	page 153
0xF45F	SFRINIT0	Symbol rate init value	page 153
0xF460	SFRUP1	Symbol rate upper limit	page 154
0xF461	SFRUP0	Symbol rate upper limit	page 154
0xF462	SFRLOW1	Symbol rate lower limit	page 155
0xF463	SFRLOW0	Symbol rate lower limit	page 155
0xF464	SFR3	Current symbol rate	page 156
0xF465	SFR2	Current symbol rate	page 156
0xF466	SFR1	Current symbol rate	page 156
0xF467	SFR0	Current symbol rate	page 157
0xF468	TMGREG2	Timing recovery accumulator	page 157
0xF469	TMGREG1	Timing recovery accumulator	page 157
0xF46A	TMGREG0	Timing recovery accumulator	page 158
0xF46B	TMGLOCK1	Timing lock indicator accumulator	page 158
0xF46C	TMGLOCK0	Timing lock indicator accumulator	page 158
0xF46D	TMGOBS	Observation of the timing loop	page 159
0xF46F	EQUALCFG	DFE equalizer configuration	page 159
0xF470:0F47E	EQUAIy	DFE Equalizer observation	page 160
0xF471:0F47F	EQUAQy	Equalizer observation	page 160
0xF480	NNOSDATAT1	Linear noise normalized on the data	page 160
0xF481	NNOSDATAT0	Linear noise normalized on the data	page 161
0xF482	NNOSDATA1	Quadratic noise normalized on the data	page 161
0xF483	NNOSDATA0	Quadratic noise normalized on the data	page 162
0xF484	NNOSPLHT1	Linear noise normalized on the structures	page 162
0xF485	NNOSPLHT0	Linear noise normalized on the structures	page 163
0xF486	NNOSPLH1	Quadratic noise normalized on the structures	page 163
0xF487	NNOSPLH0	Quadratic noise normalized on the structures	page 164
0xF488	NOSDATAT1	Absolute linear noise on the data	page 164
0xF489	NOSDATAT0	Absolute linear noise on the data	page 165
0xF48A	NOSDATA1	Absolute quadratic noise on the data	page 165

Table 36. DMD register list

Address	Register name	Description	Page
0xF48B	NOSDATA0	Absolute quadratic noise on the data	page 166
0xF48C	NOSPLHT1	Absolute linear noise on the structures	page 166
0xF48D	NOSPLHT0	Absolute linear noise on the structures	page 167
0xF48E	NOSPLH1	Absolute quadratic noise on the structures	page 167
0xF48F	NOSPLH0	Absolute quadratic noise on the structures	page 168
0xF490	CAR2CFG	Carrier loop 2 configuration	page 168
0xF491	CFR2CFR1	Carrier offset transfer control	page 169
0xF493	CFR22	Current carrier offset 2 (unit: symbols)	page 170
0xF494	CFR21	Current carrier offset 2 (unit: symbols)	page 170
0xF495	CFR20	Current carrier offset 2 (unit: symbols)	page 170
0xF497	ACLC2S2Q	Alpha specific DVBS2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)	page 171
0xF498	ACLC2S28	Alpha specific DVBS2 data 8PSK	page 171
0xF49C	BCLC2S2Q	Beta specific DVBS2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)	page 172
0xF49D	BCLC2S28	Beta specific DVBS2 data 8PSK	page 172
0xF4AC	PLROOT2	Gold code description	page 172
0xF4AD	PLROOT1	Gold code description	page 173
0xF4AE	PLROOT0	Gold code description	page 173
0xF4B0	MODCODLST0	List of prohibited MODCOD	page 173
0xF4B1	MODCODLST1	List of prohibited MODCOD	page 174
0xF4B2	MODCODLST2	List of prohibited MODCOD	page 174
0xF4B3	MODCODLST3	List of prohibited MODCOD	page 175
0xF4B4	MODCODLST4	List of prohibited MODCOD	page 175
0xF4B5	MODCODLST5	List of prohibited MODCOD	page 176
0xF4B6	MODCODLST6	List of prohibited MODCOD	page 176
0xF4B7	MODCODLST7	List of prohibited MODCOD	page 177
0xF4B8	MODCODLST8	List of prohibited MODCOD	page 177
0xF4B9	MODCODLST9	List of prohibited MODCOD	page 178
0xF4BA	MODCODLSTA	List of prohibited MODCOD	page 178
0xF4BB	MODCODLSTB	List of prohibited MODCOD	page 179
0xF4BC	MODCODLSTC	List of prohibited MODCOD	page 179
0xF4BD	MODCODLSTD	List of prohibited MODCOD	page 180
0xF4BE	MODCODLSTE	List of prohibited MODCOD	page 180
0xF4BF	MODCODLSTF	List of prohibited MODCOD	page 181

Table 36. DMD register list

Address	Register name	Description	Page
0xF4C0	GAUSSR0	Gaussien phase detector radius, R0	page 181
0xF4C1	CCIR0	CCI phase detector radius, R0	page 181
0xF4C2	CCIQUANT	CCI detector quantifier	page 182
0xF4C3	CCITHRES	CCI threshold detector level	page 182
0xF4C4	CCIACC	CCI detector accumulator	page 182
0xF4C6	DMDRESCFG	FIFO results configuration	page 183
0xF4C7	DMDRESADR	FIFO results status	page 183
0xF4C8..0xF4CF	DMDRESDATAy	FIFO results	page 184
0xF4D0..0xF4D6	FFEI1..4	FFE Equaliser coefficients	page 185
0xF4D1..0xF4D7	FFEQ1..4	FFE equaliser coefficients	page 185
0xF4D8	FFECFG	FFE equaliser configuration	page 185
0xF500	SMAPCOEF7	LLR gain in DVBS2 QPSK	page 186
0xF501	SMAPCOEF6	LLR gain in DVBS2 8PSK	page 186
0xF502	SMAPCOEF5	LLR gain in DVBS2 8PSK	page 187
0xF520	DMDPLHSTAT	PLHeaders failure rate	page 187
0xF522	LOCKTIME3	Demodulator locking time	page 188
0xF523	LOCKTIME2	Demodulator locking time	page 188
0xF524	LOCKTIME1	Demodulator locking time	page 188
0xF525	LOCKTIME0	Demodulator locking time	page 189

Table 37. TUN register list

Address	Register name	Description	Page
0xF4E0	TNRCFG	Tuner control configuration	page 190
0xF4E1	TNRCFG2	Tuner & input IQ control	page 191
0xF4E4	TNRXTAL	Tuner reference frequency	page 191
0xF4E7	TNRSTEPS	Step definition and various coefficients	page 192
0xF4E8	TNRGAIN	Tuner gain and various (static) characteristics	page 192
0xF4E9	TNRRF1	Tuner RF frequency (in MHz)	page 192
0xF4EA	TNRRF0	Tuner RF frequency (in MHz)	page 193
0xF4EB	TNRBW	Tuner bandwidth	page 193
0xF4EC	TNRADJ	Tuner specific register configurations	page 193
0xF4ED	TNRCTL2	CONTROL2 register of STV6110	page 194
0xF4EE	TNRCFG3	Additional tuner register configurations	page 194
0xF4F0	TNRLD	Tuner verification status (read only)	page 195

Table 37. TUN register list

Address	Register name	Description	Page
0xF4F6	TNROBSL	Control tuner observation	page 196
0xF4F7	TNRRESTE	RF frequency remainder	page 196

Table 38. DVB1 register list

Address	Register name	Description	Page
0xF532	VITSCALE	Additional configuration of Viterbi decoder	page 197
0xF533	FECM	Viterbi decoder configuration	page 198
0xF534	VTH12	Error threshold for puncture rate 1/2	page 198
0xF535	VTH23	Error threshold for puncture rate 2/3	page 198
0xF536	VTH34	Error threshold for puncture rate 3/4	page 199
0xF537	VTH56	Error threshold for puncture rate 5/6	page 199
0xF538	VTH67	Error threshold for puncture rate 6/7	page 199
0xF539	VTH78	Error threshold for puncture rate 7/8	page 200
0xF53A	VITCURPUN	Current puncture rate on the Viterbi decoder	page 200
0xF53B	VERROR	Current error rate	page 200
0xF53C	PRVIT	List of authorized puncture rates	page 201
0xF53D	VAVSRVIT	Viterbi decoder search speeds	page 202
0xF53E	VSTATUSVIT	Viterbi decoder status	page 203
0xF53F	VTHINUSE	Viterbi threshold currently in use	page 203
0xF540	KDIV12	Gain (k_divider) of puncture rate 1/2	page 203
0xF541	KDIV23	Gain (k_divider) of puncture rate 2/3	page 204
0xF542	KDIV34	Gain (k_divider) of puncture rate 3/4	page 204
0xF543	KDIV56	Gain (k_divider) of puncture rate 5/6	page 204
0xF544	KDIV67	Gain (k_divider) of puncture rate 6/7	page 205
0xF545	KDIV78	Gain (k_divider) of puncture rate 7/8	page 205

Table 39. DVB2 register list

Address	Register name	Description	Page
0xF550	PDELCTRL1	Packet delineator configuration	page 206
0xF551	PDELCTRL2	Packet delineator additional configuration	page 206
0xF554	HYSTTHRESH	pktdelin_lock signal hysteresis limits	page 207
0xF55E	ISIENTRY	MIS mode selection filter	page 207
0xF55F	ISIBITENA	MIS mode selection mask	page 208
0xF560	MATSTR1	MATYPE of the current frame	page 208
0xF561	MATSTR0	MATYPE of the current frame	page 208
0xF562	UPLSTR1	UPL of the current frame	page 209

Table 39. DVB2 register list

Address	Register name	Description	Page
0xF563	UPLSTR0	UPL of the current frame	page 209
0xF564	DFLSTR1	DFL of the current frame	page 209
0xF565	DFLSTR0	DFL of the current frame	page 210
0xF566	SYNCSTR	SYNC of the current frame	page 210
0xF567	SYNCDSTR1	SYNCD of the current frame	page 210
0xF568	SYNCDSTR0	SYNCD of the current frame	page 211
0xF569	PDELSTATUS1	Packet delineator status	page 211
0xF56A	PDELSTATUS2	Additional status for packet delineator	page 212
0xF56B	BBFCRCKO1	BBHeader KO counter	page 212
0xF56C	BBFCRCKO0	BBHeader KO counter	page 212
0xF56D	UPCRCKO1	Packet KO counter	page 213
0xF56E	UPCRCKO0	Packet KO counter	page 213
0xF56F	PDELCTRL3	Additional configuration of packet delineator	page 214
0xFA03:0xFA10	NBITER_NFx	Number of LDPC decoding iterations	page 214
0xFA3F	NBITERNOERR	LDPC decoding iteration stop criterion	page 215
0xFA43:0xFA50	GAINLLR_NFx	LDPC input LLR gain	page 216
0xFA80	CFGEXT	External data stream configuration	page 217
0xFA86	GENCFG	General configuration	page 218
0xFA96:0xFA97	LDPCERRx	LDPC error counter	page 218
0xFA98	BCHERR	BCH error	page 219

Table 40. TS register list

Address	Register name	Description	Page
0xF570	TSSTATEM	Configuration of merger-hardware stream line 1	page 220
0xF572	TSCFGH	Configuration of merger-hardware stream line 1	page 221
0xF573	TSCFGM	Configuration of merger-hardware stream line 1	page 222
0xF574	TSCFGL	Configuration of merger-hardware stream line 1	page 222
0xF576	TSINSDELH	Insertion/deletion mask of output packet parts	page 224
0xF579	TSDIVN	Output frequency control	page 224
0xF57A	TSCFG4	Stream merger line 1 hardware configuration	page 225
0xF580	TSSPEED	CLKOUT frequency	page 225
0xF581	TSSTATUS	Merger-hardware stream status	page 226
0xF582	TSSTATUS2	Additional status of merger-hardware stream	page 227
0xF583	TSBITRATE1	Observation of raw bit rate	page 227
0xF584	TSBITRATE0	Observation of raw bit rate	page 228

Table 40. TS register list

Address	Register name	Description	Page
0xF598	ERRCTRL1	Configuration of error counter 1	page 229
0xF599	ERRCNT12	Result of error counter 1	page 230
0xF59A	ERRCNT11	Result of error counter 1	page 230
0xF59B	ERRCNT10	Result of error counter 1	page 230
0xF59C	ERRCTRL2	Configuration of error counter 2	page 231
0xF59D	ERRCNT22	Result of error counter 2	page 231
0xF59E	ERRCNT21	Result of error counter 2	page 231
0xF59F	ERRCNT20	Result of error counter 2	page 232
0xF5A0	FECSPY	FEC spy configuration	page 232
0xF5A1	FSPYCFG	FEC spy configuration	page 233
0xF5A2	FSPYDATA	Tested packet contents	page 234
0xF5A3	FSPYOUT	FEC spy miscellaneous configuration	page 235
0xF5A4	FSTATUS	FEC spy status	page 236
0xF5A8	FBERCPT4	BER/PER meter byte counter	page 237
0xF5A9	FBERCPT3	BER/PER meter byte counter	page 237
0xF5AA	FBERCPT2	BER/PER meter byte counter	page 237
0xF5AB	FBERCPT1	BER/PER meter byte counter	page 238
0xF5AC	FBERCPT0	BER/PER meter byte counter	page 238
0xF5AD	FBERERR2	BER/PER meter error bit counter	page 239
0xF5AE	FBERERR1	BER/PER meter error bit counter	page 239
0xF5AF	FBERERR0	BER/PER meter error bit counter	page 240
0xF5B2	FSPYBER	BER/PER meter configuration	page 241
0xF600	RCCFG2	Configuration of the merger-hardware stream return channel line	page 241
0xF630	TSGENERAL	General configuration of the stream merger hardware	page 242

Table 41. TST register list

Address	Register name	Description	Page
0xFF11	TSTRES0	Test reset control 0	page 243
0xFF48	TCTL4		page 243
0xFF67	TSTDISRX	Test DiSEqC Rx configuration	page 244

17.2 SYS register descriptions

MID — Chip identification

7	6	5	4	3	2	1	0
MCHIP_IDENT				MRELEASE			
R				R			

Address: 0xF100

Type: R

Reset: 0x30

Description: This represents the ID and release number. For example, a 2.3 release would be read 0x23.

[7:4] MCHIP_IDENT: Base layer version (unsigned)

[3:0] MRELEASE: Metal fix version (unsigned)

DACRx — DAC control

	7	6	5	4	3	2	1	0
DACR1	DAC_MODE			RESERVED	DAC_VALUE[11:8]			
	R/W			R	R/W			

	7	6	5	4	3	2	1	0
DACR2	DAC_VALUE[7:0]							
	R/W							

Address: 0xF113(x=1), 0xF114(x=2)

Type: R/W

Reset: 0x0

Description: DACR1 and DACR2 generate a sigma-delta digital signal to be output to any of the GPIOs

DACR1: [7:5] DAC_MODE: Controls the clock frequency used to generate DAC_VALUE
110: mclk/4
101: mclk/8
100: mclk/32 (unsigned)

DACR1: [3:0]
DACR2: [7:0] DAC_VALUE: DAC value (unsigned)

OUTCFG Transport stream output configuration

7	6	5	4	3	2	1	0
RESERVED			OUTSERRS3_HZ	OUTPARRS3_HZ	RESERVED		
R			R/W	R/W	R		

Address: 0xF11C

Type: R/W

Reset: 0x7A

Description: Transport stream (TS) output configuration

[4] OUTSERRS3_HZ: 1: sets Transport Stream 3 pins to high impedance
0: sets Transport Stream 3 pins to push-pull (unsigned)

[3] OUTPARRS3_HZ: 1: sets Transport Stream 3 parallel pins in high impedance
0: sets Transport Stream 3 parallel pins in push-pull (unsigned)

IRQSTATUSx Interrupt request status

	7	6	5	4	3	2	1	0
IRQSTATUS3	RESERVED		SPLL_LOCK	SSTREAM_LCK_3	RESERVED			SDVBS1_PRF_1
	R		R	R	R			R

	7	6	5	4	3	2	1	0
IRQSTATUS2	SSPY_ENDSIM_3	RESERVED					SPKTDEL_ERROR_1	SPKTDEL_LOCKB_1
	R	R					R	R

	7	6	5	4	3	2	1	0
IRQSTATUS1	SPKTDEL_LOCK_1	RESERVED						
	R	R						

	7	6	5	4	3	2	1	0
IRQSTATUS0	SDEMOD_LOCKB_1	SDEMOD_LOCK_1	SDEMOD_IRQ_1	SBCH_ERRFLAG	RESERVED		SDISEQC1RX_IRQ	SDISEQC1TX_IRQ
	R	R	R	R	R		R	R

Address: 0xF120(x=3), 0xF121(x=2), 0xF122(x=1), 0xF123(x=0)

Type: R

Reset: Undefined

Description: Status register block giving the list of currently pending interrupt request occurences.
0: no interrupt request detected since last erase of this bit.
1: an interrupt request has been detected since last erase of this bit. The bits of these registers are reset to 0 when the register is read from or written to.

IRQSTATUS3: [5] SPLL_LOCK: 1: PLL is locked (read put to 0 on a read,unsigned)

IRQSTATUS3: [4] SSTREAM_LCK_3: 1: transport stream 3 is locked (read put to 0 on a read,unsigned)

IRQSTATUS3: [0] SDVBS1_PRF_1: 1: dvbs1 block 1 has found the puncture rate (read put to 0 on a read,unsigned)

IRQSTATUS2: [7] SSPY_ENDSIM_3: 1: fec spy 3 has finished (read put to 0 on a read,unsigned)

IRQSTATUS2: [1] SPKTDEL_ERROR_1: 1: dvbs2 packet delineator 1 error (read put to 0 on a read,unsigned)

IRQSTATUS2: [0] SPKTDEL_LOCKB_1: 1: dvbs2 packet delineator 1 is unlocked (read put to 0 on a read,unsigned)

IRQSTATUS1: [7] SPKTDEL_LOCK_1: 1: dvbs2 packet delineator 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS0: [7] SDEMOD_LOCKB_1: 1: demod block 1 is unlocked (read put to 0 on a read,unsigned)

IRQSTATUS0: [6] SDEMOD_LOCK_1: 1: demod block 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS0: [5] SDEMOD_IRQ_1: demod block 1 irq value (read put to 0 on a read,unsigned)

IRQSTATUS0: [4] SBCH_ERRFLAG: 1: dvbs2 bch has an error (read put to 0 on a read,unsigned)

IRQSTATUS0: [1] SDISEQC1RX_IRQ: diseqc block 1 rx irq value (read put to 0 on a read,unsigned)

IRQSTATUS0: [0] SDISEQC1TX_IRQ: diseqc block 1 rx irq value (read put to 0 on a read,unsigned)

IRQMASKx Interrupt request mask

	7	6	5	4	3	2	1	0
IRQMASK3	RESERVED		MPLL_LOCK	MSTREAM_LCK_3	RESERVED			MDVBS1_PRF_1
	R		R/W	R/W	R			R/W

	7	6	5	4	3	2	1	0
IRQMASK2	MSPY_ENDSIM_3	RESERVED					MPKTDEL_ERROR_1	MPKTDEL_LOCKB_1
	R/W	R					R/W	R/W

	7	6	5	4	3	2	1	0
IRQMASK1	MPKTDEL_LOCK_1	RESERVED		MEXTPINB1	MEXTPIN1	RESERVED		
	R/W	R		R/W	R/W	R		

	7	6	5	4	3	2	1	0
IRQMASK0	MDEMOD_LOCKB_1	MDEMOD_LOCK_1	MDEMOD_IRQ_1	MBCH_ERRFLAG	RESERVED		MDISEQC1RX_IRQ	MDISEQC1TX_IRQ
	R/W	R/W	R/W	R/W	R		R/W	R/W

Address: 0xF124(x=3), 0xF125(x=2), 0xF126(x=1), 0xF127(x=0)

Type: R/W

Reset: 0x3F, 0xFF, 0xFF, 0xFF

Description: Enable interrupt mask. These registers give the list of interrupt request occurences which are enabled to generate the IRQ signal.
1: interrupt request enabled to generate IRQ signal.
0: interrupt request not enabled to generate IRQ signal.

I2CCFG I2C bus configuration

7	6	5	4	3	2	1	0
RESERVED				I2C_FASTMODE	RESERVED	I2CADDR_INC	
R				R/W	R	R/W	

Address: 0xF129

Type: R/W

Reset: 0x88

Description: I2C bus configuration

[3] I2C_FASTMODE: 1: I2C bus is in fast mode (default recommended mode). The oversampling ratio of the I2C bus rate is 1/16 of the master clock.
0: I2C bus oversampling ratio 1/41 of the master clock. (unsigned)

[1:0] I2CADDR_INC: controls the auto-increment value for burst access modes.
00: default, +1 increment.
01: stop increment mode, automatic increment is frozen.
10: reserved
11: reserved. (unsigned)

I2CRPT I2C bus repeater control

7	6	5	4	3	2	1	0
I2CT_ON	ENARPT_LEVEL			SCLT_DELAY	STOP_ENABLE	STOP_SDAT2SDA	RESERVED
R/W	R/W			R/W	R/W	R/W	R

Address: 0xF12A

Type: R/W

Reset: 0xB2

Description: I2C bus repeater control

[7] I2CT_ON: 1: repeater is turned on.
This bit is automatically set to 0 when STOP_ENABLE = 1 by a stop event on the SDA line. (unsigned)

[6:4] ENARPT_LEVEL: the speed of the I2C repeater obtained by dividing the internal chip frequency (that is, 135 MHz).
000: divide by 256 (slow)
001: divide by 128
010: divide by 64
011: divide by 32
100: divide by 16
101: divide by 8
110: divide by 4
111: divide by 2 (very fast) (unsigned)

[3] SCLT_DELAY: SCL to SCLT signal transmission mode (SCLT2, for P2).
0: SCLT line is not delayed (default).
1: SCLT line is delayed with the same enarpt_level delay as SDAT. (unsigned)

[2] STOP_ENABLE: I2C repetition end mode.
0: manual: end of repetition when I2CT_ON is set to 0 by software, so several I2C accesses can be transmitted.
1: automatic: end of repetition on the next stop event on SDA line. (unsigned)

[1] STOP_SDAT2SDA: stop propagation from SDAT to SDA (SDAT2 for P2) line.
0: bidirectional mode: data is transferred from SDAT to SDA and SDA to SDAT.
1: monodirectional mode: data is never transferred from SDAT to SDA. (unsigned)

IOPVALUEx IO pin monitoring

	7	6	5	4	3	2	1	0
IOPVALUE6	RESERVED					VSCL	VSDA	VDATA3_0
	R					R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE5	VDATA3_1	VDATA3_2	VDATA3_3	VDATA3_4	VDATA3_5	VDATA3_6	VDATA3_7	VCLKOUT3
	R	R	R	R	R	R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE4	VSTROUT3	VDPN3	VERROR3	VDATA2_7	VCLKOUT2	VSTROUT2	VDPN2	VERROR2
	R	R	R	R	R	R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE3	VDATA1_7	VCLKOUT1	VSTROUT1	VDPN1	VERROR1	VCLKOUT27	VDISEQCOUT2	VSCLT2
	R	R	R	R	R	R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE2	VSDAT2	VAGCRF2	VDISEQCOUT1	VSCLT1	VSDAT1	VAGCRF1	VDIRCLK	VSTDBY
	R	R	R	R	R	R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE1	VCS1	VCS0	VGPIO13	VGPIO12	VGPIO11	VGPIO10	VGPIO9	VGPIO8
	R	R	R	R	R	R	R	R

	7	6	5	4	3	2	1	0
IOPVALUE0	VGPIO7	VGPIO6	VGPIO5	VGPIO4	VGPIO3	VGPIO2	VGPIO1	VCLKI2
	R	R	R	R	R	R	R	R

Address: 0xF13E - x * 0x1 (x=0 to 6)

Type: R

Reset: Undefined

Description: The value currently presented to the digital pin (high =1, low = 0) is reported. The field name indicates the pin reported.

IOPVALUE6: [2] VSCL: (unsigned)

IOPVALUE6: [1] VSDA: (unsigned)

IOPVALUE6: [0] VDATA3_0: (unsigned)

IOPVALUE5: [7] VDATA3_1: (unsigned)

IOPVALUE5: [6] VDATA3_2: (unsigned)

IOPVALUE5: [5] VDATA3_3: (unsigned)

IOPVALUE5: [4] VDATA3_4: (unsigned)

IOPVALUE5: [3] VDATA3_5: (unsigned)

IOPVALUE5: [2] VDATA3_6: (unsigned)

IOPVALUE5: [1] VDATA3_7: (unsigned)

IOPVALUE5: [0] VCLKOUT3: (unsigned)
IOPVALUE4: [7] VSTROUT3: (unsigned)
IOPVALUE4: [6] VDPN3: (unsigned)
IOPVALUE4: [5] VERROR3: (unsigned)
IOPVALUE4: [4] VDATA2_7: (unsigned)
IOPVALUE4: [3] VCLKOUT2: (unsigned)
IOPVALUE4: [2] VSTROUT2: (unsigned)
IOPVALUE4: [1] VDPN2: (unsigned)
IOPVALUE4: [0] VERROR2: (unsigned)
IOPVALUE3: [7] VDATA1_7: (unsigned)
IOPVALUE3: [6] VCLKOUT1: (unsigned)
IOPVALUE3: [5] VSTROUT1: (unsigned)
IOPVALUE3: [4] VDPN1: (unsigned)
IOPVALUE3: [3] VERROR1: (unsigned)
IOPVALUE3: [2] VCLKOUT27: (unsigned)
IOPVALUE3: [1] VDISEQCOUT2: (unsigned)
IOPVALUE3: [0] VSCLT2: (unsigned)
IOPVALUE2: [7] VSDAT2: (unsigned)
IOPVALUE2: [6] VAGCRF2: (unsigned)
IOPVALUE2: [5] VDISEQCOUT1: (unsigned)
IOPVALUE2: [4] VSCLT1: (unsigned)
IOPVALUE2: [3] VSDAT1: (unsigned)
IOPVALUE2: [2] VAGCRF1: (unsigned)
IOPVALUE2: [1] VDIRCLK: (unsigned)
IOPVALUE2: [0] VSTDBY: (unsigned)
IOPVALUE1: [7:6] VCS[1:0]: (unsigned)
IOPVALUE1: [5:0] VGPIO[13:8]: (unsigned)
IOPVALUE0: [7:1] VGPIO[7:1]: (unsigned)
IOPVALUE0: [0] VCLKI2: (unsigned)

CLKI2CFG — CLKI2 IO control

7	6	5	4	3	2	1	0
CLKI2_OPD	CLKI2_CONFIG						CLKI2_XOR
R/W	R/W						R/W

Address: 0xF140
Type: R/W
Reset: 0x82

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin CLKI2.

[7] CLKI2_OPD: (unsigned)

[6:1] CLKI2_CONFIG: (unsigned)

[0] CLKI2_XOR: (unsigned)

GPIOxCFG General purpose IO control

	7	6	5	4	3	2	1	0
GPIOxCFG	GPIOx_OPD	GPIOx_CONFIG						GPIOx_XOR
	R/W	R/W						R/W

Address: 0xF141 + (x-1) * 0x1 (x=1 to 13)

Type: R/W

Reset: 0x82

Description: Control for configurations of pins GPIOx (GPIO01 to GPIO13). See chapter 11 for more details.

GPIOxCFG: [7] GPIO1_OPD: open-drain configuration of GPIO pin
0: push-pull
1: open drain (unsigned)

GPIOxCFG: [6:1] GPIO1_CONFIG: general purpose input and output configuration. (unsigned)

GPIOxCFG: [0] GPIO1_XOR: XOR the result of GPIOCFG configuration.
0: no change
1: invert the logical value. (unsigned)

CSxCFG CSx IO control

	7	6	5	4	3	2	1	0
CS0CFG	CS0_OPD	CS0_CONFIG						CS0_XOR
CS1CFG	CS1_OPD	CS1_CONFIG						CS1_XOR
	R/W	R/W						R/W

Address: 0xF14E(x=0), 0xF14F(x=1)

Type: R/W

Reset: 0x82

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin CSx.

[7] CSx_OPD: (unsigned)

[6:1] CSx_CONFIG: (unsigned)

[0] CSx_XOR: (unsigned)

STDBYCFG STANDBY IO control

7	6	5	4	3	2	1	0
STDBY_OPD	STDBY_CONFIG						STBDY_XOR
R/W	R/W						R/W

Address: 0xF150

Type: R/W

Reset: 0x82

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin STDBY.

[7] STDBY_OPD: (unsigned)

[6:1] STDBY_CONFIG: (unsigned)

[0] STBDY_XOR: (unsigned)

DIRCLKCFG DIRCLK IO control

7	6	5	4	3	2	1	0
DIRCLK_OPD	DIRCLK_CONFIG						DIRCLK_XOR
R/W	R/W						R/W

Address: 0xF151

Type: R/W

Reset: 0x82

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin DIRCLK.

[7] DIRCLK_OPD: (unsigned)

[6:1] DIRCLK_CONFIG: (unsigned)

[0] DIRCLK_XOR: (unsigned)

AGCRF1CFG AGCRF IO control

7	6	5	4	3	2	1	0
AGCRF1_OPD	AGCRF1_CONFIG						AGCRF1_XOR
R/W	R/W						R/W

Address: 0xF152

Type: R/W

Reset: 0x91

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin AGCRF1.

[7] AGCRF1_OPD: (unsigned)

[6:1] AGCRF1_CONFIG: (unsigned)

[0] AGCRF1_XOR: (unsigned)

SDAT1CFG — SDAT IO control

7	6	5	4	3	2	1	0
SDAT1_OPD	SDAT1_CONFIG						SDAT1_XOR
R/W	R/W						R/W

Address: 0xF153

Type: R/W

Reset: 0xB0

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin SDAT1.

[7] SDAT1_OPD: (unsigned)

[6:1] SDAT1_CONFIG: (unsigned)

[0] SDAT1_XOR: (unsigned)

SCLT1CFG — SCLT IO control

7	6	5	4	3	2	1	0
SCLT1_OPD	SCLT1_CONFIG						SCLT1_XOR
R/W	R/W						R/W

Address: 0xF154

Type: R/W

Reset: 0xB2

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin SCLT1.

[7] SCLT1_OPD: (unsigned)

[6:1] SCLT1_CONFIG: (unsigned)

[0] SCLT1_XOR: (unsigned)

DISEQCO1CFG — DISEQCO IO control

7	6	5	4	3	2	1	0
DISEQCO1_OPD	DISEQCO1_CONFIG						DISEQC1_XOR
R/W	R/W						R/W

Address: 0xF155

Type: R/W

Reset: 0x14

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin DESEQCO1.

[7] DISEQCO1_OPD: (unsigned)

[6:1] DISEQCO1_CONFIG: (unsigned)

[0] DISEQC1_XOR: (unsigned)

CLKOUT27CFG — CLKOUT27 IO control

7	6	5	4	3	2	1	0
CLKOUT27_OPD	CLKOUT27_CONFIG						CLKOUT27_XOR
R/W	R/W						R/W

Address: 0xF15A

Type: R/W

Reset: 0x7E

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin CLKOUT27.

[7] CLKOUT27_OPD: (unsigned)

[6:1] CLKOUT27_CONFIG: (unsigned)

[0] CLKOUT27_XOR: (unsigned)

ERROR3CFG — ERROR IO control

7	6	5	4	3	2	1	0
ERROR3_OPD	ERROR3_CONFIG						ERROR3_XOR
R/W	R/W						R/W

Address: 0xF165

Type: R/W

Reset: 0xD8

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin ERROR3.

[7] ERROR3_OPD: (unsigned)

[6:1] ERROR3_CONFIG: (unsigned)

[0] ERROR3_XOR: (unsigned)

DPN3CFG — DPN IO control

7	6	5	4	3	2	1	0
DPN3_OPD	DPN3_CONFIG						DPN3_XOR
R/W	R/W						R/W

Address: 0xF166

Type: R/W

Reset: 0xD4

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin DPN3.

[7] DPN3_OPD: (unsigned)

[6:1] DPN3_CONFIG: (unsigned)

[0] DPN3_XOR: (unsigned)

STROUT3CFG — STROUT IO control

7	6	5	4	3	2	1	0
STROUT3_OPD	STROUT3_CONFIG						STROUT3_XOR
R/W	R/W						R/W

Address: 0xF167

Type: R/W

Reset: 0xD6

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin STROUT3.

[7] STROUT3_OPD: (unsigned)

[6:1] STROUT3_CONFIG: (unsigned)

[0] STROUT3_XOR: (unsigned)

CLKOUT3CFG — CLKOUT IO control

7	6	5	4	3	2	1	0
CLKOUT3_OPD	CLKOUT3_CONFIG						CLKOUT3_XOR
R/W	R/W						R/W

Address: 0xF168

Type: R/W

Reset: 0xDA

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin CLKOUT3.

[7] CLKOUT3_OPD: (unsigned)

[6:1] CLKOUT3_CONFIG: (unsigned)

[0] CLKOUT3_XOR: (unsigned)

DATA73CFG DATA7 IO control

7	6	5	4	3	2	1	0
DATA73_OPD	DATA73_CONFIG						DATA73_XOR
R/W	R/W						R/W

Address: 0xF169

Type: R/W

Reset: 0xDC

Description: This register is used in the same way as registers GPIOxCFG, for reconfiguring pin DATA73.

[7] DATA73_OPD: (unsigned)

[6:1] DATA73_CONFIG: (unsigned)

[0] DATA73_XOR: (unsigned)

STRSTATUSx Stream status

	7	6	5	4	3	2	1	0
STRSTATUS1	STRSTATUS_SEL2				STRSTATUS_SEL1			
STRSTATUS2	STRSTATUS_SEL4				STRSTATUS_SEL3			
STRSTATUS3	STRSTATUS_SEL6				STRSTATUS_SEL5			
	R/W				R/W			

Address: 0xF16A(x=1), 0xF16B(x=2), 0xF16C(x=3)

Type: R/W

Reset: 0x60, 0x71, 0x82

Description: Configure what information will be available when selecting streamstatus1..6 GPIO functions :

0: DEMOD_SYMIQ1 - Demodulator 1 detected an IQ inversion
1: DEMOD_LOCKED1 - Demodulator 1 locked flag
2: DEMOD_FAIL1 - Demodulator 1 failed flag
3: PKTDEL_LOCKED1 - Packet delineator 1 locked flag
4: PKTDEL_ERROR1 - Packet delineator 1 error flag
5: VITERBI_PRF1 - DVBS1 Viterbi 1 puncture rate found flag
6: DEMOD_SYMIQ2 - Demodulator 2 detected an IQ inversion
7: DEMOD_LOCKED2 - Demodulator 2 locked flag
8: DEMOD_FAIL2 - Demodulator 2 failed flag
9: PKTDEL_LOCKED2 - Packet delineator 2 locked flag
10: PKTDEL_ERROR2 - Packet delineator 2 error flag
11: VITERBI_PRF2 - DVBS1 Viterbi 2 puncture rate found flag
12: STREAM_LOCKED1 - Stream 1 (return channel) locked flag (up to transport)
13: STREAM_LOCKED2 - Stream 2 locked flag (up to transport)
14: STREAM_LOCKED3 - Stream 3 locked flag (up to transport)
15: Reserved

STRSTATUS1: [7:0] STRSTATUS_SEL[2:1]: (unsigned)

STRSTATUS2: [7:0] STRSTATUS_SEL[4:3]: (unsigned)

STRSTATUS3: [7:0] STRSTATUS_SEL[6:5]: (unsigned)

NCOARSE Analog PLL divider control

7	6	5	4	3	2	1	0
M_DIV							
R/W							

Address: 0xF1B3

Type: R/W

Reset: 0x13

Description: Analog PLL divider control

[7:0] M_DIV: PLL Divider
Fmclk = Fref x (m_div + 1) / 6 if SYNTCTRL.selx1ratio = 0
Fmclk = Fref x (m_div + 1) / 4 if SYNTCTRL.selx1ratio = 1
Fmclk2 = 2 x Fmclk. (unsigned)

SYNTCTRL Frequency synthesis control

7	6	5	4	3	2	1	0
STANDBY	BYPASSPLLCORE	SELX1RATIO	RESERVED	STOP_PLL	BYPASSPLLFSK	SELOSCI	BYPASSPLLADC
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Address: 0xF1B6

Type: R/W

Reset: 0x62

Description: Frequency synthesis control

[7] STANDBY: stop all clocks except I2C clock.
0: device active
1: device in standby (unsigned)

[6] BYPASSPLLCORE: controls the digital clocks
1: PLL is bypassed (external clocks)
0: digital clocks from PLL (unsigned)

[5] SELX1RATIO: control PLL pre-dividers
see NCOARSE for clock freq. equation (unsigned)

[3] STOP_PLL: 1: the analog PLL is stopped (unsigned)

[2] BYPASSPLLFSK: controls the FSK clock
1: PLL is bypassed (external clock)
0: FSK clock from PLL (unsigned)

[1] SELOSCI: PLL input pin selection
0: input clock comes from CLKI pin
1: input clock comes from XTALI pin (unsigned)

[0] BYPASSPLLADC: controls the ADC clock
1: PLL is bypassed (external clock)
0: ADC clock from PLL (unsigned)

FILTCTRL Filter control

7	6	5	4	3	2	1	0
INV_CLK135	RESERVED				SEL_FSKCKDIV	INV_CLKFSK	BYPASS_APPLI
R/W	R				R/W	R/W	R/W

Address: 0xF1B7

Type: R/W

Reset: 0x1

Description: Filter control

[7] INV_CLK135: 1: invert the external 135 MHz clock from pin CLKI (unsigned)

[2] SEL_FSKCKDIV: 1: clock fsk is Fmclk divided by 2
0: clock FSK is Fmclk (unsigned)

[1] INV_CLKFSK: 1: inverts the FSK clock (unsigned)

[0] BYPASS_APPLI: control external clocks
1: when PLL is bypassed, the clocks are derived from one external clock on pin CLKI which should be at a frequency = Fmclk * 2
0: when PLL is bypassed, two clocks are provided on pins CLKI and CLKI2 (CLKI = Fmclk * 2, CLKI2 = Fmclk) (unsigned)

PLLSTAT System clock status

7	6	5	4	3	2	1	0
RESERVED							PLLLOCK
R							R

Address: 0xF1B8

Type: R

Reset: Undefined

Description: System clock status

[0] PLLLOCK: 1: the PLL is locked
0: the PLL is unlocked (unsigned)

STOPCLK1 Stop clock control 1

7	6	5	4	3	2	1	0
RESERVED		STOP_CLKPKDT1	STOP_CLKFEC	RESERVED	INV_CLKADCI2	STOP_CLKADCI1	INV_CLKADCI1
R		R/W	R/W	R	R/W	R/W	R/W

Address: 0xF1C2

Type: R/W

Reset: 0x0

Description: Stop clock control 1

[5] STOP_CLKPKDT1: 1: stops the packet delineator 1 clock (unsigned)

[4] STOP_CLKFEC: 1: stops the DVBS2 FEC clock (unsigned)

[2] INV_CLKADCI2: 1: inverts the ADC interface 2 clock (unsigned)

[1] STOP_CLKADCI1: 1: stops the ADC interface 1 clock (unsigned)

[0] INV_CLKADCI1: 1: inverts the ADC interface 1 clock (unsigned)

STOPCLK2 Stop clock control 2

7	6	5	4	3	2	1	0
RESERVED				STOP_CLKSAMP1	RESERVED	STOP_CLKVIT1	STOP_CLKTS
R				R/W	R	R/W	R/W

Address: 0xF1C3

Type: R/W

Reset: 0x0

Description: Stop clock control 2

[3] STOP_CLKSAMP1: 1: stops the demodulator 1 clock (unsigned)

[1] STOP_CLKVIT1: 1: stops the viterbi 1 clock (unsigned)

[0] STOP_CLKTS: 1: stops the transport stream clock (unsigned)

TSTTNR0 FSK analog cell test and configuration

7	6	5	4	3	2	1	0
SEL_FSK	RESERVED				FSK_PON	RESERVED	
R/W	R				R/W	R	

Address: 0xF1DF

Type: R/W

Reset: 0x4

Description: FSK analog cell test and configuration

[7] SEL_FSK: 1: selects FSK analog cell instead of DiSEqC 2 analog cell
0: selects DiSEqC 2 analog cell instead of FSK analog cell (unsigned)

[2] FSK_PON: 1: fsk analog cell power on
0: FSK analog cell power off (unsigned)

TSTTNR1 ADC 1 test and configuration

7	6	5	4	3	2	1	0
RESERVED						ADC1_PON	ADC1_INMODE
R						R/W	R/W

Address: 0xF1E0

Type: R/W

Reset: 0x27

Description: ADC 1 test and configuration

[1] ADC1_PON: 1: ADC 1 power on
0: ADC 1 power off (unsigned)

[0] ADC1_INMODE: selects amplitude range of ADC input signal
0: range 1Vpp
1: range 2Vpp (unsigned)

TSTTNR2 DiSEqC 1 test and configuration

7	6	5	4	3	2	1	0
RESERVED		DISEQC1_PON	RESERVED				
R		R/W	R				

Address: 0xF1E1

Type: R/W

Reset: 0x20

Description: DiSEqC 1 test and configuration

[5] DISEQC1_PON: 1: DiSEqC 1 power on
0: DiSEqC 1 power off (unsigned)

TSTTNR3 ADC 2 test and configuration

7	6	5	4	3	2	1	0
RESERVED						ADC2_PON	RESERVED
R						R/W	R

Address: 0xF1E2

Type: R/W

Reset: 0x27

Description: ADC 2 test and configuration

[1] ADC2_PON: 1: ADC 2 power on
0: ADC 2 power off (unsigned)

TSTTNR4 DiSEqC 2 test and configuration

7	6	5	4	3	2	1	0
RESERVED		DISEQC2_PON	RESERVED				
R		R/W	R				

Address: 0xF1E3

Type: R/W

Reset: 0x20

Description: DiSEqC 2 test and configuration

[5] DISEQC2_PON: 1: DiSEqC 2 power on
0: DiSEqC 2 power off (unsigned)

17.3 FSK register descriptions

FSKTFCx FSK transmitter gain and carrier frequency

	7	6	5	4	3	2	1	0
FSKTFC2	FSKT_KMOD						FSKT_CAR[17:16]	
	R/W						R/W	

	7	6	5	4	3	2	1	0
FSKTFC1	FSKT_CAR[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
FSKTFC0	FSKT_CAR[7:0]							
	R/W							

Address: 0xF170(x=2), 0xF171(x=1), 0xF172(x=0)

Type: R/W

Reset: 0x8C, 0x75, 0xC2

Description: FSK Transmitter gain and carrier frequency

FSKTFC2: [7:2] FSKT_KMOD: gain of the FSK modulator (unsigned)

FSKTFC2: [1:0]
FSKTFC1: [7:0] FSKT_CAR: FSK modulator carrier frequency (unsigned)
FSKTFC0: [7:0]

FSKTDELTAFx FSK transmitter frequency deviation

	7	6	5	4	3	2	1	0
FSKTDELTAF1	RESERVED				FSKT_DELTAF[11:8]			
	R				R/W			

	7	6	5	4	3	2	1	0
FSKTDELTAF0	FSKT_DELTAF[7:0]							
	R/W							

Address: 0xF173(x=1), 0xF174(x=0)

Type: R/W

Reset: 0x2, 0xC

Description: FSK transmitter frequency deviation

FSKTDELTAF1: [3:0]
FSKTDELTAF0: [7:0] FSKT_DELTAF: FSK modulator frequency deviation (unsigned)

FSKTCTRL FSK transmitter control

7	6	5	4	3	2	1	0
RESERVED	FSKT_EN_SGN	FSKT_MOD_SGN	FSKT_MOD_EN			FSKT_DACMODE	
R	R/W	R/W	R/W			R/W	

Address: 0xF175

Type: R/W

Reset: 0x4

Description: FSK transmitter control

[6] FSKT_EN_SGN: sign of FSKTX_EN
0: modulator is on when FSKTX_EN = 1, off when FSKTX_EN = 0
1: modulator is off when FSKTX_EN = 1, on when FSKTX_EN = 0 (unsigned)

[5] FSKT_MOD_SGN: sign of the modulator output frequency
0: FSKTX_OUT = Fc-df when FSKTX_IN = 0, FSKTX_OUT = Fc+df when FSKTX_IN = 1
1: FSKTX_OUT = Fc+df when FSKTX_IN = 0, FSKTX_OUT = Fc-df when FSKTX_IN = 1 (unsigned)

[4:2] FSKT_MOD_EN: modulator control bus
000: modulator off
001: modulator on
010: modulator enabled by FSKTX_EN input
011: FSK carrier (no deviation)
100: modulator output is Fc-df
101: modulator output is Fc+df (unsigned)

[1:0] FSKT_DACMODE: control of the FSK modulator output
00: second order sigma-delta converter
01: first order sigma-delta converter
10: no sigma-delta conversion (unsigned)

FSKRFCx FSK receiver carrier frequency

	7	6	5	4	3	2	1	0
FSKRFC2	RESERVED	FSKR_DETSGN	FSKR_OUTSGN	FSKR_KAGC			FSKR_CAR[17:16]	
	R	R/W	R/W	R/W			R/W	

	7	6	5	4	3	2	1	0
FSKRFC1	FSKR_CAR[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
FSKRFC0	FSKR_CAR[7:0]							
	R/W							

Address: 0xF176(x=2), 0xF177(x=1), 0xF178(x=0)

Type: R/W

Reset: 0x10, 0x75, 0xC2

Description: FSK receiver carrier frequency

FSKRFC2: [6] FSKR_DETSGN: sign of demod detect output (FSKRX_DETECT)
0: FSKRX_DETECT = 1 when a frequency deviation is detected, else 0
0: FSKRX_DETECT = 0 when a frequency deviation is detected, else 1 (unsigned)

FSKRFC2: [5] FSKR_OUTSGN: sign of demod output (FSKRX_OUT) (unsigned)

FSKRFC2: [4:2] FSKR_KAGC: FSK demodulator AGC time constant (unsigned)

FSKRFC2: [1:0]
FSKRFC1: [7:0]
FSKRFC0: [7:0]
FSKR_CAR: FSK demod carrier frequency
fskr_carrier = 2^20 * Fc / FMCLK, Fc = carrier freq., FMCLK = master clock freq. (unsigned)

FSKRK1 FSK receiver K1

7	6	5	4	3	2	1	0
FSKR_K1_EXP			FSKR_K1_MANT				
R/W			R/W				

Address: 0xF179

Type: R/W

Reset: 0x3A

Description: FSK receiver K1

[7:5] FSKR_K1_EXP: K1 coefficient exponent (unsigned)

[4:0] FSKR_K1_MANT: K1 coefficient mantissa K1 = fskr_k1_mant * 2^(8 + fskr_k1_exp), fskr_k1_exp = 0 to 5 (unsigned)

FSKRK2 FSK receiver K2

7	6	5	4	3	2	1	0
FSKR_K2_EXP			FSKR_K2_MANT				
R/W			R/W				

Address: 0xF17A

Type: R/W

Reset: 0x74

Description: FSK receiver K2

[7:5] FSKR_K2_EXP: K2 coefficient exponent (unsigned)

[4:0] FSKR_K2_MANT: K2 coefficient mantissa K2 = fskr_k2_mant * 2^fskr_k2_exp, fskr_k2_exp = 0 to 7 (unsigned)

FSKRAGCR FSK receiver AGC reference

7	6	5	4	3	2	1	0
FSKR_OUTCTL		FSKR_AGC_REF					
R/W		R/W					

Address: 0xF17B

Type: R/W

Reset: 0x28

Description: FSK receiver AGC reference

[7:6] FSKR_OUTCTL: demod output control bus
00: normal mode
01: FSKRX_OUT stuck at last value
10: FSKRX_OUT stuck at 0
11: FSKRX_OUT stuck at 1 (unsigned)

[5:0] FSKR_AGC_REF: demod AGC reference (unsigned)

FSKRAGC FSK receiver AGC status

7	6	5	4	3	2	1	0
FSKR_AGC_ACCU							
R							

Address: 0xF17C

Type: R

Reset: Undefined

Description: FSK receiver AGC status

[7:0] FSKR_AGC_ACCU: demod AGC value (unsigned)

FSKRALPHA FSK receiver alpha coefficient

7	6	5	4	3	2	1	0
RESERVED			FSKR_ALPHA_EXP			FSKR_ALPHA_M	
R			R/W			R/W	

Address: 0xF17D

Type: R/W

Reset: 0x17

Description: FSK receiver alpha coefficient

[4:2] FSKR_ALPHA_EXP: alpha coefficient exponent (unsigned)

[1:0] FSKR_ALPHA_M: alpha coefficient mantissa
alpha = 256 * (4 + fskr_alpha_m) * 2^fskr_alpha_exp (unsigned)

FSKRPLTHx FSK receiver beta coefficient and PLL threshold

	7	6	5	4	3	2	1	0
FSKRPLTH1	FSKR_BETA				FSKR_PLL_TRESH[11:8]			
	R/W				R/W			

	7	6	5	4	3	2	1	0
FSKRPLTH0	FSKR_PLL_TRESH[7:0]							
	R/W							

Address: 0xF17E(x=1), 0xF17F(x=0)

Type: R/W

Reset: 0x80, 0x0

Description: FSK receiver beta coefficient and PLL threshold

FSKRPLTH1: [7:4] FSKR_BETA: beta coefficient = 2^fskr_beta (unsigned)

FSKRPLTH1: [3:0]
FSKRPLTH0: [7:0] FSKR_PLL_TRESH: PLL threshold frequency (unsigned)

FSKRDFx FSK receiver frequency deviation

	7	6	5	4	3	2	1	0
FSKRDF1	FSKR_OUT	RESERVED		FSKR_DELTAF[12:8]				
	R	R		R				

	7	6	5	4	3	2	1	0
FSKRDF0	FSKR_DELTAF[7:0]							
	R							

Address: 0xF180(x=1), 0xF181(x=0)

Type: R

Reset: Undefined

Description: FSK receiver frequency deviation

FSKRDF1: [7] FSKR_OUT: value of FSKRX_OUT (unsigned)

FSKRDF1: [4:0]
FSKRDF0: [7:0] FSKR_DELTAF: demod dynamic frequency deviation value (unsigned)

FSKRSTEPP FSK receiver positive step

7	6	5	4	3	2	1	0
FSKR_STEP_PLUS							
R/W							

Address: 0xF182

Type: R/W

Reset: 0x30

Description: FSK receiver positive step

[7:0] FSKR_STEP_PLUS: signal detection positive step
step_plus = fskr_step_plus[4:0] * 2^fskr_step_plus[7:5] (unsigned)

FSKRSTEPM FSK receiver negative step

7	6	5	4	3	2	1	0
FSKR_STEP_MINUS							
R/W							

Address: 0xF183

Type: R/W

Reset: 0x70

Description: FSK receiver negative step

[7:0] FSKR_STEP_MINUS: signal detection negative step
step_minus = fskr_step_minus[4:0] * 2^fskr_step_minus[7:5] (unsigned)

FSKRDETx FSK receiver detection status

	7	6	5	4	3	2	1	0
FSKRDET1	FSKR_DETECT	RESERVED			FSKR_CARDET_ACCU[11:8]			
	R	R			R			

	7	6	5	4	3	2	1	0
FSKRDET0	FSKR_CARDET_ACCU[7:0]							
	R							

Address: 0xF184(x=1), 0xF185(x=0)

Type: R

Reset: 0x0

Description: FSK receiver detection status

FSKRDET1: [7] FSKR_DETECT: value of FSKRX_DETECT (unsigned)

FSKRDET1: [3:0]
FSKRDET0: [7:0] FSKR_CARDET_ACCU: demod average absolute frequency deviation (unsigned)

FSKRDTHx FSK receiver carrier detection and loss threshold

	7	6	5	4	3	2	1	0
FSKRDTH1	FSKR_CARLOSS_THRESH[11:8]				FSKR_CARDET_THRESH[11:8]			
	R/W				R/W			

	7	6	5	4	3	2	1	0
FSKRDTH0	FSKR_CARDET_THRESH[7:0]							
	R/W							

Address: 0xF186(x=1), 0xF187(x=0)

Type: R/W

Reset: 0x11, 0x89

Description: FSK receiver carrier detection and loss threshold

FSKRDTH1: [7:4] FSKR_CARLOSS_THRESH: signal lost frequency threshold (unsigned)

FSKRDTH1: [3:0]
FSKRDTH0: [7:0] FSKR_CARDET_THRESH: signal detected frequency threshold (unsigned)

FSKRLOSS FSK receiver carrier loss threshold

7	6	5	4	3	2	1	0
FSKR_CARLOSS_THRESH[7:0]							
R/W							

Address: 0xF188

Type: R/W

Reset: 0x6

Description: FSK receiver carrier loss threshold

[7:0] FSKR_CARLOSS_THRESH: signal lost frequency threshold (unsigned)

17.4 DIS register descriptions

DISTXCTL DiSEqC transmitter control

7	6	5 4	3	2 1 0
TIM_OFF	DISEQC_RESET	TIM_CMD	DIS_PRECHARGE	DISTX_MODE
R/W	R/W	R/W	R/W	R/W

Address: 0xF1A0

Type: R/W

Reset: 0x2A

Description: DiSEqC transmitter control

[7] TIM_OFF: 1: time offset enabled
0: time offset disabled (unsigned)

[6] DISEQC_RESET: 1: FIFO content is cleared (unsigned)

[5:4] TIM_CMD: timer control.
00: Tim = 15 ms at f22 = 22 kHz
01: Tim = 20 ms at f22 = 22 kHz
10: Tim = 25 ms at f22 = 22 kHz
11: Tim = 30 ms at f22 = 22 kHz (unsigned)

[3] DIS_PRECHARGE: 1:FIFO precharge disabled (unsigned)

[2:0] DISTX_MODE: DiSEqC transmission configuration
000: continuous (22 kHz) tone
001: reserved
010: DiSEqC 2/3
011: DiSEqC 3/3
100: DiSEqC 2/3 Envelop mode
101: DiSEqC 3/3 Envelop mode
110: reserved
111: reserved (unsigned)

DISRXCTL DiSEqC receiver control

7	6	5	4	3	2	1	0
RECEIVER_ON	IGNO_SHORT22K	ONECHIP_TRX	EXT_ENVELOP	PIN_SELECT		IRQ_RXEND	IRQ_4NBYTES
R/W	R/W	R/W	R/W	R/W		R/W	R/W

Address: 0xF1A1

Type: R/W

Reset: 0x0

Description: DiSEqC receiver control

[7] RECEIVER_ON: 1: receiver enabled (unsigned)

[6] IGNO_SHORT22K: 1: ignore short 22k mode (unsigned)

[5] ONECHIP_TRX: 1: DiSEqC Rx connected to Tx (loopback mode for test).
0: Rx is off when Tx is transmitting. (unsigned)

[4] EXT_ENVELOP: 0: receives the 22KHz tone from the pin selected using pin_select.
1: DiSEqC Rx expects a digital 1 or 0 representing the envelope of the tone of the selected GPIO via pin_select (DISEQCINn pin is disabled). (unsigned)

[3:2] PIN_SELECT: Select DiSEqC n input pin and polarity.
00: Analog, DISEQCINn pin;
01: n=1 GPIO1. n=2 GPIO4.
10: Inverted analog, DISEQCINn pin
11: Inverted GPIO1/4 (unsigned)

[1] IRQ_RXEND: 1: DiSEqC controller sends interrupt at end of receive block
0: no IRQ (unsigned)

[0] IRQ_4NBYTES: 1: DiSEqC controller sends interrupt when RX FIFO contains 4 or more bytes.
0: no IRQ (unsigned)

DISRX_ST0 DiSEqC receiver status0

7	6	5	4	3	2	1	0
RX_END	RX_ACTIVE	SHORT_22KHZ	CONT_TONE	FIFO_4BREADY	FIFO_EMPTY	RESERVED	ABORT_DISRX
R	R	R	R	R	R	R	R

Address: 0xF1A4

Type: R

Reset: Undefined

Description: DiSEqC receiver status0

[7] RX_END: 1: reception is ended (unsigned)

[6] RX_ACTIVE: 1: receiver is active (unsigned)

[5] SHORT_22KHZ: 1: a short 22 kHz sequence has been received since last bit erase (unsigned)

[4] CONT_TONE: 1: more than 33 pulse-widths of tone burst have been detected (continuous tone present) (unsigned)

[3] FIFO_4BREADY: 1: there are 4 or more bytes in the FIFO ready for reading (unsigned)

[2] FIFO_EMPTY: 1: the FIFO is empty (unsigned)

[0] ABORT_DISRX: 1: DiSEqC receive sequence has been aborted (unsigned)

DISRX_ST1 DiSEqC receiver status1

7	6	5	4	3	2	1	0
RX_FAIL	FIFO_PARITYFAIL	RX_NONBYTE	FIFO_OVERFLOW	FIFO_BYTENBR			
R	R	R	R	R			

Address: 0xF1A5

Type: R

Reset: Undefined

Description: DiSEqC receiver status1

[7] RX_FAIL: 1: reception problem (short 22 kHz or continuous tone sequence) (unsigned)

[6] FIFO_PARITYFAIL: 1: transmission error. The parity checks fail (unsigned)

[5] RX_NONBYTE: 1: transmission error. The number of received bits does not correspond to a full data byte (8 bits + parity). (unsigned)

[4] FIFO_OVERFLOW: 1: DiSEqC receiver FIFO overflow. More than 8 bytes are waiting (unsigned)

[3:0] FIFO_BYTENBR: number of bytes contained in the DiSEqC receiver FIFO (unsigned)

DISRXDATA — DiSEqC receiver FIFO

7	6	5	4	3	2	1	0
DISRX_DATA							
R/W							

Address: 0xF1A6

Type: R/W

Reset: 0x0

Description: DiSEqC receiver FIFO

[7:0] DISRX_DATA: DiSEqC receiver FIFO, 8 bytes deep. (unsigned)

DISTXDATA — DiSEqC transmitter FIFO

7	6	5	4	3	2	1	0
DISEQC_FIFO							
R/W							

Address: 0xF1A7

Type: R/W

Reset: 0x0

Description: DiSEqC transmitter FIFO

[7:0] DISEQC_FIFO: DiSEqC transmitter FIFO. 8 bytes deep. (unsigned)

DISTXSTATUS — DiSEqC transmitter status

7	6	5	4	3	2	1	0
TX_FAIL	FIFO_FULL	TX_IDLE	GAP_BURST	TXFIFO_BYTES			
R	R	R	R	R			

Address: 0xF1A8

Type: R

Reset: Undefined

Description: DiSEqC transmitter status

[7] TX_FAIL: 1: transmission failed (unsigned)

[6] FIFO_FULL: 1: Tx FIFO is full (unsigned)

[5] TX_IDLE: 1: Tx FIFO is empty (unsigned)

[4] GAP_BURST: 1: Tx gap (as programmed in DiSEqC.tim_cmd) has not yet expired (unsigned)

[3:0] TXFIFO_BYTES: number of bytes in Tx FIFO (waiting to be transmitted) (unsigned)

F22TX DiSEqC 22 kHz transmitter frequency tone control

7	6	5	4	3	2	1	0
F22_REG							
R/W							

Address: 0xF1A9

Type: R/W

Reset: 0x99

Description: DiSEqC 22 kHz transmitter frequency tone control

[7:0] F22_REG: tone modulation frequency control.
FDiSEqC_Tx = M_CLK / (32 x DISF22dec)
For 22 kHz operation and M_CLK = 135 MHz, f22_reg = 192 or 0xC0. (unsigned)

F22RX DiSEqC 22 kHz receiver frequency tone control

7	6	5	4	3	2	1	0
F22RX_REG							
R/W							

Address: 0xF1AA

Type: R/W

Reset: 0x7

Description: DiSEqC 22 kHz receiver frequency tone control

[7:0] F22RX_REG: tone modulation frequency control.
FDiSEqC_Rx = M_CLK / (32 x DISF22dec)
For 22 kHz operation and M_CLK = 135 MHz, f22rx_reg = 192 or 0xC0. (unsigned)

ACRPRESC Auxiliary clock control

7	6	5	4	3	2	1	0
RESERVED						ACR_PRESC	
R						R/W	

Address: 0xF1AC

Type: R/W

Reset: 0x1

Description: Auxiliary clock control

[2:0] ACR_PRESC: Auxiliary clock prescaler
000: reserved
001: prescaler divided by 2
010: prescaler divided by 16
011: prescaler divided by 128
100: prescaler divided by 1024
101: prescaler divided by 8192
110: prescaler divided by 65536
111: prescaler divided by 524288 (unsigned)

ACRDIV Auxiliary clock division control

7	6	5	4	3	2	1	0
ACR_DIV							
R/W							

Address: 0xF1AD

Type: R/W

Reset: 0x14

Description: Auxiliary clock division control

[7:0] ACR_DIV: Auxliary clock division
Faux = MCLK/(acr_div x acr_presc), MCLK = 270 MHz
The obtained signal is square wave,
with 0 = divided by 256 (unsigned)

17.5 DMD register descriptions

IQCONST Constellation editor configuration

7	6	5	4	3	2	1	0
RESERVED	CONSTEL_SELECT		IQSYMB_SEL				
R	R/W		R/W				

Address: 0xF400

Type: R/W

Reset: 0x0

Description: Constellation editor configuration

[6:5] CONSTEL_SELECT: observation mode for ISYMB & QSYMB.
00: normal mode, observe the selection iqsymb_sel[4:0]
01: inverse mode, observe the selection TCTL1/tst_iqsymbsel[4:0]
10: superpose mode: observe iqsymb_sel[4:0] and TCTL1/tst_iqsymbsel[4:0]
11: staggered superpose mode: observe the selection iqsymb_sel[4:0] and the selection TCTL1/tst_iqsymbsel[4:0] divided by 2 (this will help distinguish the 2 figures). (unsigned)

[4:0] IQSYMB_SEL: selection of measuring point
Measuring Points in data flow:
0x00: demodulator IQ output
0x01: equaliser output
0x02: derotator 2 output (signal divided by 2)
0x03: symbols+inter symbols output (superimposed)
0x04: symbols output
0x05: inter symbols output
0x06: derotator 1 output (samples, divided by 2)
0x07: IQ mismatches output (amplitude, angle, DC)
0x08: demodulation input

NOSCFG Configuration of noise indicators

7	6	5	4	3	2	1	0
RESERVED		DUMMYPL_NOSDATA	NOSPLH_BETA		NOSDATA_BETA		
R		R/W	R/W		R/W		

Address: 0xF401

Type: R/W

Reset: 0x14

Description: Forcing (internally) nosplh_beta = 11 and nosdata_beta = 111 while the demodulator is unlocked will set the registers to globally correct values (correct order of magnitude) as quickly as possible.

[5] DUMMYPL_NOSDATA: Method of accounting for Dummy PLFrames in DVBS2:
0: consider them when calculating xNOSPLHx
1: consider them when calculating xNOSDATAx (unsigned)

[4:3] NOSPLH_BETA: error collection speed for structure symbols (DVBS2 only):
11: fastest, 2^0
10: 2^-8
01: 2^-10, standard value
00: slowest (unsigned)

[2:0] NOSDATA_BETA: error collection speed for usable load (DVBS2 or DVBS1/Legacy DTV):
111: fastest, 2^0
110: 2^-8
101: 2^-10
100: 2^-12, standard value
011: 2^-14
010: 2^-16
001: 2^-18
000: slowest, 2^-20 (unsigned)

ISYMB — Constellation editor I track

7	6	5	4	3	2	1	0
I_SYMBOL							
R							

Address: 0xF402

Type: R

Reset: Undefined

Description: Constellation editor I track

[7:0] I_SYMBOL: (signed)

QSYMB — Constellation editor Q track

7	6	5	4	3	2	1	0
Q_SYMBOL							
R							

Address: 0xF403

Type: R

Reset: Undefined

Description: Constellation editor Q track

[7:0] Q_SYMBOL: time consistent with ISYMB.i_symbol. (signed)

AGC1CFG IQ mismatch control

7	6	5	4	3	2	1	0
DC_FROZEN	DC_CORRECT	AMM_FROZEN	AMM_CORRECT	QUAD_FROZEN	QUAD_CORRECT	RESERVED	
R/W	R/W	R/W	R/W	R/W	R/W	R	

Address: 0xF404

Type: R/W

Reset: 0x54

Description: IQ mismatch control

[7] DC_FROZEN: compensation freeze (unsigned)

[6] DC_CORRECT: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

[5] AMM_FROZEN: compensation freeze (unsigned)

[4] AMM_CORRECT: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

[3] QUAD_FROZEN: compensation freeze (unsigned)

[2] QUAD_CORRECT: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

AGC1CN AGC1 control

7	6	5	4	3	2	1	0
AGC1_LOCKED	RESERVED		AGC1_MINPOWER	AGCOUT_FAST	AGCIQ_BETA		
R	R		R/W	R/W	R/W		

Address: 0xF406

Type: R/W

Reset: 0x19

Description: AGC1 control

[7] AGC1_LOCKED: AGC1 stability indicator
1: AGC1 has stabilized. (read put to 0 on a read,unsigned)

[4] AGC1_MINPOWER: limit selection for POWERI+POWERQ (see above). (unsigned)

[3] AGCOUT_FAST: PWM signal speed output from AGC1:
0: 1/64 Mclk
1: 1/4 Mclk
Operation latitude is required to compensate for a loss on the RC network connected to the pin of AGC1. (unsigned)

[2:0] AGCIQ_BETA: AGC1 loop speed:
As soon as the demodulator is in the process of locking (demod_tracked=1), subtract 1.5 from agciq_beta internally (division of this speed by 8).
000: stop
001: slowest
..
111: fastest (unsigned)

AGC1REF AGC1 reference

7	6	5	4	3	2	1	0
AGCIQ_REF							
R/W							

Address: 0xF407

Type: R/W

Reset: 0x58

Description: AGC1 reference

[7:0] AGCIQ_REF: AGC1 reference module.
Unit = ADCI or Q / sqrt(2)
Consign AGC1 = I^2 + Q^2 - 2 * (agciq_ref^2) (unsigned)

IDCCOMP DC compensation on I

7	6	5	4	3	2	1	0
IAVERAGE_ADJ							
R							

Address: 0xF408

Type: R

Reset: Undefined

Description: DC compensation on I

[7:0] IAVERAGE_ADJ: Unit = in 1/2 of ADCI
0x80: error of +0x40 on ADCI
0x00: no correction necessary
0x7F: error of -0x3F on ADCI (signed)

QDCCOMP DC compensation on Q

7	6	5	4	3	2	1	0
QAVERAGE_ADJ							
R							

Address: 0xF409

Type: R

Reset: Undefined

Description: DC compensation on Q

[7:0] QAVERAGE_ADJ: Unit = in 1/2 of ADCQ
0x80: error of +0x40 on ADCQ
0x00: no correction necessary
0x7F: error of -0x3F on ADCQ (signed)

POWERI Power measured on I

7	6	5	4	3	2	1	0
POWER_I							
R							

Address: 0xF40A

Type: R

Reset: Undefined

Description: Power measured on I

[7:0] POWER_I: Unit: in 1/4 of ADCI. (unsigned)

POWERQ — Power measured on Q

7	6	5	4	3	2	1	0
POWER_Q							
R							

Address: 0xF40B

Type: R

Reset: Undefined

Description: Power measured on Q

[7:0] POWER_Q: Unit: in 1/4 of ADCQ. (unsigned)

AGC1AMM — Amplitude compensation of Q with respect to I

7	6	5	4	3	2	1	0
AMM_VALUE							
R/W							

Address: 0xF40C

Type: R/W

Reset: Undefined

Description: Amplitude compensation of Q with respect to I

[7:0] AMM_VALUE: < 0x80: Q attenuated
= 0x80: no correction necessary
> 0x80: Q amplified
Compensation = amm_value / 0x80 (unsigned)

AGC1QUAD — Quadrature compensation of Q with respect to I

7	6	5	4	3	2	1	0
QUAD_VALUE							
R/W							

Address: 0xF40D

Type: R/W

Reset: Undefined

Description: Quadrature compensation of Q with respect to I

[7:0] QUAD_VALUE: < 0x00: a little of I taken from Q
0x00: no correction necessary
> 0x00: a little of I added to Q (signed)

AGCIQIN1 AGC1 accumulator

7	6	5	4	3	2	1	0
AGCIQ_VALUE[15:8]							
R/W							

Address: 0xF40E

Type: R/W

Reset: Undefined

Description: AGC1 accumulator

[7:0] AGCIQ_VALUE: 0x0000: maximum amplification (signal too weak)
0x8000: middle value
0xFFFF: minimum amplification (signal too strong) (unsigned)

AGCIQIN0 AGC1 accumulator

7	6	5	4	3	2	1	0
AGCIQ_VALUE[7:0]							
R/W							

Address: 0xF40F

Type: R/W

Reset: Undefined

Description: AGC1 accumulator

[7:0] AGCIQ_VALUE: 0x0000: maximum amplification (signal too weak)
0x8000: middle value
0xFFFF: minimum amplification (signal too strong) (unsigned)

DEMOD General register for demodulator main functions

7	6	5 4	3	2	1 0
MANUALS2_ROLLOFF	RESERVED	SPECINV_CONTROL	FORCE_ENASAMP	MANUALSX_ROLLOFF	ROLLOFF_CONTROL
R/W	R	R/W	R/W	R/W	R/W

Address: 0xF410

Type: R/W

Reset: 0x8

Description: General register for demodulator main functions

[7] MANUALS2_ROLLOFF: Roll-Off filter control mode (DVBS2 only):
0: automatic mode. Start with value in rolloff_control (decribed below) then set value read in MATYPE/RO[1:0].
1: manual mode, use value set in rolloff_control (full stop). (unsigned)

[5:4] SPECINV_CONTROL: local spectral inversion control
00: automatic
01: automatic, with reset to 0 when a new search is launched
10: manual set to 0
11: manual set to 1 (unsigned)

[3] FORCE_ENASAMP: mode for treatment at very low baud rates (oversampling > ~200)
0: decimation (raw, without filtering) of the surplus samples, which avoids saturation of the Nyquist filters at these very low baud rates. Correct calibration of the analog filters is important to avoid folding.
1: prohibit decimation. It will not be possible to capture correctly at very lowbaud rates (oversampling > ~200). (unsigned)

[2] MANUALSX_ROLLOFF: Roll-Off control of Nyquist filters in DVBS1/Legacy DTV (for DVBS2, see manuals2_rolloff above):
0:automatic mode,
DVBS1: initialisation with rolloff_control (above). Then after lock force a value of 35%.
Legacy DTV:initialisation with rolloff_control (above). Then after lock force a value of 20%.
1: manual mode, use rolloff_control whatever the situation. (unsigned)

[1:0] ROLLOFF_CONTROL: roll off at init or in manual mode
00:35% 01:25% 10:20% (11:15%)
(The same table as the DVBS2 specification)
See TMGOBS/rolloff_status to observe the chosen roll-off. (unsigned)

DMDMODCOD Override register for MODCOD&TYPE

7	6	5	4	3	2	1	0
MANUAL_MODCOD	DEMOD_MODCOD					DEMOD_TYPE	
R/W	R/W					R/W	

Address: 0xF411

Type: R/W

Reset: Undefined

Description: Override register for MODCOD&TYPE

[7] MANUAL_MODCOD: manual override of MODCOD & TYPE (DVBS2 only)
1: MODCOD & TYPE are set by the fields demod_modcod and demod_type as below.
0: they are inactive. (unsigned)

[6:2] DEMOD_MODCOD: DVBS2:
0: DummyPL 8: QPSK 4/5 16: 8PSK 8/9 24: 32APSK 3/4
1: QPSK 1/4 9: QPSK 5/6 17: 8PSK 9/10 25: 32APSK 4/5
2: QPSK 1/3 10: QPSK 8/9 18: 16APSK 2/3 26: 32APSK 5/6
3: QPSK 2/5 11: QPSK 9/10 19: 16APSK 3/4 27: 32APSK 8/9
4: QPSK 1/2 12: 8PSK 3/5 20: 16APSK 4/5 28: 32APSK 9/10
5: QPSK 3/5 13: 8PSK 2/3 21: 16APSK 5/6 29: --
6: QPSK 2/3 14: 8PSK 3/4 22: 16APSK 8/9 30: --
7: QPSK 3/4 15: 8PSK 5/6 23: 16APSK 9/10 31: RQ
DVBS1/Legacy DTV convention:
4: QPSK 1/2
5: QPSK 3/5
6: QPSK 2/3
7: QPSK 3/4
9: QPSK 5/6
10: QPSK 6/7 (DVBS2 QPSK 8/9)
11: QPSK 7/8 (DVBS2 QPSK 9/10)
The others have no meaning (unsigned)

[1:0] DEMOD_TYPE: DVBS2 only
bit 1: Short frame mode
bit 0: Pilots present (unsigned)

DSTATUS Demodulator status 1

7	6 5	4	3	2 1	0
CAR_LOCK	TMGLOCK_QUALITY	RESERVED	LOCK_DEFINITIF	RESERVED	OVADC_DETECT
R	R	R	R	R	R

Address: 0xF412

Type: R

Reset: Undefined

Description: General status

[7] CAR_LOCK: carrier lock (unsigned)

[6:5] TMGLOCK_QUALITY: timing lock quality
00: timing not locked
01: timing in process of being locked
1x: timing locked (unsigned)

[3] LOCK_DEFINITIF: demodulator locked
The official locking indicator. (unsigned)

[0] OVADC_DETECT: Persistant ADC overflow detected; on more than 1/16th of all samples from the input ADCs (i.e. >6%) . (unsigned)

DSTATUS2 Demodulator status 2

7	6	5	4	3	2	1	0
DEMOD_DELOCK	RESERVED			AGC1_NOSIGNALACK	AGC2_OVERFLOW	CFR_OVERFLOW	GAMMA_OVERUNDER
R/W	R			R	R	R	R

Address: 0xF413

Type: R

Reset: Undefined

Description: Failure observation

[7] DEMOD_DELOCK: Detection of a zero passage in DSTATUS/LOCK_DEFINITIF. Useful for debug. Reset to zero by an I2C write. (read put to 0 on a write,unsigned)

[3] AGC1_NOSIGNALACK: diagnostic “Tuner no signal“. No signal at the ADC entries. (read put to 0 on a read,unsigned)

[2] AGC2_OVERFLOW: AGC2 saturation at maximum amplification (no signal after Nyquist filtering). (read put to 0 on a read,unsigned)

[1] CFR_OVERFLOW: CFR has reached the limit of CFRUP, CFRLOW or +-tuner max range. (read put to 0 on a read,unsigned)

[0] GAMMA_OVERUNDER: SFR has reached the limit of SFRmin (symbol rate min range) or SFRmax (tuner max range). (read put to 0 on a read,unsigned)

DMDCFGMD Demodulator configuration 1

7	6	5	4	3	2	1	0
DVBS2_ENABLE	DVBS1_ENABLE	RESERVED	SCAN_ENABLE	CFR_AUTOSCAN	RESERVED	TUN_RNG	
R	R	R	R	R	R	R	

Address: 0xF414

Type: R

Reset: 0xC9

Description: Main modes. Value recommended: 0xF8+tuner_range[1:0]
Certain bits of this register are independently set to 1 or 0 (internally) depending upon the AEP selected and upon the step currently in progress in the state machine.

[7] DVBS2_ENABLE: 1: authorize a DVBS2 search. (unsigned)

[6] DVBS1_ENABLE: 1: authorize a DVBS1/Legacy DTV search. (unsigned)

[4] SCAN_ENABLE: 1: authorize symbol rate scanning. (unsigned)

[3] CFR_AUTOSCAN: 1: authorize CFRINIT as a variable. (unsigned)

[1:0] TUN_RNG: tuner bandwidth range:
tuner_range: 0 1 2 3
SFRxx max: 1/2 1/2 1/4 1/8 MCLK
CFRxx max: +-1/2 +-1/4 +-1/8 +-1/16 MCLK
@135 MHz 67.5 67.5 33.7 16.9 MSymb/s
+-67.5 +-33.7 +-16.9 +-8.4 MHz
Usual range: 1 (unsigned)

DMDCFG2 Demodulator configuration 2

7	6	5	4	3	2	1	0
RESERVED	S1S2_SEQUENTIAL	RESERVED	INFINITE_RELOCK	RESERVED			
R	R/W	R	R/W	R			

Address: 0xF415

Type: R/W

Reset: 0xFB

Description: State machine internal behavior. Value recommended in general: 0xFB
Certain bits of this register are independently set to 1 or 0 (internally) in “demod relock“ and “tuner centering“ modes.

[6] S1S2_SEQUENTIAL: 1: sequential search DVBS2 and DVBS1/Legacy DTV (if DMDCFGMD.dvbs2_enable AND DMDMDCFG.dvbs1_enable are at 1).
0: parallel search.
For broadcast QPSK and 8PSK,parallel search (Pn_S1S2_SEQUENTIAL = 0) is recommended
For 16APSK and 32APSK (advanced version only) sequential search (Pn_S1S2_SEQUENTIAL = 1) is recommended (unsigned)

[4] INFINITE_RELOCK: timeout mode during relock:
1: try to relock infinitely.
0: time out after 64 trials. (unsigned)

DMDISTATE AEP launch register

7	6	5	4	3	2	1	0
RESERVED			I2C_DEMOD_MODE				
R			R/W				

Address: 0xF416

Type: R/W

Reset: 0x5C

Description: AEP launch register

[4:0] I2C_DEMOD_MODE: See Chapter 5.13 Algorithmic Entry Points. (unsigned)

DMDT0M — Coarse carrier & symbol time constant

7	6	5	4	3	2	1	0
DMDT0_MIN							
R/W							

Address: 0xF417

Type: R/W

Reset: 0x10

Description: Coarse carrier & symbol time constant

[7:0] DMDT0_MIN: minimum wait time (in samples) in coarse carrier search. If the value zero is assigned, the AEPs using the coarse search algorithm will exit at the end of the coarse search state (and will not proceed with the fine search). (unsigned)

DMDSTATE — Step currently in progress in the demodulator general state machine

7	6	5	4	3	2	1	0
RESERVED	HEADER_MODE		RESERVED				
R	R		R				

Address: 0xF41B

Type: R

Reset: Undefined

Description: Attention: If bit 7 is set to ‘0‘ then any I2C write to this register will cause the AEP to be re-launched.

[6:5] HEADER_MODE: locking status
- 00: searching
- 01: 1st DVBS2 PLHeader detected, searching for residual offset symbol.
- 10: DVBS2 mode
- 11: DVBS1/Legacy DTV mode (unsigned)

DMDFLYW Demodulator status

7	6	5	4	3	2	1	0
I2C_IRQVAL				FLYWHEEL_CPT			
R				R			

Address: 0xF41C

Type: R

Reset: 0x0

Description: Demodulator status

[7:4] I2C_IRQVAL: IRQ (Interrupt ReQuest) sent by the demodulator. Also serves as a final diagnostic for the demodulator. This info is supplied at the same time as the impulse demod_irq to the circuit interrupt manager. The host processor must therefore read this field to get details on the interruption received:
0x0: --
0x1: AGC1/AGC2/CFR1/SFR overflow -> no signal
0x2: limits of CFRUP<->CFRLOW and/or SFRUP<->SFRLOW exceeded
If the demodulator is locked, a simple indication
Otherwise, a timeout (followed by demod_fail)
0x3: timeout steps 3,6 -> no signal
0x4: fail after 8 (or 64 in force relock mode) looped
0x5: timeout step 9 -> undecodable
0x6: lock DVBS2
0x7: unlock DVBS2
0x8: lock DVBS1/Legacy DTV
0x9: unlock DVBS1/Legacy DTV
0xA: --
0xB: --
0xC: FIFO results full
Final demand to empty
0xD: BandWidth FullScan done
Scan finished (end of AEP 0x11 or 0x1B)
0xE: FIFO results have passed the mark of 8 results
Urgent demand to empty results register
0xF: --
A write to this register erases the value in i2c_irqval (unsigned)

[3:0] FLYWHEEL_CPT: PLHeader correct counter detected. When this counter becomes 0xF the demodulator is defined as locked (DVBS2 only). A little before (from 3), the internal signal demod_tracked becomes 1 (visible on the SD Data, see chapter “SDD - Serial Data Description“). (unsigned)

DSTATUS3 Demodulator status 3

7	6	5	4	3	2	1	0
RESERVED	DEMOD_CFGMODE		RESERVED				
R	R		R				

Address: 0xF41D

Type: R

Reset: Undefined

Description: Status of certain operation steps

[6:5] DEMOD_CFGMODE: Demodulator functional mode:
00: demodulation
01: Scanning pass band (no tuner control)
10: Scanning tuner range
11: Calibration (of tuner) (unsigned)

DMDCFG3 Demodulator configuration 3

7	6	5	4	3	2	1	0
RESERVED				NOSTOP_FIFOFULL	RESERVED		
R				R/W	R		

Address: 0xF41E

Type: R/W

Reset: 0x8

Description: Demodulator configuration 3

[3] NOSTOP_FIFOFULL: behavior when FIFO results full
0: wait for emptying before continuing. Can lead to hang situations (that can be baffling) if no emptying procedure is in action for that FIFO.
1: do not hang the system (the data may be lost). (unsigned)

DMDCFG4 Demodulator configuration 4

7	6	5	4	3	2	1	0
RESERVED				TUNER_NRELAUNCH	RESERVED		
R				R/W	R		

Address: 0xF41F

Type: R/W

Reset: 0x0

Description: Demodulator configuration 4

[3] TUNER_NRELAUNCH: A method of reprogramming the tuner in the case of failure due to tuner I2C error or tuner lock criteria.
1: soft increment tuner. Hypothesis: the problem may have been related to a 'frequency hole' thus it is better to move along a bit.
0: AEP Stop. Sstop the state machine for manual intervention. (unsigned)

CORRELMANT Differential correlator limit mantissa

7	6	5	4	3	2	1	0
CORREL_MANT							
R/W							

Address: 0xF420

Type: R/W

Reset: 0x70

Description: Differential correlator limit mantissa

[7:0] CORREL_MANT: see CORRELEXP.correl_exp (unsigned)

CORRELABS Absolute correlator limit mantissa

7	6	5	4	3	2	1	0
CORREL_ABS							
R/W							

Address: 0xF421

Type: R/W

Reset: 0x9E

Description: Absolute correlator limit mantissa

[7:0] CORREL_ABS: see CORRELEXP.correl_absexp (unsigned)

CORRELEXP Relative and absolute correlation limit exponents

7	6	5	4	3	2	1	0
CORREL_ABSEXP				CORREL_EXP			
R/W				R/W			

Address: 0xF422

Type: R/W

Reset: 0xAA

Description: Relative and absolute correlation limit exponents.

[7:4] CORREL_ABSEXP: calculation mode of absolute limit (“Fast Hadamar“)
Values referenced on simple AGC2REF.agc2_ref:
0000: limit = correl_abs*agc2_ref/32
0001: limit = correl_abs*agc2_ref/16
0010: limit = correl_abs*agc2_ref/8
0011: limit = correl_abs*agc2_ref/4
Manual values:
0100: limit = correl_abs*8
0101: limit = correl_abs*16
0110: limit = correl_abs*32
0111: limit = correl_abs*64
Values referenced on adaptive agc2_ref (3/4=0.75):
1000: init limit = correl_abs*agc2_ref/32
1001: init limit = correl_abs*agc2_ref/16
1010: init limit = correl_abs*agc2_ref/8 <-Recommended
1011: init limit = correl_abs*agc2_ref/4
Special case reference values:
0100: --
0101: limit = 640
0110: --
0111: limit = 0xFFFF
correl_abs: CORRELABS register field. (unsigned)

[3:0] CORREL_EXP: calculation mode of relative limit (“Real Time Correlator“)
Values referenced on simple AGC2REF.agc2_ref:
0000: limit = (correl_mant*agc2_ref)^2/4
0001: limit = (correl_mant*agc2_ref)^2/2
0010: limit = (correl_mant*agc2_ref)^2
0011: limit = (correl_mant*agc2_ref)^2*2
Manual values:
0100: limit = correl_mant*32
0101: limit = correl_mant*64
0110: limit = correl_mant*128
0111: limit = correl_mant*256
Values referenced on adaptive agc2_ref (3/4):
1000: init limit = (correl_mant*agc2_ref)^2/4
1001: init limit = (correl_mant*agc2_ref)^2/2
1010: init limit = (correl_mant*agc2_ref)^2 <-Recommended
1011: init limit = (correl_mant*agc2_ref)^2*2
Values referenced on adaptive agc2_ref (1/2):
1100: init limit = (correl_mant*agc2_ref)^2/4
1101: init limit = (correl_mant*agc2_ref)^2/2
1110: init limit = (correl_mant*agc2_ref)^2
1111: init limit = (correl_mant*agc2_ref)^2*2
agc2_ref: see AGC2REF register
correl_mant: CORRELMANT register field. (unsigned)

PLHMODCOD — Current MODCOD&TYPE, only DVBS2

7	6	5	4	3	2	1	0
SPECINV_DEMOD	PLH_MODCOD					PLH_TYPE	
R	R					R	

Address: 0xF424

Type: R

Reset: Undefined

Description: Current MODCOD&TYPE, only DVBS2

[7] SPECINV_DEMOD: local spectral inversion detected by the demodulator in DVBS2 mode. (unsigned)

[6:2] PLH_MODCOD: Current MODCOD (value not stable). Use register DMDMODCOD. (unsigned)

[1:0] PLH_TYPE: current TYPE (value not stable). Use register DMDMODCOD. (unsigned)

DMDREG — Various special cases

7	6	5	4	3	2	1	0
RESERVED							DECIM_PLFRAMES
R							R/W

Address: 0xF425

Type: R/W

Reset: 0x0

Description: Various special cases

[0] DECIM_PLFRAMES: 1: eliminate 1 frame in 2 if more than 64 consecutive errored packets or fames are detected false.
This can prevent the IC from overheating in rain fade conditions. (unsigned)

AGC2O AGC2 configuration

7	6	5	4	3	2	1	0
RESERVED					AGC2_COEF		
R					R/W		

Address: 0xF42C

Type: R/W

Reset: 0x5B

Description: AGC2 configuration

[2:0] AGC2_COEF: 000: open loop, AGC2I1/0 manual
001: slowest
...
111: fastest (unsigned)

AGC2REF Demodulator general reference

7	6	5	4	3	2	1	0
AGC2_REF							
R/W							

Address: 0xF42D

Type: R/W

Reset: 0x38

Description: Demodulator general reference

[7:0] AGC2_REF: reference module for the whole demodulator (applies much further than AGC2). Same units as the IQ coming from the ADC. (unsigned)

AGC1ADJ AGC1 set point

7	6	5	4	3	2	1	0
RESERVED	AGC1_ADJUSTED						
R	R/W						

Address: 0xF42E

Type: R/W

Reset: 0x58

Description: AGC1 set point

[6:0] AGC1_ADJUSTED: Set point value applied to AGC1 loop. Normally constant. However, if this value moves then the machine is receiving 16 or 32 APSK in constant envelope mode. (unsigned)

AGC2I1 AGC2 accumulator

7	6	5	4	3	2	1	0
AGC2_INTEGRATOR[15:8]							
R/W							

Address: 0xF436

Type: R/W

Reset: Undefined

Description: AGC2 accumulator

[7:0] AGC2_INTEGRATOR: 0x0000: minimum amplification
0xFFFF: maximum amplification (unsigned)

AGC2I0 AGC2 accumulator

7	6	5	4	3	2	1	0
AGC2_INTEGRATOR[7:0]							
R/W							

Address: 0xF437

Type: R/W

Reset: Undefined

Description: AGC2 accumulator

[7:0] AGC2_INTEGRATOR: 0x0000: minimum amplification
0xFFFF: maximum amplification (unsigned)

CARCFG Carrier 1 configuration

7	6	5	4	3	2	1	0
RESERVED					ROTAON	PH_DET_ALGO	
R					R/W	R/W	

Address: 0xF438

Type: R/W

Reset: 0xE4

Description: Carrier 1 configuration

[2] ROTAON: 1: carrier 1 derotator in action
0: carrier 1 loop open (unsigned)

[1:0] PH_DET_ALGO: algorithm used to calculate the phase error on the QPSK symbols:
00: costas
01: citroen 1
10: citroen 2
11: -- (unsigned)

ACLC Alpha DVBS1/legacy DTV

7	6	5	4	3	2	1	0
RESERVED		CAR_ALPHA_MANT		CAR_ALPHA_EXP			
R		R/W		R/W			

Address: 0xF439

Type: R/W

Reset: 0x1A

Description: This register is used primarily for DVBS1/legacy DTV.

[5:4] CAR_ALPHA_MANT: (unsigned)

[3:0] CAR_ALPHA_EXP: 0000: feedback loop is frozen in its last accumulated state
0001: slowest
1111: fastest (unsigned)

BCLC Beta DVBS1/legacy DTV

7	6	5	4	3	2	1	0
RESERVED		CAR_BETA_MANT		CAR_BETA_EXP			
R		R/W		R/W			

Address: 0xF43A

Type: R/W

Reset: 0x9

Description: This register is used primarily for DVBS1/legacy DTV.

[5:4] CAR_BETA_MANT: (unsigned)

[3:0] CAR_BETA_EXP: 0000: feedback loop is frozen in its last accumulated state
0001: slowest
1111: fastest (unsigned)

CARFREQ — Loop carrier 1 coefficients

7	6	5	4	3	2	1	0
KC_COARSE_EXP				BETA_FREQ			
R/W				R/W			

Address: 0xF43D

Type: R/W

Reset: 0x68

Description: Loop carrier 1 coefficients

[7:4] KC_COARSE_EXP: exponent of coarse carrier loop coefficient: multcoef_kccoarse = (4 + kc_coarse_mant) * 2^(1 + 2 * kc_coarse_exp)
0000: stop coarse carrier.
0001: slowest
1111: fastest (unsigned)

[3:0] BETA_FREQ: Frequency Detector, DVBS1 only
0000: stop coarse carrier corrections
0001: minimum coefficient
1111: maximum coefficient (unsigned)

CARHDR — PLHeader delta F coefficient in DVBS2

7	6	5	4	3	2	1	0
K_FREQ_HDR							
R/W							

Address: 0xF43E

Type: R/W

Reset: 0x20

Description: PLHeader delta F coefficient in DVBS2

[7:0] K_FREQ_HDR: carrier offset coefficient detected by the PLHeader in stable conditions
0x00: no more correction
0x40: coefficient 1.00 at start up and 1/32 in steady state conditions (unsigned)

LDT — Positive edge of carrier lock detector

7	6	5	4	3	2	1	0
CARLOCK_THRES							
R/W							

Address: 0xF43F

Type: R/W

Reset: 0x19

Description: Positive edge of carrier lock detector

[7:0] CARLOCK_THRES: (signed)

LDT2 Negative edge of carrier lock detector

7	6	5	4	3	2	1	0
CARLOCK_THRES2							
R/W							

Address: 0xF440

Type: R/W

Reset: 0xE3

Description: Negative edge of carrier lock detector

[7:0] CARLOCK_THRES2: (signed)

CFRICFG CFRINIT management configuration

7	6	5	4	3	2	1	0
RESERVED							NEG_CFRSTEP
R							R/W

Address: 0xF441

Type: R/W

Reset: 0xF8

Description:

Note: previous channel = channel captured during previous locking process.

[0] NEG_CFRSTEP: 1: negative increment mode for CFRINIT (also valid for RF frequency increments).
0: positive increment mode for CFRINIT (also valid for RF frequency increments). (unsigned)

CFRUP1 Upper limit of carrier offset

7	6	5	4	3	2	1	0
CFR_UP[15:8]							
R/W							

Address: 0xF442

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] CFR_UP: (signed)

CFRUP0 Upper limit of carrier offset

7	6	5	4	3	2	1	0
CFR_UP[7:0]							
R/W							

Address: 0xF443

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] CFR_UP: (signed)

CFRLOW1 Lower limit of carrier offset

7	6	5	4	3	2	1	0
CFR_LOW[15:8]							
R/W							

Address: 0xF446

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] CFR_LOW: (signed)

CFRLOW0 Lower limit of carrier offset

7	6	5	4	3	2	1	0
CFR_LOW[7:0]							
R/W							

Address: 0xF447

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] CFR_LOW: (signed)

CFRINIT1 Carrier offset init value

7	6	5	4	3	2	1	0
CFR_INIT[15:8]							
R/W							

Address: 0xF448

Type: R/W

Reset: Undefined

Description: Carrier offset init value

[7:0] CFR_INIT: (signed)

CFRINIT0 Carrier offset init value

7	6	5	4	3	2	1	0
CFR_INIT[7:0]							
R/W							

Address: 0xF449

Type: R/W

Reset: Undefined

Description: Carrier offset init value

[7:0] CFR_INIT: (signed)

CFRINC1 Carrier offset increment

7	6	5	4	3	2	1	0
MANUAL_CFRINC	RESERVED	CFR_INC[13:8]					
R/W	R	R/W					

Address: 0xF44A

Type: R/W

Reset: 0x0

Description: Carrier offset increment

[7] MANUAL_CFRINC: Method of calculating cfr_inc (the step increment used in carrier searches):
0: automatic mode, see cfrinc_mode[1:0] below.
1: manual mode. Value set in cfr_inc[13:3]. (unsigned)

[5:0] CFR_INC: Carrier search step size.
Increment in MHz = Mclk * CFR_INC / 2^13 (unsigned)

CFRINC0 Carrier offset increment

7	6	5	4	3	2	1	0
CFR_INC[7:3]					RESERVED		
R/W					R		

Address: 0xF44B

Type: R/W

Reset: 0x31

Description: Carrier offset increment

[7:3] CFR_INC: Carrier search step size.
Increment in MHz = Mclk * CFR_INC / 2^13 (unsigned)

CFR2 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[23:16]							
R/W							

Address: 0xF44C

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] CAR_FREQ: (signed)

CFR1 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[15:8]							
R/W							

Address: 0xF44D

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] CAR_FREQ: (signed)

CFR0 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[7:0]							
R/W							

Address: 0xF44E

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] CAR_FREQ: (signed)

LDI Carrier lock indicator accumulator

7	6	5	4	3	2	1	0
LOCK_DET_INTEGR							
R							

Address: 0xF44F

Type: R

Reset: Undefined

Description: Especially useful in DVBS1/legacy DTV. not in DVBS2. The diagnostic on this digital value is provided by DSTATUS/car_lock.

[7:0] LOCK_DET_INTEGR: > LDT.carlock_thres: carrier locked, DSSTATSUS.car_lock=1.
< LDT2.carlock_thres2: carrier unlocked, DSTATSUS.car_lock=0.
car_lock functions by hysteresis. (signed)

TMGCFG Timing loop configuration

7	6	5	4	3	2	1	0
TMGLOCK_BETA		RESERVED	DO_TIMING_CORR	RESERVED		TMG_MINFREQ	
R/W		R	R/W	R		R/W	

Address: 0xF450

Type: R/W

Reset: 0xD3

Description: Timing loop configuration

[7:6] TMGLOCK_BETA: Timing Lock Indicator loop speed
00: Minimum speed
01:
10:
11: Maximum speed
Acceleration +1 if DSTATUS3/gamma_lowbaudrate=1 as long as the demodulator is not locked. (unsigned)

[4] DO_TIMING_CORR: DVBS2 only
1: use the symbol rate offset calculated on the 2nd PLHeader (unsigned)

[1:0] TMG_MINFREQ: compensate for symbol minimum rate
tmg_minfreq 00 01 10 11
SFRxx min: 1/32 1/128 1/512 1/2048 MCLK
at 135 MHz 4.2 1.06 0.264 0.066 MSymb/s (unsigned)

RTC Timing loop DVBS1/legacy DTV

7	6	5	4	3	2	1	0
TMGALPHA_EXP				TMGBETA_EXP			
R/W				R/W			

Address: 0xF451

Type: R/W

Reset: 0x88

Description: This register is used primarily for DVBS1/legacy DTV.

[7:4] TMGALPHA_EXP: 0000: alpha stopped
0001: slowest
1111: fastest (unsigned)

[3:0] TMGBETA_EXP: 0000: beta stopped
0001: slowest
1111: fastest (unsigned)

RTCS2 Timing loop specific to DVBS2

7	6	5	4	3	2	1	0
TMGALPHAS2_EXP				TMGBETAS2_EXP			
R/W				R/W			

Address: 0xF452

Type: R/W

Reset: 0x66

Description: This register is used by DVBS2. Same description as RTC.

[7:4] TMGALPHAS2_EXP: (unsigned)

[3:0] TMGBETAS2_EXP: (unsigned)

TMGTHRISE Postitive edge of timing lock detector

7	6	5	4	3	2	1	0
TMGLOCK_THRISE							
R/W							

Address: 0xF453

Type: R/W

Reset: 0x20

Description: Postitive edge of timing lock detector

[7:0] TMGLOCK_THRISE: (unsigned)

TMGTHFALL Negative edge of timing lock detector

7	6	5	4	3	2	1	0
TMGLOCK_THFALL							
R/W							

Address: 0xF454

Type: R/W

Reset: 0x0

Description: Negative edge of timing lock detector

[7:0] TMGLOCK_THFALL: (unsigned)

SFRUPRATIO — Ratio to calculate SFRUP

7	6	5	4	3	2	1	0
SFR_UPRATIO							
R/W							

Address: 0xF455

Type: R/W

Reset: 0x40

Description: Ratio to calculate SFRUP

[7:0] SFR_UPRATIO: (unsigned)

SFRLOWRATIO — Ratio to calculate SFRLOW

7	6	5	4	3	2	1	0
SFR_LOWRATIO							
R/W							

Address: 0xF456

Type: R/W

Reset: 0xE0

Description: Ratio to calculate SFRLOW

[7:0] SFR_LOWRATIO: (unsigned)

KREFTMG — Reference level for the symbol rate part of the coarse steps

7	6	5	4	3	2	1	0
KREF_TMG							
R/W							

Address: 0xF458

Type: R/W

Reset: 0x70

Description: Reference level for the symbol rate part of the coarse steps

[7:0] KREF_TMG: kref_tmg_absolu = (KREF_TMG + 0x80) * agc2_ref / 2^7 (unsigned)

SFRSTEP Scan and centering increment steps

7	6	5	4	3	2	1	0
SFR_SCANSTEP				SFR_CENTERSTEP			
R/W				R/W			

Address: 0xF459

Type: R/W

Reset: 0x58

Description: Scan and centering increment steps

[7:4] SFR_SCANSTEP: scroll speed between SFRUP and SFRLOW during the symbol rate scan.
0000: stop
0001: slowest
1111: fastest
Subtract 1 in DVBS1/Legacy DTV if TMGCFG2.notmg_dvbs1derat = 0. (unsigned)

[3:0] SFR_CENTERSTEP: TMGREG2/1/0 content transfer speed towards SFR3/2/1 once locking is launched. This speed must be small enough not to disrupt the locking process.
0000: Stop
0001: slowest
1111: fastest (unsigned)

TMGCFG2 Timing loop additional configuration

7	6	5	4	3	2	1	0
RESERVED							SFRRATIO_FINE
R							R/W

Address: 0xF45A

Type: R/W

Reset: 0x0

Description: Timing loop additional configuration

[0] SFRRATIO_FINE: fine mode on SFRUPRATIO and SFRLOWRATIO
1: fine mode (sensitivity multiplied by 64)
SFRUP = SFR(INIT) * (1 + SFRUPRATIO/16384)
SFRLOW = SFR(INIT) * (63/64 + SFRLOWRATIO/16384)
0: normal mode (or coarse)
SFRUP = SFR(INIT) * (1 + SFRUPRATIO/256)
SFRLOW = SFR(INIT) * (0 + SFRLOWRATIO/256) (unsigned)

KREFTMG2 Coarse symbol rate reference frequency

7	6	5	4	3	2	1	0
KREF_TMG2							
R							

Address: 0xF45B

Type: R

Reset: 0x70

Description: Coarse symbol rate reference frequency

[7:0] KREF_TMG2: observation register of the current value of the coarse search symbol rate reference
Useful whenUtile quand TMGCFG2/kreftmg2_decmode[1:0]!=00. (unsigned)

SFRINIT1 Symbol rate init value

7	6	5	4	3	2	1	0
RESERVED	SFR_INIT[14:8]						
R	R/W						

Address: 0xF45E

Type: R/W

Reset: 0x3

Description: Symbol rate init value

[6:0] SFR_INIT: used at launch of certain AEPs. (unsigned)

SFRINIT0 Symbol rate init value

7	6	5	4	3	2	1	0
SFR_INIT[7:0]							
R/W							

Address: 0xF45F

Type: R/W

Reset: 0x1

Description: Symbol rate init value

[7:0] SFR_INIT: used at launch of certain AEPs. (unsigned)

SFRUP1 Symbol rate upper limit

7	6	5	4	3	2	1	0
AUTO_GUP	SYMB_FREQ_UP[14:8]						
R/W	R/W						

Address: 0xF460

Type: R/W

Reset: 0x8X

Description: Symbol rate upper limit

[7] AUTO_GUP: automatic calculation mode
1: automatic calculation based on SFRUPRATIO,
symb_freq_up below is read-only.
0: manual mode, symb_freq_up is read/write. (unsigned)

[6:0] SYMB_FREQ_UP: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 256)
TMGCFG2.sfrratio_fine=1 (fine mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 16384) (unsigned)

SFRUP0 Symbol rate upper limit

7	6	5	4	3	2	1	0
SYMB_FREQ_UP[7:0]							
R/W							

Address: 0xF461

Type: R/W

Reset: Undefined

Description: Symbol rate upper limit

[7:0] SYMB_FREQ_UP: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 256)
TMGCFG2.sfrratio_fine=1 (fine mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 16384) (unsigned)

SFRLOW1 Symbol rate lower limit

7	6	5	4	3	2	1	0
AUTO_GLOW	SYMB_FREQ_LOW[14:8]						
R/W	R/W						

Address: 0xF462

Type: R/W

Reset: 0x8X

Description: Symbol rate lower limit

[7] AUTO_GLOW: automatic calculation mode
1: automatic calculation based on SFRLOWRATIO, symb_freq_low below is read-only.
0: manual mode, symb_freq_low is read/write. (unsigned)

[6:0] SYMB_FREQ_LOW: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRLOW = SFR * (0 + SFRLOWRATIO / 256)
TMGCFG2.sfrratio_fine = 1 (fine mode) in automatic mode:
SFRLOW = SFR * (63 / 64 + SFRLOWRATIO / 16384) (unsigned)

SFRLOW0 Symbol rate lower limit

7	6	5	4	3	2	1	0
SYMB_FREQ_LOW[7:0]							
R/W							

Address: 0xF463

Type: R/W

Reset: Undefined

Description: Symbol rate lower limit

[7:0] SYMB_FREQ_LOW: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRLOW = SFR * (0 + SFRLOWRATIO / 256)
TMGCFG2.sfrratio_fine = 1 (fine mode) in automatic mode:
SFRLOW = SFR * (63 / 64 + SFRLOWRATIO / 16384) (unsigned)

SFR3 Current symbol rate

7	6	5	4	3	2	1	0
SYMB_FREQ[31:24]							
R/W							

Address: 0xF464

Type: R/W

Reset: 0x3

Description: Current symbol rate

[7:0] SYMB_FREQ: Bits 7:0 are read-only. (unsigned)

SFR2 Current symbol rate

7	6	5	4	3	2	1	0
SYMB_FREQ[23:16]							
R/W							

Address: 0xF465

Type: R/W

Reset: 0x1

Description: Current symbol rate

[7:0] SYMB_FREQ: Bits 7:0 are read-only. (unsigned)

SFR1 Current symbol rate

7	6	5	4	3	2	1	0
SYMB_FREQ[15:8]							
R/W							

Address: 0xF466

Type: R/W

Reset: 0x0

Description: Current symbol rate

[7:0] SYMB_FREQ: Bits 7:0 are read-only. (unsigned)

SFR0 Current symbol rate

7	6	5	4	3	2	1	0
SYMB_FREQ[7:0]							
R/W							

Address: 0xF467

Type: R

Reset: 0x0

Description: Current symbol rate

[7:0] SYMB_FREQ: Bits 7:0 are read-only. (unsigned)

TMGREG2 Timing recovery accumulator

7	6	5	4	3	2	1	0
TMGREG[23:16]							
R/W							

Address: 0xF468

Type: R/W

Reset: 0x0

Description: Timing recovery accumulator

[7:0] TMGREG: (unsigned)

TMGREG1 Timing recovery accumulator

7	6	5	4	3	2	1	0
TMGREG[15:8]							
R/W							

Address: 0xF469

Type: R/W

Reset: 0x0

Description: Timing recovery accumulator

[7:0] TMGREG: (unsigned)

TMGREG0 Timing recovery accumulator

7	6	5	4	3	2	1	0
TMGREG[7:0]							
R/W							

Address: 0xF46A

Type: R/W

Reset: 0x0

Description: Timing recovery accumulator

[7:0] TMGREG: (unsigned)

TMGLOCK1 Timing lock indicator accumulator

7	6	5	4	3	2	1	0
TMGLOCK_LEVEL[15:8]							
R							

Address: 0xF46B

Type: R

Reset: Undefined

Description: The diagnostic on this digital value is provided by the DSTATUS/tmglock_quality field. It uses the TMGTHRISE/tmglock_thrise and TMGTHFALL/tmglock_thfall limits. tmglock_quality[0] simply indicates that tmglock_level > tmglock_thfall tmglock_quality[1] functions by hysteresis on tmglock_level with tmglock_thrise and tmglock_thfall.

[7:0] TMGLOCK_LEVEL: (signed)

TMGLOCK0 Timing lock indicator accumulator

7	6	5	4	3	2	1	0
TMGLOCK_LEVEL[7:0]							
R							

Address: 0xF46C

Type: R

Reset: Undefined

Description: Timing lock indicator accumulator

[7:0] TMGLOCK_LEVEL: (signed)

TMGOBS Observation of the timing loop

7	6	5	4	3	2	1	0
ROLLOFF_STATUS		RESERVED					
R		R					

Address: 0xF46D

Type: R

Reset: Undefined

Description: Observation of the timing loop

[7:6] ROLLOFF_STATUS: Roll-off in progress (list DVBS2)
00: 35%
01: 25%
10: 20%
(11: 15%) (unsigned)

EQUALCFG DFE equalizer configuration

7	6	5	4	3	2	1	0
RESERVED	EQUAL_ON	RESERVED			MU_EQUALDFE		
R	R/W	R			R/W		

Address: 0xF46F

Type: R/W

Reset: 0x41

Description: DFE equalizer configuration

[6] EQUAL_ON: 1: activate the equalizer
0: stop and reset the equalizer. Disconnection of data flow and coefficient reset. (unsigned)

[2:0] MU_EQUALDFE: DFE eEqualiser loop speed.
111: Fastest
100: median value
001: Very slow (good for tracking)
000: Coefficients frozen (but equaliser still active). (unsigned)

EQUAIy DFE Equalizer observation

7	6	5	4	3	2	1	0
EQUA_ACCIy							
R/W							

Address: 0xF470 + (y-1) * 0x2 (y=1 to 8)

Type: R/W

Reset: Undefined

Description: Observation of equaliser behavior:
EQUAI1+EQUAQ1: echo level between 0 and 1 symbols delay.
..
EQUAI8+EQUAQ8: echo level between 7 and 8 symbols delay.

[7:0] EQUA_ACCIy: (signed)

EQUAQy Equalizer observation

7	6	5	4	3	2	1	0
EQUA_ACCQy							
R/W							

Address: 0xF471+ (y-1) * 0x2 (y=1 to 8)

Type: R/W

Reset: Undefined

Description: Equalizer observation

[7:0] EQUA_ACCQy: (signed)

NNOSDATAT1 Linear noise normalized on the data

7	6	5	4	3	2	1	0
NOSDATAT_NORMED[15:8]							
R/W							

Address: 0xF480

Type: R/W

Reset: Undefined

Description: Noise level (in modulus) normalized on the data.

[7:0] NOSDATAT_NORMED: nosdatat_normed = 2^6 * nosdatat_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdatat_normed = 0x4000 -> noise as strong as the signal
nosdatat_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSDATAT0 Linear noise normalized on the data

7	6	5	4	3	2	1	0
NOSDATAT_NORMED[7:0]							
R/W							

Address: 0xF481

Type: R/W

Reset: Undefined

Description: Noise level (in modulus) normalized on the data.

[7:0] NOSDATAT_NORMED: nosdatat_normed = 2^6 * nosdatat_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdatat_normed = 0x4000 -> noise as strong as the signal
nosdatat_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSDATA1 Quadratic noise normalized on the data

7	6	5	4	3	2	1	0
NOSDATA_NORMED[15:8]							
R/W							

Address: 0xF482

Type: R/W

Reset: Undefined

Description: Noise level (in squared modulus) normalized on the data.

[7:0] NOSDATA_NORMED: nosdata_normed = 2^12 * nosdata_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdata_normed = 0x4000 -> noise as strong as the signal
nosdata_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSDATA0 Quadratic noise normalized on the data

7	6	5	4	3	2	1	0
NOSDATA_NORMED[7:0]							
R/W							

Address: 0xF483

Type: R/W

Reset: Undefined

Description: Noise level (in squared modulus) normalized on the data.

[7:0] NOSDATA_NORMED: nosdata_normed = 2^12 * nosdata_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdata_normed = 0x4000 -> noise as strong as the signal
nosdata_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLHT1 Linear noise normalized on the structures

7	6	5	4	3	2	1	0
NOSPLHT_NORMED[15:8]							
R/W							

Address: 0xF484

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Noise level (in modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLHT_NORMED: nosplht_normed = 2^6 * nosplht_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplht_normed = 0x4000 -> noise as strong as the signal
nosplht_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLHT0 Linear noise normalized on the structures

7	6	5	4	3	2	1	0
NOSPLHT_NORMED[7:0]							
R/W							

Address: 0xF485

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Noise level (in modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLHT_NORMED: nosplht_normed = 2^6 * nosplht_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplht_normed = 0x4000 -> noise as strong as the signal
nosplht_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLH1 Quadratic noise normalized on the structures

7	6	5	4	3	2	1	0
NOSPLH_NORMED[15:8]							
R/W							

Address: 0xF486

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Noise level (in squared modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLH_NORMED: nosplh_normed = 2^12 * nosplh_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplh_normed = 0x4000 -> noise as strong as the signal
nosplh_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLH0 Quadratic noise normalized on the structures

7	6	5	4	3	2	1	0
NOSPLH_NORMED[7:0]							
R/W							

Address: 0xF487

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Noise level (in squared modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLH_NORMED: nosplh_normed = 2^12 * nosplh_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplh_normed = 0x4000 -> noise as strong as the signal
nosplh_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSDATAT1 Absolute linear noise on the data

7	6	5	4	3	2	1	0
NOSDATAT_UNNORMED[15:8]							
R/W							

Address: 0xF488

Type: R/W

Reset: Undefined

Description: Absolute (non-normalized) noise level (in modulus) on the data.
This register contains the value that is historically compatible with the previous generations of satellite decoders.

[7:0] NOSDATAT_UNNORMED: Decimal point between bit 7 and bit 8
nosdatat_unnormed = 0x0200 -> loss of LSB of signal due to noise
nosdatat_unnormed = 0x0400 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSDATAT0 Absolute linear noise on the data

7	6	5	4	3	2	1	0
NOSDATAT_UNNORMED[7:0]							
R/W							

Address: 0xF489

Type: R/W

Reset: Undefined

Description: Absolute (non-normalized) noise level (in modulus) on the data.
This register contains the value that is historically compatible with the previous generations of satellite decoders.

[7:0] NOSDATAT_UNNORMED: Decimal point between bit 7 and bit 8
nosdatat_unnormed = 0x0200 -> loss of LSB of signal due to noise
nosdatat_unnormed = 0x0400 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSDATA1 Absolute quadratic noise on the data

7	6	5	4	3	2	1	0
NOSDATA_UNNORMED[15:8]							
R/W							

Address: 0xF48A

Type: R/W

Reset: Undefined

Description: Absolute (non-normalized) noise level (in squared modulus) on the data.

[7:0] NOSDATA_UNNORMED: Decimal point between bit 1 and bit 2
nosdata_unnormed = 0x0010 -> loss of LSB of signal due to noise
nosdata_unnormed = 0x0040 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSDATA0 Absolute quadratic noise on the data

7	6	5	4	3	2	1	0
NOSDATA_UNNORMED[7:0]							
R/W							

Address: 0xF48B

Type: R/W

Reset: Undefined

Description: Absolute (non-normalized) noise level (in squared modulus) on the data.

[7:0] NOSDATA_UNNORMED: Decimal point between bit 1 and bit 2
nosdata_unnormed = 0x0010 -> loss of LSB of signal due to noise
nosdata_unnormed = 0x0040 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSPLHT1 Absolute linear noise on the structures

7	6	5	4	3	2	1	0
NOSPLHT_UNNORMED[15:8]							
R/W							

Address: 0xF48C

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Absolute (non-normalized) noise level (in modulus) on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLHT_UNNORMED: Decimal point between bit 7 and bit 8
nosplht_unnormed = 0x0200 -> loss of LSB of signal due to noise
nosplht_unnormed = 0x0400 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSPLHT0 Absolute linear noise on the structures

7	6	5	4	3	2	1	0
NOSPLHT_UNNORMED[7:0]							
R/W							

Address: 0xF48D

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Absolute (non-normalized) noise level (in modulus) on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLHT_UNNORMED: Decimal point between bit 7 and bit 8
nosplht_unnormed = 0x0200 -> loss of LSB of signal due to noise
nosplht_unnormed = 0x0400 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSPLH1 Absolute quadratic noise on the structures

7	6	5	4	3	2	1	0
NOSPLH_UNNORMED[15:8]							
R/W							

Address: 0xF48E

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Absolute (non-normalized) noise level (in squared modulus) on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLH_UNNORMED: Decimal point between bit 1 and bit 2
nosplh_unnormed = 0x0010 -> loss of LSB of signal due to noise
nosplh_unnormed = 0x0040 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSPLH0 Absolute quadratic noise on the structures

7	6	5	4	3	2	1	0
NOSPLH_UNNORMED[7:0]							
R/W							

Address: 0xF48F

Type: R/W

Reset: Undefined

Description: DVBS2 only.
Absolute (non-normalized) noise level (in squared modulus) on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] NOSPLH_UNNORMED: Decimal point between bit 1 and bit 2
nosplh_unnormed = 0x0010 -> loss of LSB of signal due to noise
nosplh_unnormed = 0x0040 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

CAR2CFG Carrier loop 2 configuration

7	6	5	4	3	2	1	0
RESERVED	CARRIER3_DISABLE	RESERVED			ROTA2ON	PH_DET_ALGO2	
R	R/W	R			R/W	R/W	

Address: 0xF490

Type: R/W

Reset: 0x6

Description: Carrier loop 2 configuration

[6] CARRIER3_DISABLE: Bypass carrier 3 loop (unsigned)

[2] ROTA2ON: 1: carrier 2 derotator in action
0: carrier 2 loop open (unsigned)

[1:0] PH_DET_ALGO2: algorithm used to calculate the phase error on the QPSK symbols:
00: Algo 0: For CNR>7dB (Legacy compatibility)
01: Algo 1: For CNR<7dB (Legacy compatibility)
10: Algo 2: 900 native algorithm; recommended.
11: -- (unsigned)

CFR2CFR1 Carrier offset transfer control

7	6	5	4	3	2	1	0
CFR2TOCFR1_DVBS1		EN_S2CAR2CENTER	DIS_BCHERRCFR2	RESERVED	CFR2TOCFR1_BETA		
R/W		R/W	R/W	R	R/W		

Address: 0xF491

Type: R/W

Reset: 0x65

Description: Carrier offset transfer control between registers CFR2 to CFR1.

[7:6] CFR2TOCFR1_DVBS1: These bits control how the value in CFR2 is transferred by small increments to CFR1 in DVBS1/Legacy DTV mode:
00: stop Carrier loop 2 in DVBS1/Legacy DTV mode.
01: accelerated carrier loop 2 operation during start-up to improve locktime (DSTATUS/car_lock=1). As soon as DSTATUS/car_lock=1, the value in carrier 2 is transfered to carrier 1 in increments of 2^-16 symbols until CFR2 is within +-1/1024 of a symbol. After which this loop is stopped (for ever).
10: Continuous transfer of CFR2->CFR1.
11:Continuous transfer ofCFR2->CFR1 as soon as ICFR2I exceeds1/1024th of a symbol. (unsigned)

[5] EN_S2CAR2CENTER: Re-centering of CFR2 by small increments to CFR1 in DVBS2 mode when cfr2tocfr1_beta=000
1: transfer of CFR2 into CFR1 once DSTATUS/car_lock=1 by steps of 2^-16 symbols until CFR2 is within 1/1024th of a symbol. (unsigned)

[4] DIS_BCHERRCFR2: Do wait for BCH/RS check before transferring CFR2 to CFR1 (not recommended, do not forget to reduce cfr2tocfr1_beta). (unsigned)

[2:0] CFR2TOCFR1_BETA: multiplying coefficient on the carrier 2 offset controlling the speed of transfer to CFR1. Available in DVBS2(Pilots On ou Off). Automatically disconnected in DVBS1 and Legacy DTV modes:
000: transfer stopped.
001: 1/64
010: 1/32
011: 1/16
100: 1/8
101: 1/4 <---default.
110: 1/2
111: 1/1 (unsigned)

CFR22 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[23:16]							
R/W							

Address: 0xF493

Type: R/W

Reset: Undefined

Description: Normally centered on 0.

[7:0] CAR2_FREQ: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

CFR21 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[15:8]							
R/W							

Address: 0xF494

Type: R/W

Reset: Undefined

Description: Current carrier offset 2 (unit: symbols)

[7:0] CAR2_FREQ: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

CFR20 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[7:0]							
R/W							

Address: 0xF495

Type: R/W

Reset: Undefined

Description: Current carrier offset 2 (unit: symbols)

[7:0] CAR2_FREQ: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

ACLC2S2Q — Alpha specific DVBS2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)

7	6	5 4	3 2 1 0
ENAB_SPSKSYMB	RESERVED	CAR2S2_Q_ALPH_M	CAR2S2_Q_ALPH_E
R/W	R	R/W	R/W

Address: 0xF497

Type: R/W

Reset: 0x6A

Description: This register is used by DVBS2.

[7] ENAB_SPSKSYMB: Stop carrier loop 2 alpha and beta updates during DVB-S2 header, pilot and dummyPL symbols.
1: The structure symbols are never used in the calculation of alpha and beta.
0: The structure symbols contribute to alpha and beta. (unsigned)

[5:4] CAR2S2_Q_ALPH_M: (unsigned)

[3:0] CAR2S2_Q_ALPH_E: (unsigned)

ACLC2S28 — Alpha specific DVBS2 data 8PSK

7	6	5 4	3 2 1 0
OLDI3Q_MODE	RESERVED	CAR2S2_8_ALPH_M	CAR2S2_8_ALPH_E
R/W	R	R/W	R/W

Address: 0xF498

Type: R/W

Reset: 0x58

Description: This register is used by DVBS2.

[7] OLDI3Q_MODE: Use the phase detector as implemented in cut 2.0 and prior versions (unsigned)

[5:4] CAR2S2_8_ALPH_M: (unsigned)

[3:0] CAR2S2_8_ALPH_E: (unsigned)

BCLC2S2Q — Beta specific DVBS2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)

7	6	5	4	3	2	1	0
RESERVED		CAR2S2_Q_BETA_M		CAR2S2_Q_BETA_E			
R		R/W		R/W			

Address: 0xF49C

Type: R/W

Reset: 0xA5

Description: This register is used by DVBS2. Same description as BCLC2.

[5:4] CAR2S2_Q_BETA_M: (unsigned)

[3:0] CAR2S2_Q_BETA_E: (unsigned)

BCLC2S28 — Beta specific DVBS2 data 8PSK

7	6	5	4	3	2	1	0
RESERVED		CAR2S2_8_BETA_M		CAR2S2_8_BETA_E			
R		R/W		R/W			

Address: 0xF49D

Type: R/W

Reset: 0xA5

Description: This register is used by DVBS2. Same description as BCLC2.

[5:4] CAR2S2_8_BETA_M: (unsigned)

[3:0] CAR2S2_8_BETA_E: (unsigned)

PLROOT2 — Gold code description

7	6	5	4	3	2	1	0
RESERVED						PLSCRAMB_ROOT[17:16]	
R						R/W	

Address: 0xF4AC

Type: R/W

Reset: 0x0

Description: Gold code description

[1:0] PLSCRAMB_ROOT: DVBS2 Gold Code or root of PRBS X. (unsigned)

PLROOT1 Gold code description

7	6	5	4	3	2	1	0
PLSCRAMB_ROOT[15:8]							
R/W							

Address: 0xF4AD

Type: R/W

Reset: 0x0

Description: Gold code description

[7:0] PLSCRAMB_ROOT: DVBS2 Gold Code or root of PRBS X. (unsigned)

PLROOT0 Gold code description

7	6	5	4	3	2	1	0
PLSCRAMB_ROOT[7:0]							
R/W							

Address: 0xF4AE

Type: R/W

Reset: 0x1

Description: Gold code description

[7:0] PLSCRAMB_ROOT: DVBS2 Gold Code or root of PRBS X. (unsigned)

MODCODLST0 List of prohibited MODCOD

7	6	5	4	3	2	1	0
R/W							

Address: 0xF4B0

Type: R/W

Reset: 0xFF

Description: List of prohibited MODCOD

MODCODLST1 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_MODCOD29				DIS_32PSK_9_10			
R/W				R/W			

Address: 0xF4B1

Type: R/W

Reset: 0xFC

Description: List of prohibited MODCOD

[7:4] DIS_MODCOD29: disable MODCOD 29
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_32PSK_9_10: disable 32APSK 9/10
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST2 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_32PSK_8_9				DIS_32PSK_5_6			
R/W				R/W			

Address: 0xF4B2

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_32PSK_8_9: disable 32APSK 8/9
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_32PSK_5_6: disable 32APSK 5/6
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST3 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_32PSK_4_5				DIS_32PSK_3_4			
R/W				R/W			

Address: 0xF4B3

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_32PSK_4_5: disable 32APSK 4/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_32PSK_3_4: disable 32APSK 3/4
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST4 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_16PSK_9_10				DIS_16PSK_8_9			
R/W				R/W			

Address: 0xF4B4

Type: R/W

Reset: 0xC0

Description: List of prohibited MODCOD

[7:4] DIS_16PSK_9_10: disable 16APSK 9/10
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_16PSK_8_9: disable 16APSK 8/9
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST5 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_16PSK_5_6				DIS_16PSK_4_5			
R/W				R/W			

Address: 0xF4B5

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_16PSK_5_6: disable 16APSK 5/6
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_16PSK_4_5: disable 16APSK 4/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST6 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_16PSK_3_4				DIS_16PSK_2_3			
R/W				R/W			

Address: 0xF4B6

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_16PSK_3_4: disable 16APSK 3/4
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_16PSK_2_3: disable 16APSK 2/1
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST7 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_8P_9_10				DIS_8P_8_9			
R/W				R/W			

Address: 0xF4B7

Type: R/W

Reset: 0xC0

Description: List of prohibited MODCOD

[7:4] DIS_8P_9_10: disable 8PSK 9/10
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_8P_8_9: disable 8PSK 8/9
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST8 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_8P_5_6				DIS_8P_3_4			
R/W				R/W			

Address: 0xF4B8

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_8P_5_6: disable 8PSK 5/6
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_8P_3_4: disable 8PSK 3/4
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST9 List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_8P_2_3				DIS_8P_3_5			
R/W				R/W			

Address: 0xF4B9

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_8P_2_3: disable 8PSK 2/3
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_8P_3_5: disable 8PSK 3/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTA List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_9_10				DIS_QP_8_9			
R/W				R/W			

Address: 0xF4BA

Type: R/W

Reset: 0xC0

Description: List of prohibited MODCOD

[7:4] DIS_QP_9_10: disable QPSK 9/10
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_QP_8_9: disable QPSK 8/9
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTB List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_5_6				DIS_QP_4_5			
R/W				R/W			

Address: 0xF4BB

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_QP_5_6: disable QPSK 5/6
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_QP_4_5: disable QPSK 4/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTC List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_3_4				DIS_QP_2_3			
R/W				R/W			

Address: 0xF4BC

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_QP_3_4: disable QPSK 3/4
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_QP_2_3: disable QPSK 2/3
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTD List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_3_5				DIS_QP_1_2			
R/W				R/W			

Address: 0xF4BD

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_QP_3_5: disable QPSK 3/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_QP_1_2: disable QPSK 1/2
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTE List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_2_5				DIS_QP_1_3			
R/W				R/W			

Address: 0xF4BE

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] DIS_QP_2_5: disable QPSK 2/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] DIS_QP_1_3: disable QPSK 1/3
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTF List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_1_4				RESERVED			
R/W				R			

Address: 0xF4BF

Type: R/W

Reset: 0xF

Description: List of prohibited MODCOD

[7:4] DIS_QP_1_4: disable QPSK 1/4 frame (inactive):
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

GAUSSR0 Gaussien phase detector radius, R0

7	6	5	4	3	2	1	0
EN_CCIMODE	R0_GAUSSIEN						
R/W	R/W						

Address: 0xF4C0

Type: R/W

Reset: 0x98

Description: Gaussien phase detector radius, R0

[7] EN_CCIMODE: 1: switch on this machine (unsigned)

[6:0] R0_GAUSSIEN: Reference radius in Gaussian mode. (unsigned)

CCIR0 CCI phase detector radius, R0

7	6	5	4	3	2	1	0
CCIDETECT_PLHONLY	R0_CCI						
R/W	R/W						

Address: 0xF4C1

Type: R/W

Reset: 0x30

Description: CCI phase detector radius, R0

[7] CCIDETECT_PLHONLY: 1: allow switching to CCI/Gaussien mode (unsigned)

[6:0] R0_CCI: reference radius in CCI mode. (unsigned)

CCIQUANT — CCI detector quantifier

7	6	5	4	3	2	1	0
CCI_BETA			CCI_QUANT				
R/W			R/W				

Address: 0xF4C2

Type: R/W

Reset: 0xAC

Description: CCI detector quantifier

[7:5] CCI_BETA: CCI detector beta:
000: stop
001: minimum speed
111: maximum speed (unsigned)

[4:0] CCI_QUANT: Quantitive estimation on CCI (unsigned)

CCITHRES — CCI threshold detector level

7	6	5	4	3	2	1	0
CCI_THRESHOLD							
R/W							

Address: 0xF4C3

Type: R/W

Reset: 0x32

Description: CCI threshold detector level

[7:0] CCI_THRESHOLD: To be compared with the value in cci_value. (unsigned)

CCIACC — CCI detector accumulator

7	6	5	4	3	2	1	0
CCI_VALUE							
R							

Address: 0xF4C4

Type: R

Reset: Undefined

Description: CCI detector accumulator

[7:0] CCI_VALUE: Quantitive estimation of CCI in the signal.
A write to this register causes the CCI state-machine to be reset. (unsigned)

DMDRESCFG FIFO results configuration

7	6	5	4	3	2	1	0
DMDRES_RESET	RESERVED			DMDRES_STRALL	DMDRES_NEWONLY	DMDRES_NOSTORE	RESERVED
R/W	R			R/W	R/W	R/W	R

Address: 0xF4C6

Type: R/W

Reset: 0x29

Description: FIFO results configuration

[7] DMDRES_RESET: 1: reset FIFO results (unsigned)

[3] DMDRES_STRALL: 1: do not store the undecodables (unsigned)

[2] DMDRES_NEWONLY: 1: only store the new channels (unsigned)

[1] DMDRES_NOSTORE: 1: only store the tuner information and forget the channel information (both decodables and undecodables). (unsigned)

DMDRESADR FIFO results status

7	6	5	4	3	2	1	0
RESERVED	DMDRES_VALIDCFR	DMDRES_MEMFULL		DMDRES_RESNBR			
R	R	R		R			

Address: 0xF4C7

Type: R

Reset: Undefined

Description: FIFO results status

[6] DMDRES_VALIDCFR: 1: channel valid
0: channel undecodable (unsigned)

[5:4] DMDRES_MEMFULL: FIFO results load:
00: empty
01: results waiting
10: more than 8 results waiting
11: full, urgently needs to be emptied (unsigned)

[3:0] DMDRES_RESNBR: number of results waiting. (unsigned)

DMDRESDATAy FIFO results

7	6	5	4	3	2	1	0
DMDRES_DATA[63:56]							
DMDRES_DATA[55:48]							
DMDRES_DATA[47:40]							
DMDRES_DATA[39:32]							
DMDRES_DATA[31:24]							
DMDRES_DATA[23:16]							
DMDRES_DATA[15:8]							
DMDRES_DATA[7:0]							
R/W							

Address: 0xF4C8 - y * 0x1 (y=0 to 7)

Type: R/W

Reset: Undefined

Description: FIFO results

[63:0] DMDRES_DATA: The results of one captured channel stored in the FIFO.

Bit 19 indicates whether the results are valid or if the block is empty and should be discarded. The 64-bit DMDRES_DATA field must be interpreted according to the type of modulation found (DVB-S2/DVB-S/undecoded) which is indicated in bits 7:5.
In order to read the next FIFO result a single write to any of the DMDRES_DATA7..0 registers will flush the present result and index to the next.
The interpretation of the FIFO contents is as follows:
If [7] = 1 then signal = DVB-S2; If [7]=0 & [5] =1 then signal=DVBS/DSS else invalid.

63..48: SFR[15:0], symbol rate of signal found.
47..32: CFR[15:0], carrier offset 1 of signal found.
31..28: mantissa of AGC2 level of signal found.
27..24: exponent of AGC2 level of signal found. AGC2 ~ AGC2_mantissa * 2^AGC2_exponant.
23..20: noise_exponant, exponent (only) of noise level of signal found. Noise level ~ 2^noise_exponant.
19: valid_result, at 1 if the result is valid (usable). At 0 if the data is not relevant.
18: specinv_demod, local spectral inversion detected by the demodulator (for DVBS2 only).
17..16: rolloff_control[1:0], Nyquist filter type at the moment of locking (00:35% 01:25% 10:20% 11:15%).
8: Demod locked.

DVBS2:
7: constant, 1
6..2: MODCOD[4:0], MODCOD of channel found.
1..0: TYPE[1:0], TYPE of channel found.

DVBS1/Legacy DTV:
7: constant, 0
5: constant, 1
4: local spectral inversion detected by the Viterbi.
3: DVBS1 or Legacy DTV:
0: DVBS1
1: Legacy DTV
2..0: puncture rate found. 000:1/2 001:2/3 010:3/4 011:5/6 100:6/7 101:7/8.

Invalid:
7: constant, 0
5: constant, 0 (unsigned)

FFEI1..4 FFE Equaliser coefficients

7	6	5	4	3	2	1	0
FFE_ACCIy							
R/W							

Address: 0xF4D0 + (y-1) * 0x2 (y=1 to 4)

Type: R/W

Reset: Undefined

Description: FFE equaliser observation
FFEI1..FFEQ1
.....
FFEI4..FFEQ4

[7:0] FFE_ACCIy: (signed)

FFEQy FFE equaliser coefficients

7	6	5	4	3	2	1	0
FFE_ACCQy							
R/W							

Address: 0xF4D1 + (y-1) * 0x2 (y=1 to 4)

Type: R/W

Reset: Undefined

Description: FFE equaliser coefficients

[7:0] FFE_ACCQy: (signed)

FFECFG FFE equaliser configuration

7	6	5	4	3	2	1	0
RESERVED	EQUALFFE_ON	RESERVED			MU_EQUALFFE		
R	R/W	R			R/W		

Address: 0xF4D8

Type: R/W

Reset: 0x71

Description: FFE equaliser configuration

[6] EQUALFFE_ON: (unsigned)

[2:0] MU_EQUALFFE: FFE equaliser update speed.
111: Fastest
100: median value
001: Very slow (good for tracking)
000: Coefficients frozen (but equaliser still active). (unsigned)

SMAPCOEF7 LLR gain in DVBS2 QPSK

7	6	5	4	3	2	1	0
DIS_QSCALE	SMAPCOEF_Q_LLR12						
R/W	R/W						

Address: 0xF500

Type: R/W

Reset: 0x6

Description: LLR gain in DVBS2 QPSK

[7] DIS_QSCALE: disable LLR scaling factor for DVB-S2 QPSK
1: do not use scale factor
0: use scale factor (unsigned)

[6:0] SMAPCOEF_Q_LLR12: LLR gain in DVB-S2 QPSK (signed)

SMAPCOEF6 LLR gain in DVBS2 8PSK

7	6	5	4	3	2	1	0
RESERVED					ADJ_8PSKLLR1	OLD_8PSKLLR1	DIS_AB8PSK
R					R/W	R/W	R/W

Address: 0xF501

Type: R/W

Reset: 0x0

Description: LLR gain in DVBS2 8PSK

[2] ADJ_8PSKLLR1: 1: Use cut 2.0 or greater method for calculating LLRs. Add adjusting factor. (unsigned)

[1] OLD_8PSKLLR1: 1: The method of calculating LLRs prior to cut2.0 is employed. The field SMAPCOEF_32_LLR15[6:0] is used. (unsigned)

[0] DIS_AB8PSK: Disable the addition of the adjusting factor (a+b)(-I) (unsigned)

SMAPCOEF5 LLR gain in DVBS2 8PSK

7	6	5	4	3	2	1	0
DIS_8SCALE	SMAPCOEF_8P_LLR23						
R/W	R/W						

Address: 0xF502

Type: R/W

Reset: 0x4

Description: LLR gain in DVBS2 8PSK

[7] DIS_8SCALE: disable LLR scaling factor for DVB-S2 8PSK
1: do not use scale factor
0: use scale factor (unsigned)

[6:0] SMAPCOEF_8P_LLR23: (signed)

DMDPLHSTAT PLHeaders failure rate

7	6	5	4	3	2	1	0
PLH_STATISTIC							
R							

Address: 0xF520

Type: R

Reset: Undefined

Description: PLHeaders failure rate

[7:0] PLH_STATISTIC: Number of refused PLHeaders. 0 to 255. Rolls over to 0 when 255 reached. (unsigned)

LOCKTIME3 Demodulator locking time

7	6	5	4	3	2	1	0
DEMOD_LOCKTIME[31:24]							
R							

Address: 0xF522

Type: R

Reset: Undefined

Description: Demodulator locking time

[7:0] DEMOD_LOCKTIME: time taken between writing the AEP and locking. Some options available with DMDCFG3.locktime_mode.
Equation:
locking time = 2^7 * demod_locktime / Master_clock (unsigned)

LOCKTIME2 Demodulator locking time

7	6	5	4	3	2	1	0
DEMOD_LOCKTIME[23:16]							
R							

Address: 0xF523

Type: R

Reset: Undefined

Description: Demodulator locking time

[7:0] DEMOD_LOCKTIME: time taken between writing the AEP and locking. Some options available with DMDCFG3.locktime_mode.
Equation:
locking time = 2^7 * demod_locktime / Master_clock (unsigned)

LOCKTIME1 Demodulator locking time

7	6	5	4	3	2	1	0
DEMOD_LOCKTIME[15:8]							
R							

Address: 0xF524

Type: R

Reset: Undefined

Description: Demodulator locking time

[7:0] DEMOD_LOCKTIME: time taken between writing the AEP and locking. Some options available with DMDCFG3.locktime_mode.
Equation:
locking time = 2^7 * demod_locktime / Master_clock (unsigned)

LOCKTIME0 Demodulator locking time

7	6	5	4	3	2	1	0
DEMOD_LOCKTIME[7:0]							
R							

Address: 0xF525

Type: R

Reset: Undefined

Description: Demodulator locking time

[7:0] DEMOD_LOCKTIME: time taken between writing the AEP and locking. Some options available with DMDCFG3.locktime_mode.

Equation:

locking time = 2^7 * demod_locktime / Master_clock (unsigned)

17.6 TUN register descriptions

TNRCFG Tuner control configuration

7	6	5	4	3	2	1	0
TUN_ACKFAIL	TUN_TYPE			TUN_SECSTOP	TUN_VCOSRCH	TUN_MADDRESS	
R	R/W			R/W	R/W	R/W	

Address: 0xF4E0

Type: R/W

Reset: 0x6C

Description: Tuner control configuration

[7] TUN_ACKFAIL: (read-only) 1: Tuner I2C bus malfunctioning, there are acknoweldge errors. (read put to 0 on a read,unsigned)

[6:4] TUN_TYPE: selection of tuner type.
Automatic reprogramming of certain fields upon changing tuner_type except for Tuner off.
000: Tuner off, no longer program the tuner in this way.
001: STB6000
010: SATTUNER cut 1
011: STB6100
100: STV6110
101: STV6120
110: No Tuner
111: -- (unsigned)

[3] TUN_SECSTOP: implementation of operational safety.
1: introduce an I2C stop event before starting each I2C access. (unsigned)

[2] TUN_VCOSRCH: for STB6000 and STB6100 only. No effect for other types of tuners.
1: implementation of the tuner OSCM (recommended). (unsigned)

[1:0] TUN_MADDRESS: tuner Master Address
00: C0
01: C2
10: C4
11: C6
The default tuner selection is: C0 for demodulator 1, C6 for demodulator 2. (unsigned)

TNRCFG2 Tuner & input IQ control

7	6	5	4	3	2	1	0
TUN_IQSWAP	RESERVED				DIS_BWCALC	SHORT_WAITSTATES	RESERVED
R/W	R				R/W	R/W	R

Address: 0xF4E1

Type: R/W

Reset: 0x82

Description: Tuner & input IQ control

[7] TUN_IQSWAP: Swap IQ paths immediately after ADCs (to correct for external wiring inversion if necessary).
Defaut for demodulator 1 =1; default for demodulator 2 = 0. (unsigned)

[2] DIS_BWCALC: mechanism to calculate and adjust the tuner bandwidth in the Controlled Tuner:
1: active, TNRBW/tuner_bandwidth is defined automatically.
0: inactive, TNRBW/tuner_bandwidth must be entered manually. (unsigned)

[1] SHORT_WAITSTATES: global waiting times between two I2C accesses
1: divide tempo by 4 (see TNRI2CFREQ and TNRCFG3 registers). (unsigned)

TNRXTAL Tuner reference frequency

7	6	5	4	3	2	1	0
RESERVED			TUN_XTALFREQ				
R			R/W				

Address: 0xF4E4

Type: R/W

Reset: 0x1B

Description: Tuner reference frequency

[4:0] TUN_XTALFREQ: Tuner reference frequency (e.g. quartz) in MHz Ftuner= 1MHz x TUNER_XTALFREQ
Hint: 0 resets the tuner controller. (unsigned)

TNRSTEPS Step definition and various coefficients

7	6	5	4	3	2	1	0
R/W							

Address: 0xF4E7

Type: R/W

Reset: 0x5

Description: Step definition and various coefficients

TNRGAIN Tuner gain and various (static) characteristics

7	6	5	4	3	2	1	0
TUN_KDIVEN		STB6X00_OCK		TUN_GAIN			
R/W		R/W		R/W			

Address: 0xF4E8

Type: R/W

Reset: 0x49

Description: Tuner gain and various (static) characteristics

[7:6] TUN_KDIVEN: output divider ratio
STB6x00: K/k[1:0]
SATTUNER and STB6110: odiv[1:0] (unsigned)

[5:4] STB6X00_OCK: STB6x00 only
field VCO/ock[1:0] (VCO search clock) (unsigned)

[3:0] TUN_GAIN: tuner gain. In the same units as the proposed tuner. (unsigned)

TNRRF1 Tuner RF frequency (in MHz)

7	6	5	4	3	2	1	0
TUN_RFFREQ[17:10]							
R/W							

Address: 0xF4E9

Type: R/W

Reset: 0x4B

Description: Tuner RF frequency (in MHz)

[7:0] TUN_RFFREQ: Tuner RF frequency.
RF_Freq = tuner_rffreq[17:0] / 64 (unsigned)

TNRRF0 Tuner RF frequency (in MHz)

7	6	5	4	3	2	1	0
TUN_RFFREQ[9:2]							
R/W							

Address: 0xF4EA

Type: R/W

Reset: 0x0

Description: Tuner RF frequency (in MHz)

[7:0] TUN_RFFREQ: Tuner RF frequency.
RF_Freq = tuner_rffreq[17:0] / 64 (unsigned)

TNRBW Tuner bandwidth

7	6	5	4	3	2	1	0
TUN_RFFREQ[1:0]		TUN_BW					
R/W		R/W					

Address: 0xF4EB

Type: R/W

Reset: 0x1F

Description: Tuner bandwidth

[7:6] TUN_RFFREQ: Tuner RF frequency.
RF_Freq = tuner_rffreq[17:0] / 64 (unsigned)

[5:0] TUN_BW: tuner bandwidth. The value written in this field will be replaced by an automatic calculation if TNRCFG2.dis_bwcalc = 0. The value 0x00 is a special case. This value indicates that there is no desire to modify the tuner_bandwidth field by wirting in TNRBW. This is specially designed for when we want to write the two LSB of tuner_rffreq without touching tuner_bandwidth. The value 0 is chosen for this special case because a bandwidth of 0 MHz is meaningless. (unsigned)

TNRADJ Tuner specific register configurations

7	6	5	4	3	2	1	0
RESERVED	STB61X0_CALTIME	RESERVED					
R	R/W	R					

Address: 0xF4EC

Type: R/W

Reset: 0x0

Description: Tuner register fields are automatically accessed and programmed with the values contained herein (see tuner datasheet for functionality).

[6] STB61X0_CALTIME: (unsigned)

TNRCTL2 CONTROL2 register of STV6110

7	6	5	4	3	2	1	0
R/W							

Address: 0xF4ED

Type: R/W

Reset: 0x97

Description: Refer to STV6110 datasheet for more information.

TNRCFG3 Additional tuner register configurations

7	6	5	4	3	2	1	0
RESERVED			TUN_PLLFREQ			TUN_I2CFREQ_MODE	
R			R/W			R/W	

Address: 0xF4EE

Type: R/W

Reset: 0x0

Description: Additional tuner register configurations

[4:2] TUN_PLLFREQ: calculation method for the STB0900 Master Clock (field tuner_masterclock:tuner_mclkdecimal (11 bits), see TNRMCLK and TNRXTAL and chapter “Le controle de la PLL du 900“):
000: automatic based on tuner Xtal
The STB0900 reference clock is declared as ref clock = PLL900 = TNRXTAL
001: the STB0900 PLL functions with a local reference 27 MHz
010: the STB0900 PLL functions with a local reference 16 MHz
011: the STB0900 PLL functions with a local reference 4 MHz
100: --
101: --
110: Same as 000, but clock ref PLL900 = 0.5 * TNRXTAL
111: manual mode (unsigned)

[1:0] TUN_I2CFREQ_MODE: calculation method for the I2C frequency and the delay times between 2 I2C accesses:
00: automatic cki2c = 100 kHz delay = 11.2 msec
01: automatic cki2c = 50 kHz delay = 22.5 msec
10: automatic cki2c = 200 kHz delay = 5.6 msec
11: manual
cki2c = Mclk/(8*4*tuner_i2cfreq)
delay = 128*9*8*4*tuner_i2cfreq / Mclk = 128*9 / cki2c
TNRCFG2/short_waitstates=1 -> divide all the above delay values by 4. (unsigned)

TNRLD Tuner verification status (read only)

7	6	5	4	3	2	1	0
TUNLD_VCOING	TUN_REG1FAIL	TUN_REG2FAIL	TUN_REG3FAIL	TUN_REG4FAIL	TUN_REG5FAIL	TUN_BWING	TUN_LOCKED
R	R	R	R	R	R	R	R

Address: 0xF4F0

Type: R

Reset: Undefined

Description: Tuner diagnostics.
Any value other than 0x81 in this register indicates a fault.

[7] TUNLD_VCOING: 0: VCO adjustment in progress. (unsigned)

[6] TUN_REG1FAIL: 1: the 1st register of tuner control is different. (unsigned)

[5] TUN_REG2FAIL: 1: the 2nd register of tuner control is different. (unsigned)

[4] TUN_REG3FAIL: 1: the 3rd register of tuner control is different. (unsigned)

[3] TUN_REG4FAIL: 1: the 4th register of tuner control is different. (unsigned)

[2] TUN_REG5FAIL: 1: the 5th register of tuner control is different. (unsigned)

[1] TUN_BWING: 1: bandwidth adjustment in progress. (unsigned)

[0] TUN_LOCKED: 1: tuner is locked. (unsigned)

TNROBSL Control tuner observation

7	6	5	4	3	2	1	0
TUN_I2CABORTED	TUN_LPEN	TUN_FCCK	TUN_I2CLOCKED	TUN_PROGDONE		TUN_RFRESTE[9:8]	
R	R	R	R	R		R	

Address: 0xF4F6

Type: R

Reset: Undefined

Description: Control tuner observation

[7] TUN_I2CABORTED: I2C malfunction alarm. I2C collisions may have taken place.
1: one or more I2C accesses have been sunk by the I2C repeater. (unsigned)

[6] TUN_LPEN: RF local oscillator status
0: RF local oscillator locking/programming in progress.
1: RF local oscillator locked/programmed or not restarted. (unsigned)

[5] TUN_FCCK: tuner bandwidth status
1: tuner bandwidth locking/programming in progress.
0: tuner bandwidth locked/programmed or not restarted. (unsigned)

[4] TUN_I2CLOCKED: tuner programming success. Final diagnostic.
1: procedure completed with success, tuner locked.
0: procedure incomplete, in progress or failure, tuner unlocked. (unsigned)

[3:2] TUN_PROGDONE: 00: (nothing)
01: programming in progress
10: programming succeeded
11: programming failure (512 attempts for nothing). (unsigned)

[1:0] TUN_RFRESTE: 8 LSBs of the remainder calculation to obtain the RF frequency currently programmed. (unsigned)

TNRRESTE RF frequency remainder

7	6	5	4	3	2	1	0
TUN_RFRESTE[7:0]							
R							

Address: 0xF4F7

Type: R

Reset: Undefined

Description: RF frequency remainder

[7:0] TUN_RFRESTE: 8 LSBs of the remainder calculation to obtain the RF frequency currently programmed. (unsigned)

17.7 DVB1 register descriptions

VITSCALE Additional configuration of Viterbi decoder

7	6	5	4	3	2	1	0
NVTH_NOSRANGE	VERROR_MAXMODE	RESERVED		NSLOWSN_LOCKED	RESERVED	DIS_RSFLOCK	RESERVED
R/W	R/W	R		R/W	R	R/W	R

Address: 0xF532

Type: R/W

Reset: 0x0

Description: Additional configuration of Viterbi decoder

[7] NVTH_NOSRANGE: Automatic calculation of Viterbi threshold as a function of noise. Used during acquisition.
0: The Viterbi threshold is calculated as a function of noise measured by the demodulator
1: No automatic adaptation of Vth. The Vth is taken from the VTHxx registers programmed by I2C. (unsigned)

[6] VERROR_MAXMODE: observation mode of VERROR register.
1: VERROR contains the maximum value achieved since its last reinitialization (via I2C write); very useful for adjusting the limits of each puncture rate or to obtain the maximum observed.
0: VERROR contains the instantaneous value of the number of errors. (unsigned)

[3] NSLOWSN_LOCKED: Slow the VERROR calculation (for a smoother result)
0: slow down
1: don‘t slow down (unsigned)

[1] DIS_RSFLOCK: False lock detection from Reed-Solomon decoder
1: Retrigger Viterbi if false lock detected
0: ignore false lock detection, do nothing. (unsigned)

FECM Viterbi decoder configuration

7	6	5	4	3	2	1	0
DSS_DVB	RESERVED		DSS_SRCH	RESERVED		SYNCVIT	IQINV
R	R		R/W	R		R/W	R

Address: 0xF533

Type: R/W

Reset: 0x10

Description: Viterbi decoder configuration

[7] DSS_DVB: standard used
1: Legacy DTV
0: DVBS1 (read put to 0 on a read,unsigned)

[4] DSS_SRCH: norm searching mode
1: automatic DVBS1/Legacy DTV search
0: manual search, program FECM.dss_dvb. (unsigned)

[1] SYNCVIT: 1: freeze the synchro word search mechanism. Very dangerous in case of unlocking: the machine will be incapable of re-hooking. (unsigned)

[0] IQINV: observation of the local spectral inversion detected by the Viterbi decoder. In manual mode, i2csym = DEMOD.specinv_control(0). (read put to 0 on a read,unsigned)

VTH12 Error threshold for puncture rate 1/2

7	6	5	4	3	2	1	0
VTH12							
R/W							

Address: 0xF534

Type: R/W

Reset: 0xD0

Description: Error threshold for puncture rate 1/2

[7:0] VTH12: (unsigned)

VTH23 Error threshold for puncture rate 2/3

7	6	5	4	3	2	1	0
VTH23							
R/W							

Address: 0xF535

Type: R/W

Reset: 0x7D

Description: Error threshold for puncture rate 2/3

[7:0] VTH23: (unsigned)

VTH34 Error threshold for puncture rate 3/4

7	6	5	4	3	2	1	0
VTH34							
R/W							

Address: 0xF536

Type: R/W

Reset: 0x53

Description: Error threshold for puncture rate 3/4

[7:0] VTH34: (unsigned)

VTH56 Error threshold for puncture rate 5/6

7	6	5	4	3	2	1	0
VTH56							
R/W							

Address: 0xF537

Type: R/W

Reset: 0x2F

Description: Error threshold for puncture rate 5/6

[7:0] VTH56: (unsigned)

VTH67 Error threshold for puncture rate 6/7

7	6	5	4	3	2	1	0
VTH67							
R/W							

Address: 0xF538

Type: R/W

Reset: 0x24

Description: Error threshold for puncture rate 6/7

[7:0] VTH67: (unsigned)

VTH78 Error threshold for puncture rate 7/8

7	6	5	4	3	2	1	0
VTH78							
R/W							

Address: 0xF539

Type: R/W

Reset: 0x1F

Description: Error threshold for puncture rate 7/8

[7:0] VTH78: (unsigned)

VITCURPUN Current puncture rate on the Viterbi decoder

7	6	5	4	3	2	1	0
RESERVED			VIT_CURPUN				
R			R				

Address: 0xF53A

Type: R

Reset: Undefined

Description: Current puncture rate on the Viterbi decoder

[4:0] VIT_CURPUN: current puncture rate
0x0d:1/2 0x12:2/3 0x15:3/4 0x18:5/6 0x19:6/7 0x1a:7/8 (unsigned)

VERROR Current error rate

7	6	5	4	3	2	1	0
REGERR_VIT							
R/W							

Address: 0xF53B

Type: R/W

Reset: Undefined

Description: Current error rate

[7:0] REGERR_VIT: current error rate or maximum observed by the Viterbi decoder.
Equation:
proportion of errors = regerr_vit / 2048
Examples:
0x00 = no errors, signal perfect
0xFF = 6.23% errors (255 bits corrected out of 2048). (read put to 0 on a write,unsigned)

PRVIT List of authorized puncture rates

7	6	5	4	3	2	1	0
RESERVED	DIS_VTHLOCK	E7_8VIT	E6_7VIT	E5_6VIT	E3_4VIT	E2_3VIT	E1_2VIT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF53C

Type: R/W

Reset: 0x3F

Description: List of authorized puncture rates

[6] DIS_VTHLOCK: Automatic adjustment of VTH as a function of noise after decoder lock.
1: automatic adjustment enabled
0: disabled (unsigned)

[5] E7_8VIT: authorization of rate 7/8 (unsigned)

[4] E6_7VIT: authorization of rate 6/7 (unsigned)

[3] E5_6VIT: authorization of rate 5/6 (unsigned)

[2] E3_4VIT: authorization of rate 3/4 (unsigned)

[1] E2_3VIT: authorization of rate 2/3 (unsigned)

[0] E1_2VIT: authorization of rate 1/2 (unsigned)

VAVSRVIT — Viterbi decoder search speeds

7	6	5 4	3 2	1 0
AMVIT	FROZENVIT	SNVIT	TOVVIT	HYPVIT
R/W	R/W	R/W	R/W	R/W

Address: 0xF53D

Type: R/W

Reset: 0x0

Description: Viterbi decoder search speeds

[7] AMVIT: puncture rate search manual or automatic mode. Used with frozenvit below.
1: manual search. Each positive edge on frozenvit increments the internal puncture rate search mechanism.
0: automatic mode, normal (unsigned)

[6] FROZENVIT: freeze the synchronizations
If amvit=0:
1: freeze the puncture rate search mechanism
0: automatic mode, normal
If amvit=1: each positive edge of this bit increments the internal puncture rate search machine. (unsigned)

[5:4] SNVIT: measuring time (number of symbols) for evaluating VERROR.regerr_vit
00: 4096 bits
01: 16384 bits
10: 65536 bits
11: 262144 bits (unsigned)

[3:2] TOVVIT: synchro word search time-out.
If no synchro word has been found during this time, the internal puncture rate search mechanism switches itself back on.
This time-out counter only starts once a puncture rate has been found (VSTATUSVIT.prfvit goes to 1). 00: 32768 bits or the time for 23 packets DVB+Legacy DTV
01: 65536 bits 46 packets DVB+Legacy DTV
10: 131072 bits 93 packets DVB+Legacy DTV
11: 262144 bits 186 packets DVB+Legacy DTV (unsigned)

[1:0] HYPVIT: Viterbi decoder locking validation or devalidation limit
If the specified number of consecutive synchro words are detected, then the Viterbi decoder is locked (VSTATUSVIT.lockedvit goes to 1).
If the specified number of consecutive synchro words are lost, then the Viterbi decoder is unlocked (VSTATUSVIT.lockedvit goes to 0). The puncture rate search mechanism switches itself back on. 00: 16 consecutive synchro words found or lost
01: 32 consecutive synchro words found or lost
10: 64 consecutive synchro words found or lost
11: 128 consecutive synchro words found or lost (unsigned)

VSTATUSVIT Viterbi decoder status

7	6	5	4	3	2	1	0
RESERVED			PRFVIT	LOCKEDVIT	RESERVED		
R			R/W	R/W	R		

Address: 0xF53E

Type: R/W

Reset: Undefined

Description: Certain bits of this register reset themselves to 0 uniquely via I2C writing (the value of the data written is unimportant, only the action of I2C writing).

[4] PRFVIT: Puncture Rate Found
1: puncture rate found
0: searching puncture rate (unsigned)

[3] LOCKEDVIT: Viterbi Locked
1: decoder locked
0: searching synchro word (unsigned)

VTHINUSE Viterbi threshold currently in use

7	6	5	4	3	2	1	0
VIT_INUSE							
R							

Address: 0xF53F

Type: R

Reset: Undefined

Description: Viterbi threshold currently in use

[7:0] VIT_INUSE: Actual Viterbi threshold in use (observation).
During acquisition this is controlled by VITSCALE:NVTH_NOSRANGE
After acquisition; PRFVIT:DIS_VTHLOCK (unsigned)

KDIV12 Gain (k_divider) of puncture rate 1/2

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_12						
R	R/W						

Address: 0xF540

Type: R/W

Reset: 0x27

Description: Gain (k_divider) of puncture rate 1/2

[6:0] K_DIVIDER_12: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_12 / 256 * |I or Q| (unsigned)

KDIV23 Gain (k_divider) of puncture rate 2/3

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_23						
R	R/W						

Address: 0xF541

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 2/3

[6:0] K_DIVIDER_23: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_23 / 256 * II or QI (unsigned)

KDIV34 Gain (k_divider) of puncture rate 3/4

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_34						
R	R/W						

Address: 0xF542

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 3/4

[6:0] K_DIVIDER_34: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_34 / 256 * II or QI (unsigned)

KDIV56 Gain (k_divider) of puncture rate 5/6

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_56						
R	R/W						

Address: 0xF543

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 5/6

[6:0] K_DIVIDER_56: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_56 / 256 * II or QI (unsigned)

KDIV67 Gain (k_divider) of puncture rate 6/7

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_67						
R	R/W						

Address: 0xF544

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 6/7

[6:0] K_DIVIDER_67: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_67 / 256 * II or QI (unsigned)

KDIV78 Gain (k_divider) of puncture rate 7/8

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_78						
R	R/W						

Address: 0xF545

Type: R/W

Reset: 0x50

Description: Gain (k_divider) of puncture rate 7/8

[6:0] K_DIVIDER_78: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_78 / 256 * II or QI (unsigned)

17.8 DVB2 register descriptions

PDELCTRL1 Packet delineator configuration

7	6	5	4	3	2	1	0
INV_MISMASK	RESERVED	FILTER_EN	RESERVED			EN_MIS00	ALGOSWRST
R/W	R	R/W	R			R/W	R/W

Address: 0xF550

Type: R/W

Reset: 0x0

Description: Packet delineator configuration

[7] INV_MISMASK: 1: inverse the MIS mask (unsigned)

[5] FILTER_EN: 1: activate the MIS filter if MATYPE.sis_mis = 0 (unsigned)

[1] EN_MIS00: when MIS = 00:
1: it is special and systematically accepted (system frame)
0: subjected to the usual MIS filter restrictions (if filter_en = 1). (unsigned)

[0] ALGOSWRST: 1: Packet Delineator reset (unsigned)

PDELCTRL2 Packet delineator additional configuration

7	6	5	4	3	2	1	0
RESERVED	RESET_UPKO_COUNT	RESERVED				FRAME_MODE	RESERVED
R	R/W	R				R/W	R

Address: 0xF551

Type: R/W

Reset: 0x0

Description: Packet delineator additional configuration

[6] RESET_UPKO_COUNT: Reset BBFCRCKO and UPCRCKO counters (unsigned)

[1] FRAME_MODE: 1: circuit configuration in frame mode.
0: circuit configuration in packet mode if the system is not (forced) in Generic Continuous Stream. (unsigned)

HYSTTHRESH pktdelin_lock signal hysteresis limits

7	6	5	4	3	2	1	0
UNLCK_THRESH				DELIN_LCK_THRESH			
R/W				R/W			

Address: 0xF554

Type: R/W

Reset: 0x41

Description: pktdelin_lock signal hysteresis limits

[7:4] UNLCK_THRESH: negative edge (unsigned)

[3:0] DELIN_LCK_THRESH: positive edge (unsigned)

ISIENTRY MIS mode selection filter

7	6	5	4	3	2	1	0
ISI_ENTRY							
R/W							

Address: 0xF55E

Type: R/W

Reset: 0x0

Description: The multiple input stream filter is available when the BBHeader MATYPE/SISMIS=0 and is activated when register field PDELCTRL1/filter_en=1. A set of masks permit the selection of frames with the correct MATYPE/ISI (the 8 bits LSB of MATYPE at the start of BBheader). The masking equation is the following:
test_MIS = MATYPE/ISI and ISIBITENA/isi_bit_en

The following depends on the polarity of register field PDELCTRL1/inv_mismask:

-inv_mismask=0: the frame is accepted if test_MIS = ISIENTRY/isi_entry

-inv_mismask=1: the frame is accepted if test_MIS /= ISIENTRY/isi_entry

The case MATYPE/ISI=0 could be considered as a special case if PDELCTRL1/en_mis00=1, this frame is always accepted regardless of the configuration of inv_mismask, isi_bit_en and isi_entry.

This frame can then be seen as a system frame which is always accepted, such as the channel descriptors and other telementry.

[7:0] ISI_ENTRY: (unsigned)

ISIBITENA MIS mode selection mask

7	6	5	4	3	2	1	0
ISI_BIT_EN							
R/W							

Address: 0xF55F

Type: R/W

Reset: 0x0

Description: See ISIENTRY.

[7:0] ISI_BIT_EN: (unsigned)

MATSTR1 MATYPE of the current frame

7	6	5	4	3	2	1	0
MATYPE_CURRENT[15:8]							
R							

Address: 0xF560

Type: R

Reset: Undefined

Description: MATYPE of the current frame

[7:0] MATYPE_CURRENT: (unsigned)

MATSTR0 MATYPE of the current frame

7	6	5	4	3	2	1	0
MATYPE_CURRENT[7:0]							
R							

Address: 0xF561

Type: R

Reset: Undefined

Description: MATYPE of the current frame

[7:0] MATYPE_CURRENT: (unsigned)

UPLSTR1 UPL of the current frame

7	6	5	4	3	2	1	0
UPL_CURRENT[15:8]							
R							

Address: 0xF562

Type: R

Reset: Undefined

Description: UPL of the current frame

[7:0] UPL_CURRENT: (unsigned)

UPLSTR0 UPL of the current frame

7	6	5	4	3	2	1	0
UPL_CURRENT[7:0]							
R							

Address: 0xF563

Type: R

Reset: Undefined

Description: UPL of the current frame

[7:0] UPL_CURRENT: (unsigned)

DFLSTR1 DFL of the current frame

7	6	5	4	3	2	1	0
DFL_CURRENT[15:8]							
R							

Address: 0xF564

Type: R

Reset: Undefined

Description: DFL of the current frame

[7:0] DFL_CURRENT: (unsigned)

DFLSTR0 DFL of the current frame

7	6	5	4	3	2	1	0
DFL_CURRENT[7:0]							
R							

Address: 0xF565

Type: R

Reset: Undefined

Description: DFL of the current frame

[7:0] DFL_CURRENT: (unsigned)

SYNCSTR SYNC of the current frame

7	6	5	4	3	2	1	0
SYNC_CURRENT							
R							

Address: 0xF566

Type: R

Reset: Undefined

Description: SYNC of the current frame

[7:0] SYNC_CURRENT: (unsigned)

SYNCDSTR1 SYNCD of the current frame

7	6	5	4	3	2	1	0
SYNCD_CURRENT[15:8]							
R							

Address: 0xF567

Type: R

Reset: Undefined

Description: SYNCD of the current frame

[7:0] SYNCD_CURRENT: (unsigned)

SYNCDSTR0 SYNCD of the current frame

7	6	5	4	3	2	1	0
SYNCD_CURRENT[7:0]							
R							

Address: 0xF568

Type: R

Reset: Undefined

Description: SYNCD of the current frame

[7:0] SYNCD_CURRENT: (unsigned)

PDELSTATUS1 Packet delineator status

7	6	5	4	3	2	1	0
PKTDELIN_DELOCK	SYNCDUPDFL_BADDFL	CONTINUOUS_STREAM	UNACCEPTED_STREAM	BCH_ERROR_FLAG	RESERVED	PKTDELIN_LOCK	FIRST_LOCK
R/W	R	R	R	R	R	R	R

Address: 0xF569

Type: R

Reset: Undefined

Description: Packet delineator status

[7] PKTDELIN_DELOCK: Detection of a 0 event on pktdelin_lock. Useful for debugging the origin of a signal fault
Reset by an I2C write (read put to 0 on a write,unsigned)

[6] SYNCDUPDFL_BADDFL: 1: error: DFL > DFL maximum possible for this MODCOD or SYNCD greater than DFL or UPL (and not 0xFFFF)
has happend since last reset
Reset by I2C read (read put to 0 on a read,unsigned)

[5] CONTINUOUS_STREAM: 1: the current frame is a Generic Continuous Stream (MATYPE/tsgs=01, UPL=0 and/or PDELCTRL2/force_continuous=1). (unsigned)

[4] UNACCEPTED_STREAM: 1: current frame refused (due to error or bad ISI) (read put to 0 on a read,unsigned)

[3] BCH_ERROR_FLAG: 1: a BCH error occurred in one of the previous frames.
Bit automatically reset to 0 after I2C reading. (read put to 0 on a read,unsigned)

[1] PKTDELIN_LOCK: 1: Packet Delineator locked (unsigned)

[0] FIRST_LOCK: 1: The Packet Delineator is locked and processing frames (functioning normally) (unsigned)

PDELSTATUS2 Additional status for packet delineator

7	6	5	4	3	2	1	0
RESERVED	FRAME_MODCOD					FRAME_TYPE	
R	R					R	

Address: 0xF56A

Type: R

Reset: Undefined

Description: Additional status for packet delineator

[6:2] FRAME_MODCOD: MODCOD of the current frame (unsigned)

[1:0] FRAME_TYPE: TYPE of the current frame (unsigned)

BBFCRCKO1 BBHeader KO counter

7	6	5	4	3	2	1	0
BBHCRC_KOCNT[15:8]							
R/W							

Address: 0xF56B

Type: R/W

Reset: 0x0

Description: BBHeader KO counter

[7:0] BBHCRC_KOCNT: number of false frames (CRC8 BBHeader false) since the last reinitialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

BBFCRCKO0 BBHeader KO counter

7	6	5	4	3	2	1	0
BBHCRC_KOCNT[7:0]							
R/W							

Address: 0xF56C

Type: R/W

Reset: 0x0

Description: BBHeader KO counter

[7:0] BBHCRC_KOCNT: number of false frames (CRC8 BBHeader false) since the last reinitialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

UPCRCKO1 Packet KO counter

7	6	5	4	3	2	1	0
PKTCRC_KOCNT[15:8]							
R/W							

Address: 0xF56D

Type: R/W

Reset: 0x0

Description: Packet KO counter

[7:0] PKTCRC_KOCNT: number of false packets (CRC8 packet false) since the last reinitialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

UPCRCKO0 Packet KO counter

7	6	5	4	3	2	1	0
PKTCRC_KOCNT[7:0]							
R/W							

Address: 0xF56E

Type: R/W

Reset: 0x0

Description: Packet KO counter

[7:0] PKTCRC_KOCNT: number of false packets (CRC8 packet false) since the last reinitialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

PDELCTRL3 Additional configuration of packet delineator

7	6	5	4	3	2	1	0
PKTDEL_CONTFAIL	RESERVED						
R/W	R						

Address: 0xF56F

Type: R/W

Reset: 0x0

Description: Additional configuration of packet delineator

[7] PKTDEL_CONTFAIL: Selection of LDPC power saving more in deep fade situations.
A count up-down accumulator is (with a floor of zero) used. If the thrshold is reached the function is engaged.
0: packet mode. If 64 packets are false then reject one frame in 2 without LDPC processing.
1: frame mode. If more than 64 frames false then reject one frame in 2 without LDPC processing. (unsigned)

NBITER_NFx Number of LDPC decoding iterations

	7	6	5	4	3	2	1	0
NBITER_NF4	NBITER_NF_QP_1_2							
NBITER_NF5	NBITER_NF_QP_3_5							
NBITER_NF6	NBITER_NF_QP_2_3							
NBITER_NF7	NBITER_NF_QP_3_4							
NBITER_NF8	NBITER_NF_QP_4_5							
NBITER_NF9	NBITER_NF_QP_5_6							
NBITER_NF10	NBITER_NF_QP_8_9							
NBITER_NF11	NBITER_NF_QP_9_10							
NBITER_NF12	NBITER_NF_8P_3_5							
NBITER_NF13	NBITER_NF_8P_2_3							
NBITER_NF14	NBITER_NF_8P_3_4							
NBITER_NF15	NBITER_NF_8P_5_6							
NBITER_NF16	NBITER_NF_8P_8_9							
NBITER_NF17	NBITER_NF_8P_9_10							
	R/W							

Address: 0xFA03 + (x-4) * 0x1 (x=4 to 17)

Type: R/W

Reset: 0x37, 0x29, 0x37, 0x33, 0x31, 0x2F, 0x39, 0x3A, 0x29, 0x37, 0x33, 0x2F, 0x39, 0x3A

Description: NbIter_NFn -> number of normal frame iterations for MODCOD n.

NBITER_NF4: [7:0] NBITER_NF_QP_1_2: (unsigned)

NBITER_NF5: [7:0] NBITER_NF_QP_3_5: (unsigned)

NBITER_NF6: [7:0] NBITER_NF_QP_2_3: (unsigned)

NBITER_NF7: [7:0] NBITER_NF_QP_3_4: (unsigned)

NBITER_NF8: [7:0] NBITER_NF_QP_4_5: (unsigned)

NBITER_NF9: [7:0] NBITER_NF_QP_5_6: (unsigned)

NBITER_NF10: [7:0] NBITER_NF_QP_8_9: (unsigned)

NBITER_NF11: [7:0] NBITER_NF_QP_9_10: (unsigned)

NBITER_NF12: [7:0] NBITER_NF_8P_3_5: (unsigned)

NBITER_NF13: [7:0] NBITER_NF_8P_2_3: (unsigned)

NBITER_NF14: [7:0] NBITER_NF_8P_3_4: (unsigned)

NBITER_NF15: [7:0] NBITER_NF_8P_5_6: (unsigned)

NBITER_NF16: [7:0] NBITER_NF_8P_8_9: (unsigned)

NBITER_NF17: [7:0] NBITER_NF_8P_9_10: (unsigned)

NBITERNOERR LDPC decoding iteration stop criterion

7	6	5	4	3	2	1	0
RESERVED				NBITER_STOP_CRIT			
R				R/W			

Address: 0xFA3F

Type: R/W

Reset: 0x4

Description: LDPC decoding iteration stop criterion

[3:0] NBITER_STOP_CRIT: This 4-bit value gives the number of iterations for which the decoding result is correlated to determine whether the LDPC decoder has converged or not. If the value is 0, there is no decoding stop process and the decoder performs the default iteration number given by the register NbIter_xx (unsigned)

GAINLLR_NFx — LDPC input LLR gain

	7	6	5	4	3	2	1	0
GAINLLR_NF4	RESERVED	GAINLLR_NF_QP_1_2						
GAINLLR_NF5	RESERVED	GAINLLR_NF_QP_3_5						
GAINLLR_NF6	RESERVED	GAINLLR_NF_QP_2_3						
GAINLLR_NF7	RESERVED	GAINLLR_NF_QP_3_4						
GAINLLR_NF8	RESERVED	GAINLLR_NF_QP_4_5						
GAINLLR_NF9	RESERVED	GAINLLR_NF_QP_5_6						
GAINLLR_NF10	RESERVED	GAINLLR_NF_QP_8_9						
GAINLLR_NF11	RESERVED	GAINLLR_NF_QP_9_10						
GAINLLR_NF12	RESERVED	GAINLLR_NF_8P_3_5						
GAINLLR_NF13	RESERVED	GAINLLR_NF_8P_2_3						
GAINLLR_NF14	RESERVED	GAINLLR_NF_8P_3_4						
GAINLLR_NF15	RESERVED	GAINLLR_NF_8P_5_6						
GAINLLR_NF16	RESERVED	GAINLLR_NF_8P_8_9						
GAINLLR_NF17	RESERVED	GAINLLR_NF_8P_9_10						
	R	R/W						

Address: 0xFA43 + (x-4) * 0x1 (x=4 to 17)

Type: R/W

Reset: 0x20

Description: GainLLR_NFn -> normal frame LLR gain for MODCOD n.

GAINLLR_NF4: [6:0] GAINLLR_NF_QP_1_2: (unsigned)

GAINLLR_NF5: [6:0] GAINLLR_NF_QP_3_5: (unsigned)

GAINLLR_NF6: [6:0] GAINLLR_NF_QP_2_3: (unsigned)

GAINLLR_NF7: [6:0] GAINLLR_NF_QP_3_4: (unsigned)

GAINLLR_NF8: [6:0] GAINLLR_NF_QP_4_5: (unsigned)

GAINLLR_NF9: [6:0] GAINLLR_NF_QP_5_6: (unsigned)

GAINLLR_NF10: [6:0] GAINLLR_NF_QP_8_9: (unsigned)

GAINLLR_NF11: [6:0] GAINLLR_NF_QP_9_10: (unsigned)

GAINLLR_NF12: [6:0] GAINLLR_NF_8P_3_5: (unsigned)

GAINLLR_NF13: [6:0] GAINLLR_NF_8P_2_3: (unsigned)

GAINLLR_NF14: [6:0] GAINLLR_NF_8P_3_4: (unsigned)

GAINLLR_NF15: [6:0] GAINLLR_NF_8P_5_6: (unsigned)

GAINLLR_NF16: [6:0] GAINLLR_NF_8P_8_9: (unsigned)

GAINLLR_NF17: [6:0] GAINLLR_NF_8P_9_10: (unsigned)

CFGEXT External data stream configuration

7	6	5	4	3	2	1	0
STAGMODE	BYPBCH	BYPLDPC	LDPCMODE	INVLLRSIGN	SHORTMULT	RESERVED	EXTERNTX
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Address: 0xFA80

Type: R/W

Reset: 0x1

Description: External data stream configuration

[7] STAGMODE: 1: staggered mode, the scheduling of the LDPC decoding process is modified. It allows a faster convergence.

CodeRate	NbcycleiterNF	NbcycleinitNF	NbcycleiterSF	NbcycleinitSF
1/4	906 (911)	568	255	162
1/3	1054	630	289	180
2/5	1162	676	307 (316)	190
1/2	1149	654	264 (269)	160
3/5	1504	820	397	226
2/3	1138	628	297 (314)	178
3/4	1208 (1233)	658	281 (272)	160
4/5	1268	674	254 (256)	142
5/6	1303	688	287 (294)	164
8/9	1080	560	258 (310)	154
9/10	1073	560	na	na (unsigned)

[6] BYPBCH: 1: bypass BCH, the BCH correction is not done, is not applied on the output data. Thus the global latency is respected -> fully transparent on the flow (unsigned)

[5] BYPLDPC: 1: bypass LDPC, the LDPC decoder is OFF. Only the initialization phase is done. Thus the hard decision is done on the LLR sign (unsigned)

[4] LDPCMODE: 1: LDPC debug mode, Nldpc (64800 or 16200) bits will be delivered, all enabled with bch_data_en and bch_data_par_en. BCH correction is NOT applied.
0: normal mode, Nbch (see coderates) bits are delivered, all enabled by bch_data_par_en. And only the first Kbch bits are also enabled with bch_data_en. BCH correction is of course done. (unsigned)

[3] INVLLRSIGN: 1: inverts the sign of input data. It corresponds to the LLR definition: either Ln(P0/P1) or Ln(P1/P0). (unsigned)

[2] SHORTMULT: 1: allows to bypass the input LLRs gain (unsigned)

[0] EXTERNTX: 0: DVBS2_FEC sub-block is used in autotest/internal mode
1: external (functional) mode. Data coming from the demodulator (unsigned)

GENCFG General configuration

7	6	5	4	3	2	1	0
RESERVED			BROADCAST	RESERVED			DDEMOD
R			R/W	R			R/W

Address: 0xFA86

Type: R/W

Reset: 0xC

Description: General configuration

[4] BROADCAST: 1: “Broadcast Mode“, decoding of frame n starts when the start-of-frame of (SOF) frame n+1 is received. Thus, as long as there is no new frame on the LDPC input, there is a frame stored in RAM, waiting for a decoding start. Invalid frames are detected and NOT processed.

0: “ASAP mode“, decoding of frame n starts when enough data (64800 or 16200) is received and when the LDPC decoder is ready to process data. Invalid frames are not detected. (unsigned)

[0] DDEMOD: 1: dual demodulation mode. The two input streams are processed

0: single demodulation mode. Only the priority input stream is processed (unsigned)

LDPCERRx LDPC error counter

	7	6	5	4	3	2	1	0
LDPCERR1	LDPC_ERRORS_COUNTER[15:8]							
LDPCERR0	LDPC_ERRORS_COUNTER[7:0]							
	R							

Address: 0xFA96(x=1), 0xFA97(x=0)

Type: R

Reset: 0x0

Description: LDPC error counter

[7:0] LDPC_ERRORS_COUNTER: counter value = number of errors corrected by the LDPC decoder on the current output frame (unsigned)

BCHERR BCH error

7	6	5	4	3	2	1	0
RESERVED			ERRORFLAG	BCH_ERRORS_COUNTER			
R			R	R			

Address: 0xFA98

Type: R

Reset: 0x0

Description: BCH error

[4] ERRORFLAG: Comparison flag between the bch_errors_counter value and the corrected error number. If the GENCFG.2 bit is set to 1, the flag is valid for the current frame but available when the last output byte, otherwise, it is valid for the previous frame. (unsigned)

[3:0] BCH_ERRORS_COUNTER: BCH error number location polynomial degree for the current output frame.
Max values are 0xA = d10 for 2/3 and 5/6 coderates, 0x8 = d8 for 8/9 and 9/10 coderates, 0xC = d12 for all others (unsigned)

17.9 TS register descriptions

TSSTATEM Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSDIL_ON	RESERVED	TSRS_ON	TSDESCRAMB_ON	TSFRAME_MODE	TS_DISABLE	RESERVED	TSOUT_NOSYNC
R/W	R	R/W	R/W	R/W	R/W	R	R/W

Address: 0xF570

Type: R/W

Reset: 0xF0

Description: Configuration of merger-hardware stream line 1

[7] TSDIL_ON: use of deinterleaver (active in DVBS1 and Legacy DTV only):
1: deinterleaver active if authorized.
0: inactive. (unsigned)

[5] TSRS_ON: use of Reed-Solomon decoder (active in DVBS1 and Legacy DTV only) if tsskiprs_on = 0:
1: decode and correct the data flow
0: decode but do not correct (unsigned)

[4] TSDESCRAMB_ON: use of descrambler (active in DVBS1 only) if tsskiprs_on=0 and if TSSTATUS2/scrambdetect=1 (scrambling type DVBS1 has been detected):
1: descramble the data flow
0: do not descramble (even if scrambling is detected) (unsigned)

[3] TSFRAME_MODE: (read only)
1: data flow in frame mode
0: data flow in packet mode (unsigned)

[2] TS_DISABLE: disable line
1: the line is stopped, nothing outputs.
0: normal function (unsigned)

[0] TSOUT_NOSYNC: output controls
In packet modes ISSYI, NPD:
1: hysteresis mode authortized at power up
0: immediate output of all ready packets or frames
Other modes (packet or frame):
1: integrated circuit latency regulation
0: immediate output of all ready packets or frames (unsigned)

TSCFGH Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_DVBCI	TSFIFO_SERIAL	TSFIFO_TEIUPDATE	TSFIFO_DUTY50	TSFIFO_HSGNLOUT	TSFIFO_ERRMODE		RST_HWARE
R/W	R/W	R/W	R/W	R/W	R/W		R/W

Address: 0xF572

Type: R/W

Reset: 0x0

Description: Configuration of merger-hardware stream line 1

[7] TSFIFO_DVBCI: treatment of the signals CLKOUT and Data/Parity
1: mode DVB-CI: CLKOUT continuous, D/P indicates the data pulses
0: normal mode: a CLKOUT pulse with each data, CLKOUT off if no data, D/P remains punctured
In order to avoid a “hole“ on D/P, there are 3 equivalent solutions:
-do not connect it
-program TSCFGL/tsfifo_dpunact = 1
-deprogram the associated GPIO (unsigned)

[6] TSFIFO_SERIAL: 1: serial output: note the restriction to 135 Mbit/s.
0: parallel output, up to 270 Mbit/s. (unsigned)

[5] TSFIFO_TEIUPDATE: MPEG packets only (TSSTATEL/tsdss_packet=0)
1: update of TEI bit in accordance with the output ERROR signal. (unsigned)

[4] TSFIFO_DUTY50: CLKOUT signal duty cycle:
1: guarantees 50% but causes larger granularity on the available frequencies.
0: maximum granularity on the available frequences, but duty cycle not guaranteed (though always as close as possile to 50%). (unsigned)

[3] TSFIFO_HSGNLOUT: Header signalling
1: output the 16 byte Header Signaling.
0: no header output. (unsigned)

[2:1] TSFIFO_ERRMODE: treatment of ERROR signal:
00: ERROR label the packets or frames in error.
01: ERROR = 0
The false packets or frames are deleted before being output.
10: ERROR = start of frame byte indicator (packet mode)
ERROR = start of packet byte indicator (frame mode)
The false packets or frames are deleted before being output.
11: ERROR = reference start of frame of the latency regulation.
The false packets or frames are deleted before being output. (unsigned)

[0] RST_HWARE: 1: reset of Merger/HWare Stream line 1. (unsigned)

TSCFGM Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_MANSPEED		TSFIFO_PERMDATA	RESERVED			TSFIFO_DPUNACT	TSFIFO_INVDATA
R/W		R/W	R			R/W	R/W

Address: 0xF573

Type: R/W

Reset: 0x0

Description: Configuration of merger-hardware stream line 1

[7:6] TSFIFO_MANSPEED: CLKOUT frequency processing:
00: automatic calculation
01: automatic calculation while progressively keeping only the highest frequency (for ACM).
10: automatic calculation of the instantaneous frequency without memorizing the highest frequency found.
11: manual (unsigned)

[5] TSFIFO_PERMDATA: (active in serial and parallel)
1: switch DATA7<->DATA0 (unsigned)

[1] TSFIFO_DPUNACT: 1: disactivate D/P (unsigned)

[0] TSFIFO_INVDATA: 1: inverse DATA7..0 (unsigned)

TSCFGL Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_BCLKDEL1CK		BCHERROR_MODE		TSFIFO_NSGNL2DATA	TSFIFO_EMBINDVB	TSFIFO_BITSPEED	
R/W		R/W		R/W	R/W	R/W	

Address: 0xF574

Type: R/W

Reset: 0x20

Description: Configuration of merger-hardware stream line 1

[7:6] TSFIFO_BCLKDEL1CK: 270 MHz delay cycle on CLKOUT with respect to other signals (STROUT, D/P, ERROR, DATA7..0)
00: (0) no delay
01: (+1) advance by one 270 MHz cycle
11: (-1) move back by one 270 MHz cycle
10: (-2) -- (unsigned)

[5:4] BCHERROR_MODE: error packet construction
DVBS1/Legacy DTV (Reed-Solomon active):
00: RSerror
01: RSerror(+BBHeader)
10: RSerror (defaut)
11: RSerror(+BBHeader+BCHerror)
(Disable RSerror by TSSTATEM/tsrs_on=0)
DVBS2 Packet mode:
00: nothing
01: CRC8pkt+BBHeader
10: CRC8pkt (default)
11: (CRC8pkt+BBHeader+)BCHerror
DVB-S2 frame mode:
00: BBHeader +CRC8pkt if frame is packetised
01: BBHeader
10: BBHeader (default)
+CRC8pkt if frame is packetised
+BCHerror if generic stream
11: (CRC8pkt+BBHeader+)BCHerror
Note in Generic Continuous Stream, CRC8pkt does not exist. (unsigned)

[3] TSFIFO_NSGNL2DATA: 1: D/P=0 during Signaling Header and Footer
0: D/P=1 during Signaling Header and Footer (unsigned)

[2] TSFIFO_EMBINDVB: 1: load the short packets (Legacy DTV) in an MPEG packet (unsigned)

[1:0] TSFIFO_BITSPEED: Method of calculation of the bit rate, generating the packet rate and the frequency of the output clock, CLKOUT (TSSPEED/tsfifo_outspeed). The result may be read in the register TSBITRATE.
00: automatic mode (default).
- In broadcast mode (CCM and VCM) (set by ACM bit in MATYPE) bit rate calculated using 0b10 below (note: not valid when using MIS).
- For modes when NPD, ACM or MIS is selected. See 0b11 below.
01: Manual mode. The value written in TSBITRATE is the value used to calculate the packet rate and CLKOUT.
10: Symbol rate mode: Output clock rate (bit rate) is calculated from symbol rate and MODCOD using the table 13 in EN302307v1.1.1. The results are not smoothed (change with DFL, PLFRAME length of each frame) but are perfectly exact in the space of a frame.
11: Pragmatic smoothing mode: The TSBITRATE is calculated from the long term average of bits leaving the packet delineator. The incoming frames must arrive regularly for this mode to work effectively. The register TSDLYSET/soffifo_offset is used to define the mid-point load on the TS FIFO. (unsigned)

TSINSDELH Insertion/deletion mask of output packet parts

7	6	5	4	3	2	1	0
TSDEL_SYNCBYTE	TSDEL_XXHEADER	TSDEL_BBHEADER	TSDEL_DATAFIELD	TSINSDEL_ISCR	TSINSDEL_NPD	TSINSDEL_RSPARITY	TSINSDEL_CRC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF576

Type: R/W

Reset: 0x0

Description: Insertion/deletion mask of output packet parts

[7] TSDEL_SYNCBYTE: (1 byte) deletion of synchro word. (unsigned)

[6] TSDEL_XXHEADER: (3 bytes) deletion of Packet Header. (unsigned)

[5] TSDEL_BBHEADER: frame mode only (10 bytes), deletion of BBHeader (unsigned)

[4] TSDEL_DATAFIELD: deletion of the payload
Generic Continuous Stream: entire DATAFIELD
packet mode: packet payload
frame mode: packet payload (unsigned)

[3] TSINSDEL_ISCR: (2 or 3 bytes according to TSBUFSTAT2/tsiscr_3bytes) output/deletion of ISCR field (if present). (unsigned)

[2] TSINSDEL_NPD: (1 byte) output/deletion of NPD byte (if present). (unsigned)

[1] TSINSDEL_RSPARITY: more specific to DVBS1/Legacy DTV (16 bytes), output/deletion of the Reed-Solomon part (if present). (unsigned)

[0] TSINSDEL_CRC8: (1 byte) output/deletion of CRC8 packet. (unsigned)

TSDIVN Output frequency control

7	6	5	4	3	2	1	0
TSFIFO_SPEEDMODE		RESERVED					
R/W		R					

Address: 0xF579

Type: R/W

Reset: 0x3

Description: Output frequency control

[7:6] TSFIFO_SPEEDMODE: Transport stream output speed mode contol
00: Classical mode
- Parallel: Fclkout = 4*Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 12 (Fclkout < Mclk/3)
- Serial: Fclkout = 32*Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 32 (Fclkout < Mclk)
01: Mantissa-Exponent mode.
- Parallel: Fclkout = 4*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
- Serial: Fclkout = 32*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
10: divide by 32 mode:
- Parallel: Fclkout = Mclk / 8*tsfifo_outspeed. Limited totsfifo_outspeed >= 4 (Fclkout < Mclk/32)
- Serial: Fclkout = Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/4)
11: -- (unsigned)

TSCFG4 Stream merger line 1 hardware configuration

7	6	5	4	3	2	1	0
TSFIFO_TSSPEEDMODE		RESERVED					
R/W		R					

Address: 0xF57A

Type: R/W

Reset: 0x0

Description: Stream merger line 1 hardware configuration

[7:6] TSFIFO_TSSPEEDMODE: Method of calculating TSSPEED/tsfifo_outspeed:
11: “instantaneous“ mode, tsfifo_outspeed is the instantaneous value of the bit or byte currently running. This is appropriate for variable rate streams (e.g ACM with the output of all MODCODS and latency regulation turned off)
10: “Smoothed“ mode, tsfifo_outspeed is smoothed (temporal averaging) over a large number of frames.
Ideal for CCM modes and where smoothing is useful (NPD, ISSYI).
00: “automatic“ mode, selects the best mode.
“smoothed“ mode when: CCM, NPD and or ISSYI, MIS;
“instantaneous“ mode when: ACM non NPD, ISSYI or MIS, latency regulation is off (TSSTATEM/tsout_nosync=1), external packet/frame synchronisation (TSSYNC/tsfifo_syncmode=10) mode, frame output mode or Generic Stream mode.
01: -- (unsigned)

TSSPEED CLKOUT frequency

7	6	5	4	3	2	1	0
TSFIFO_OUTSPEED							
R/W							

Address: 0xF580

Type: R/W

Reset: Undefined

Description: See the field TSDIVN/tsfifo_speedmode for TSSPEED calculation mode.
See the field TSCFG4/tsfifo_tsspeedmode for TSSPEED update mode.

[7:0] TSFIFO_OUTSPEED: stream output frequency.
There are three modes for calculating outspeed depending on the configuration of TSDIVN/tsfifo_speedmode.
00: Legacy calculation mode:
Parallel: Fclkout = 4*Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 12 (Fclkout < Mclk/3)
Serial: Fclkout = 32*Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 32 (Fclkout < Mclk)
01: mantissa+exponant mode (internal value on 19 bits):
Parallel: Fclkout = 4*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
Serial: Fclkout = 32*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
10: division by 32 of the output speed.
Parallel: Fclkout = Mclk / 8*tsfifo_outspeed
Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/32)
Serial: Fclkout = Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/4)
11: -- (unsigned)

TSSTATUS — Merger-hardware stream status

7	6	5	4	3	2	1	0
TSFIFO_LINEOK	TSFIFO_ERROR	RESERVED					DIL_READY
R	R	R					R

Address: 0xF581

Type: R

Reset: Undefined

Description: Merger-hardware stream status

[7] TSFIFO_LINEOK: inverse of the ERROR signal:
1: the ERROR signal is currently at 0
-> no packets with errors at the moment
-> line OK (unsigned)

[6] TSFIFO_ERROR: stored value of the ERROR signal
1: a packet in error has passed since the last I2C reading of TSSTATUS.
Automatically reset to 0 after an I2C read (read put to 0 on a read,unsigned)

[0] DIL_READY: 1: the output FIFO contains data
0: it is empty or does not contain enough data (unsigned)

TSSTATUS2 Additional status of merger-hardware stream

7	6	5	4	3	2	1	0
TSFIFO_DEMODSEL	TSFIFOSPEED_STORE	DILXX_RESET	TSSERIAL_IMPOS	RESERVED		SCRAMBDETECT	RESERVED
R/W	R/W	R/W	R/W	R		R/W	R

Address: 0xF582

Type: R/W

Reset: Undefined

Description: Additional status of merger-hardware stream

[7] TSFIFO_DEMODSEL: signal source:
1: demodulator 2
0: demodulator 1 (unsigned)

[6] TSFIFOSPEED_STORE: 1: a CLKOUT speed change event (TSSPEED.tsfifo_outspeed) has occurred.
Reset to 0 by an I2C write (read put to 0 on a write,unsigned)

[5] DILXX_RESET: 1: a FIFO or deinterleaver DVBS1 reset has occurred. There was a break in the data flow.
Reset to 0 by an I2C write (read put to 0 on a write,unsigned)

[4] TSSERIAL_IMPOS: 1: throughput too high for a serial transmission (unsigned)

[1] SCRAMBDETECT: in DVBS1 only
1: detection (stable) of inverse synchro word, indicating the presence of DVBS1 scrambling. (unsigned)

TSBITRATE1 Observation of raw bit rate

7	6	5	4	3	2	1	0
TSFIFO_BITRATE[15:8]							
R/W							

Address: 0xF583

Type: R/W

Reset: Undefined

Description: Observation of raw bit rate

[7:0] TSFIFO_BITRATE: Bit rate = Mclk * tsfifo_bitrate / 16384
It is possible to write in this register to reinitialize the bit rate calculation. (unsigned)

TSBITRATE0 Observation of raw bit rate

7	6	5	4	3	2	1	0
TSFIFO_BITRATE[7:0]							
R/W							

Address: 0xF584

Type: R/W

Reset: Undefined

Description: Observation of raw bit rate

[7:0] TSFIFO_BITRATE: Bit rate = Mclk * tsfifo_bitrate / 16384
It is possible to write in this register to reinitialize the bit rate calculation. (unsigned)

ERRCTRL1 Configuration of error counter 1

7	6	5	4	3	2	1	0
ERR_SOURCE1				RESERVED	NUM_EVENT1		
R/W				R	R/W		

Address: 0xF598

Type: R/W

Reset: 0x35

Description: Configuration of error counter 1

[7:4] ERR_SOURCE1: measurement unit (byte, packet, frame..), decimal point location, measurement point by mode (S1 or S2)
example: for option 0000, measurement unit is in bytes, the measurement value = Reg_value/ 2^19 and this option measures DVBS1 demod errors only.
0000: byte 19 Demod bit errors (S1)
0001: frame 7 ldpc_errnbr (S2), LDPC errors
frame 15 regerr (S1), Viterbi errors
0010: frame 19 bch_errnbr (S2), BCH errors
byte 23 Viterbi (ReedSolo) bit error (S1)
0011: frame 23 bch_error_flag (S2)
packet 23 Viterbi (ReedSolo) byte error (S1)
0100: Mck / 4K 23 Frame Rate LDPC
0101: frame 23 bbheader_error (S2)
byte 23 Viterbi (ReedSolo) bit error ~BER (S1)
0110: packet 23 CRC-8 packet (S2)
byte 23 Viterbi (ReedSolo) byte error ~BER (S1)
0111: byte 23 Viterbi (ReedSolo) bit error BER (S1)
1000: byte 23 Viterbi (ReedSolo) byte error BER (S1)
1001: packet 23 Viterbi (ReedSolo) packet error (S1)
1010: packet 19 Viterbi (ReedSolo) packet error nbr (S1)
1011: frame 23 bad_dfl+syncd_up_dfl (S2)
1100: packet 23 TS error count, packet error final
1101: Mck/4K 7 TS FIFO
1110: frame 7 DFL
1111: Mck/512 23 Packet Rate
Notes:
- (S2): only in DVBS2; (S1): only in DVBS1/Legacy DTV
-errcpt_size: counting unit
-byte: bytes
-packet: packets
-frame: frames
-Mck/512: Master clock/512
-Mck/4K: Master clock/4096 (unsigned) (unsigned)

[2:0] NUM_EVENT1: time constant
000: count mode (WITH reset of counter upon reading)
001: count mode (WITHOUT reset of counter upon reading)
The reset to 0 is achieved by writing (any value)
in any of the 3 bytes of ERRCNT12/11/10.
byte packet frame
010: 2^14 2^8 2^4
011: 2^16 2^10 2^6 | rate modes
100: 2^18 2^12 2^8 |
101: 2^20 2^14 2^10 |
110: 2^22 2^16 2^12 /
111: ---- average mode --- (unsigned)

ERRCNT12 Result of error counter 1

7	6	5	4	3	2	1	0
ERRCNT1_OLDVALUE	ERR_CNT1[22:16]						
R	R/W						

Address: 0xF599

Type: R/W

Reset: Undefined

Description: Result of error counter 1

[7] ERRCNT1_OLDVALUE: validity of the information read
1: this value is old and has already been read by I2C. Do not use it.
0: new value (read put to 0 on a read,unsigned)

[6:0] ERR_CNT1: result of counting (read put to 0 on a write,unsigned)

ERRCNT11 Result of error counter 1

7	6	5	4	3	2	1	0
ERR_CNT1[15:8]							
R/W							

Address: 0xF59A

Type: R/W

Reset: Undefined

Description: Result of error counter 1

[7:0] ERR_CNT1: result of counting (read put to 0 on a write,unsigned)

ERRCNT10 Result of error counter 1

7	6	5	4	3	2	1	0
ERR_CNT1[7:0]							
R/W							

Address: 0xF59B

Type: R/W

Reset: Undefined

Description: Result of error counter 1

[7:0] ERR_CNT1: result of counting (read put to 0 on a write,unsigned)

ERRCTRL2 Configuration of error counter 2

7	6	5	4	3	2	1	0
ERR_SOURCE2				RESERVED	NUM_EVENT2		
R/W				R	R/W		

Address: 0xF59C

Type: R/W

Reset: 0xC1

Description: Configuration of error counter 2

[7:4] ERR_SOURCE2: measuring point (unsigned)

[2:0] NUM_EVENT2: time constant (unsigned)

ERRCNT22 Result of error counter 2

7	6	5	4	3	2	1	0
ERRCNT2_OLDVALUE	ERR_CNT2[22:16]						
R	R/W						

Address: 0xF59D

Type: R/W

Reset: Undefined

Description: Result of error counter 2

[7] ERRCNT2_OLDVALUE: validity of the information read (read put to 0 on a read,unsigned)

[6:0] ERR_CNT2: result of counting (read put to 0 on a write,unsigned)

ERRCNT21 Result of error counter 2

7	6	5	4	3	2	1	0
ERR_CNT2[15:8]							
R/W							

Address: 0xF59E

Type: R/W

Reset: Undefined

Description: Result of error counter 2

[7:0] ERR_CNT2: result of counting (read put to 0 on a write,unsigned)

ERRCNT20 Result of error counter 2

7	6	5	4	3	2	1	0
ERR_CNT2[7:0]							
R/W							

Address: 0xF59F

Type: R/W

Reset: Undefined

Description: Result of error counter 2

[7:0] ERR_CNT2: result of counting (read put to 0 on a write,unsigned)

FECSPY FEC spy configuration

7	6	5	4	3	2	1	0
SPY_ENABLE	NO_SYNCBYTE	SERIAL_MODE	UNUSUAL_PACKET	BERMETER_DATAMODE	RESERVED	BERMETER_LMODE	BERMETER_RESET
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Address: 0xF5A0

Type: R/W

Reset: 0x80

Description: FEC spy configuration

[7] SPY_ENABLE: operational state of the spy
1: functioning
0: stopped/reset
To completely reset the spy, simply write a 0 on this bit. (unsigned)

[6] NO_SYNCBYTE: (read only)
1: no synchro word in the data flow (DVBS2 only). (unsigned)

[5] SERIAL_MODE: (read only)
1: serial flow
0: parallel flow (unsigned)

[4] UNUSUAL_PACKET: (read only)
1: non-MPEG and non-Legacy DTV packet mode (the packet length is no longer verified, and the synchro word, if present, is no longer verified).
0: MPEG or Legacy DTV packet mode (packet length and synchro word verified). (unsigned)

[3] BERMETER_DATAMODE: bermeter_datamode
0: bit error rate
1: packet error rate (unsigned)

[1] BERMETER_LMODE: 1: BER/PER long mode (fbermeter_cpt measured over 2^48 bytes)
0: BER/PER normal mode (fbermeter_cpt measured over 2^40 bytes) (unsigned)

[0] BERMETER_RESET: stop/reset of BER/PER only (not of FEC Spy)
1: freeze the BER/PER Meter.
A return to 0 will provoke a reset of the BER/PER meter.
0: the BER/PER is running (if spy_enable=1) (unsigned)

FSPYCFG FEC spy configuration

7	6	5	4	3	2	1	0
FECSPY_INPUT		RST_ON_ERROR	ONE_SHOT	I2C_MODE		SPY_HYSTERESIS	
R/W		R/W	R/W	R/W		R/W	

Address: 0xF5A1

Type: R/W

Reset: 0x2C

Description: FEC spy configuration

[7:6] FECSPY_INPUT: measured signal source
00: output of line 1
01: debug, FIFO 1 output or Reed-Solomon decoder line 1 according to TSTTS/tstts_fspybefrs bit (DVBS1/Legacy DTV only).
10: debug, Viterbi decoder 1 output
11: Return Channel Line output (unsigned)

[5] RST_ON_ERROR: impact of an error detection
1: The FEC Spy searches a number of adjoining good packets.
0: The FEC Spy will give the global number of good packets. To obtain a ratio of good packets. (unsigned)

[4] ONE_SHOT: 1: stop once the operation is finished. Relaunch the FEC Spy by a positive edge on FECSPY.spy_enable.
0: the FEC Spy continuously restarts the test once finished. (unsigned)

[3:2] I2C_MODE: FEC Spy general function mode
00: reserved.
01: reserved.
10: reserved.
11: BER/PER Meter mode. FPACKCNT.fpacket_counter contains the previous result. The output signals represent the previous result. The BER/PER Meter is master of FEC Spy synchro. (unsigned)

[1:0] SPY_HYSTERESIS: number of packets measured for each test session
00: a test lasts 255 packets (maximum). FSTATUS/valid_sim=1 after 128 good packets.
01: a test lasts 511 packets (maximum). FSTATUS/valid_sim=1 after 255 good packets.
WARNING: consider saturation on the GOODPACK and PACKCNT registers.
10: a test lasts 63 packets (maximum). FSTATUS/valid_sim=1 after 32 good packets.
11: a test lasts 127 packets (maximum). FSTATUS/valid_sim=1 after 64 good packets.
(unsigned)

FSPYDATA Tested packet contents

7	6	5	4	3	2	1	0
SPY_STUFFING	RESERVED	SPY_CNULLPKT	SPY_OUTDATA_MODE				
R/W	R	R/W	R/W				

Address: 0xF5A2

Type: R/W

Reset: 0x3A

Description: Tested packet contents.

[7] SPY_STUFFING: 1: indicate the possible presence of stuffing packets to the FEC Spy. They will be specifically analyzed as stuffing packets.
0: all packets must be analyzed in the same way. (unsigned)

[5] SPY_CNULLPKT: presence of Packet Header
1: Null TS Packet mode,
1 synchro word:
DVB: 47
DirecTV: 1D
3 Packet Header bytes:
DVB: 1F,FE/FF,10
DirecTV: A0/20,00/01,04
184 payload bytes for an MPEG packet.
127 payload bytes for a Legacy DTV packet.
0: Non TS Packet mode
1 synchro word
DVB: 47
DirecTV: 1D
187 payload bytes for an MPEG packet.
130 payload bytes for a Legacy DTV packet. (unsigned)

[4:0] SPY_OUTDATA_MODE: form and type of data that the spy must expect to confirm:
43.210
00.000: no content verification, simply the form
00.001: Legacy DTV: auto increment, DVB (+others):auto decrement
00.010: auto increment, rising
00.011: auto decrement, falling
00.1xx: Toggling data:
00.100: 55/AA
00.101: 66/99
00.110: C3/3C
00.111: 00/FF
01.xxx: (Pseudo) Constants:
01.000: 00
01.001: 1 byte non null (value 0x01) every 256.
01.010: 55
01.011: 66
01.100: 99
01.101: AA
01.110: Legacy DTV null packet (the official DTV stuffing packet).
01.111: FF (the official MEPG stuffing packet).
1x.xxx: PRBS modes:
10.000 6: X^6 + X^5 + 1 Validated on BER Meter
10.001 7: X^7 + X^6 + 1 Unknown on BER Meter
10.010 9: X^9 + X^5 + 1 Validated on BER Meter
10.011 10: X^10 + X^7 + 1 Unknown on BER Meter
10.100 11: X^11 + X^9 + 1 Validated on BER Meter
10.101 15: X^15 + X^14 + 1 NON Validated on BER Meter
10.110 15: X^15 + X^14 Validated on BER Meter
10.111 17: X^17 + X^14 + 1 Validated on BER Meter
11.000 20: X^20 + X^17 + 1 Validated on BER Meter
11.001 23: X^23 + X^18 + 1 NON Validated on BER Meter
11.010 23: X^23 + X^18 Validated on BER Meter
11.011 31: X^31 + X^28 + 1 Unknown on BER Meter
11.100 41: X^41 + X^3 + 1
11.101 49: X^49 + x^9 + 1
11.110 --
11.111 -- (unsigned)

FSPYOUT FEC spy miscellaneous configuration

7	6	5	4	3	2	1	0
FSPY_DIRECT	RESERVED					STUFF_MODE	
R/W	R					R/W	

Address: 0xF5A3

Type: R/W

Reset: 0x7

Description: FEC spy miscellaneous configuration

[7] FSPY_DIRECT: 1: raw output flow test (without the SGNL[1:0] pins). The signaling bytes (if present) may cause test failure.
0: provide the signaling indications to the FEC Spy. The signaling bytes (if present) will be removed from the test. (unsigned)

[2:0] STUFF_MODE: payload description of a stuffing packet:
000: 0x00
001: DirecTV:auto increment, DVB (+others): auto decrement
010: (test bus)
011: Legacy DTV null packet (the official DTV stuffing packet).
100: PRBS 11
101: PRBS 15
110: PRBS 23
111: 0xFF (the official MEPG stuffing packet). (unsigned)

FSTATUS FEC spy status

7	6	5	4	3 2 1 0
SPY_ENDSIM	VALID_SIM	FOUND_SIGNAL	DSS_SYNCBYTE	RESULT_STATE
R	R	R	R	R

Address: 0xF5A4

Type: R

Reset: Undefined

Description: FEC spy status

[7] SPY_ENDSIM: 1: test finished, the number of packets designated by FSPYCFG.spy_hysteresis have been seen. (unsigned)

[6] VALID_SIM: 1: test positive, there is the right number of good packets (see FSPYCFG.spy_hysteresis). (unsigned)

[5] FOUND_SIGNAL: 1: good packet
0: false packet (unsigned)

[4] DSS_SYNCBYTE: 1: detection of Legacy DTV packets (syncbyte = 0x1D) (unsigned)

[3:0] RESULT_STATE: status of work in progress
0000: no signal
0001: data correct
0010: warning, packet declared false by the ERROR signal
0011: error, packet false
0100: warning, detection of inverse synchro word DVBS1
0101: error, bad synchro word
0110: --
0111: error, packet too long
1000: --
1001: warning, packet correct but deconnected from previous
1010: warning, MPEG TEI bit at 1
1011: stuffing packet good
1100: warning, stuffing packet correct but deconnected from previous
1101: error, packet too short
1110: --
1111: -- (unsigned)

FBERCPT4 BER/PER meter byte counter

7	6	5	4	3	2	1	0
FBERMETER_CPT[39:32]							
R/W							

Address: 0xF5A8

Type: R/W

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] FBERMETER_CPT: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligeable. (read put to 0 on a write,unsigned)

FBERCPT3 BER/PER meter byte counter

7	6	5	4	3	2	1	0
FBERMETER_CPT[31:24]							
R/W							

Address: 0xF5A9

Type: R/W

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] FBERMETER_CPT: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligeable. (read put to 0 on a write,unsigned)

FBERCPT2 BER/PER meter byte counter

7	6	5	4	3	2	1	0
FBERMETER_CPT[23:16]							
R/W							

Address: 0xF5AA

Type: R/W

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] FBERMETER_CPT: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligeable. (read put to 0 on a write,unsigned)

FBERCPT1 BER/PER meter byte counter

7	6	5	4	3	2	1	0
FBERMETER_CPT[15:8]							
R/W							

Address: 0xF5AB

Type: R/W

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] FBERMETER_CPT: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligeable. (read put to 0 on a write,unsigned)

FBERCPT0 BER/PER meter byte counter

7	6	5	4	3	2	1	0
FBERMETER_CPT[7:0]							
R/W							

Address: 0xF5AC

Type: R/W

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] FBERMETER_CPT: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligeable. (read put to 0 on a write,unsigned)

FBERERR2 BER/PER meter error bit counter

7	6	5	4	3	2	1	0
FBERMETER_ERR[23:16]							
R/W							

Address: 0xF5AD

Type: R/W

Reset: Undefined

Description: BER/PER meter error bit counter

[7:0] FBERMETER_ERR: counter of BITs or packets in error
fbermeter_err is not affected by FECSPY/bermeter_lmode.
Important note:
Regardless of mode, fbermeter_cpt and fbermeter_err are read in coherence: reading register FBERCPT4 provokes a sampling of fbermeter_cpt and fbermeter_err in the register buffers. It is those register buffers that will be read as long as a new reading of the FBERCPT4 register has not been made.
In rate mode (FSPYBER/fspyber_ctime different from 000 and 001), if a new measuring result arrives while a read is in progress (ie: FBERCPT4 has been read, but FBERERR0 has not yet been read), it will be lost.
Writing in any of the FBERCPT4..FBERCPT0 or FBERERR2..FBERERR0 registers at any time resets fbermeter_cpt and fbermeter_err to 0 (reset). This also resets FSPYOBS7..0 (the FEC Spy observer, see below). (read put to 0 on a write,unsigned)

FBERERR1 BER/PER meter error bit counter

7	6	5	4	3	2	1	0
FBERMETER_ERR[15:8]							
R/W							

Address: 0xF5AE

Type: R/W

Reset: Undefined

Description: BER/PER meter error bit counter

[7:0] FBERMETER_ERR: counter of BITs or packets in error
fbermeter_err is not affected by FECSPY/bermeter_lmode.
Important note:
Regardless of mode, fbermeter_cpt and fbermeter_err are read in coherence: reading register FBERCPT4 provokes a sampling of fbermeter_cpt and fbermeter_err in the register buffers. It is those register buffers that will be read as long as a new reading of the FBERCPT4 register has not been made.
In rate mode (FSPYBER/fspyber_ctime different from 000 and 001), if a new measuring result arrives while a read is in progress (ie: FBERCPT4 has been read, but FBERERR0 has not yet been read), it will be lost.
Writing in any of the FBERCPT4..FBERCPT0 or FBERERR2..FBERERR0 registers at any time resets fbermeter_cpt and fbermeter_err to 0 (reset). This also resets FSPYOBS7..0 (the FEC Spy observer, see below). (read put to 0 on a write,unsigned)

FBERERR0 BER/PER meter error bit counter

7	6	5	4	3	2	1	0
FBERMETER_ERR[7:0]							
R/W							

Address: 0xF5AF

Type: R/W

Reset: Undefined

Description: BER/PER meter error bit counter

[7:0] FBERMETER_ERR: counter of BITs or packets in error
fbermeter_err is not affected by FECSPY/bermeter_lmode.
Important note:
Regardless of mode, fbermeter_cpt and fbermeter_err are read in coherence: reading register FBERCPT4 provokes a sampling of fbermeter_cpt and fbermeter_err in the register buffers. It is those register buffers that will be read as long as a new reading of the FBERCPT4 register has not been made.
In rate mode (FSPYBER/fspyber_ctime different from 000 and 001), if a new measuring result arrives while a read is in progress (ie: FBERCPT4 has been read, but FBERERR0 has not yet been read), it will be lost.
Writing in any of the FBERCPT4..FBERCPT0 or FBERERR2..FBERERR0 registers at any time resets fbermeter_cpt and fbermeter_err to 0 (reset). This also resets FSPYOBS7..0 (the FEC Spy observer, see below). (read put to 0 on a write,unsigned)

FSPYBER BER/PER meter configuration

7	6	5	4	3	2	1	0
RESERVED			FSPYBER_SYNCBYTE	FSPYBER_UNSYNC	FSPYBER_CTIME		
R			R/W	R/W	R/W		

Address: 0xF5B2

Type: R/W

Reset: 0x10

Description: BER/PER meter configuration

[4] FSPYBER_SYNCBYTE: 1: reset of BER/PER Meter if error on synchro word and if result_state = 0x7 or 0xD (that is, packet too short or too long). (unsigned)

[3] FSPYBER_UNSYNC: 1: reset of BER/PER Meter if desynchronization
0: no reset, wait for it to come back by itself (unsigned)

[2:0] FSPYBER_CTIME: BER/PER measuring time
000: counting the error bits or packets to infinity
001: reserved
010: measure on 2^16 bytes 2^9 packets
011: measure on 2^18 bytes 2^11 packets
100: measure on 2^20 bytes 2^13 packets
101: measure on 2^22 bytes 2^15 packets
110: measure on 2^34 bytes 2^17 packets
111: measure on 2^26 bytes 2^19 packets
The FECSPY.bermeter_lmode = 1 mode adds 8 to the exponent. (unsigned)

RCCFG2 Configuration of the merger-hardware stream return channel line

7	6	5	4	3	2	1	0
R/W							

Address: 0xF600

Type: R/W

Reset: 0x20

Description: Configuration of the merger-hardware stream return channel line

TSGENERAL — General configuration of the stream merger hardware

7	6	5	4	3	2	1	0
RESERVED				MUXSTREAM_OUTMODE	TSFIFO_PERMPARAL		RESERVED
R				R/W	R/W		R

Address: 0xF630

Type: R/W

Reset: 0x0

Description: General configuration of the stream merger hardware

[3] MUXSTREAM_OUTMODE: 1: the lines 1, 2 and RC ore connected to the transport steams according to tsfifo_permparal.
0: the outputs are routed as follows
Line 1 -> TS3
Line 2 -> TS2
RC line -> TS1 (unsigned)

[2:1] TSFIFO_PERMPARAL: parallel bus allocation=.
00 Line1 -> TS3, Line 2 -> TS2, RC Line -> TS1
01 Line1 -> TS2, Line 2 -> TS3, RC Line -> TS1
10 Line1 -> TS1, Line 2 -> TS2, RC Line -> TS3
11 Line1 -> TS3, Line 2 -> TS2, Parallel bits D63..D03 common (Muxmode). (unsigned)

17.10 TST register descriptions

TSTRES0 Test reset control 0

7	6	5	4	3	2	1	0
FRESFEC	RESERVED						
R/W	R						

Address: 0xFF11

Type: R/W

Reset: 0x0

Description: Test reset control 0

[7] FRESFEC: 1: force reset LDPC FEC (unsigned)

TCTL4

7	6	5	4	3	2	1	0
RESERVED		PN4_SELECT	RESERVED				
R		R/W	R				

Address: 0xFF48

Type: R/W

Reset: 0x0

Description:

[5] PN4_SELECT: Selection of phase noise derating factor list
1: PN4
0: PN1 (unsigned)

TSTDISRX Test DiSEqC Rx configuration

7	6	5	4	3	2	1	0
RESERVED				PIN_SELECT[2:2]	RESERVED		
R				R/W	R		

Address: 0xFF67

Type: R/W

Reset: 0x0

Description: Test DiSEqC Rx configuration

[3] PIN_SELECT: Select DiSEqC n input pin and polarity.
00: Analog, DISEQCINn pin;
01: n=1 GPIO1. n=2 GPIO4.
10: Inverted analog, DISEQCINn pin
11: Inverted GPIO1/4 (unsigned)

18 Revision history

Table 42. Document revision history

Date	Revision	Changes
Jul-2007	A	Initial release.
Feb-2008	B	New process (CMOS80), Overview, JTAG, Electrical spec and register list sections updated.
Apr-2008	C	Overview, electrical spec, package and register list sections updated.
12-Dec-2008	D	Updated *Table 3 on page 10* for generic stream capability support updated text for environmentally-friendly packaging *on page 75* Updated register *DMDCFGMD on page 132* Added register *DMDT0M on page 134* , Added tuner registers (TNRxxx) to *Section 17.6 on page 190*.
21-Apr-09	E	STV0903BAB (cut 2.0) full data sheet release. - The words 'preliminary data' removed from cover page. No other change.
04-May-09	F	1.2 - new datasheet versions mentioned. 1.2 - rate claims revised (1 to 45Mbaud in S2, 1 to 62Mbaud in S). 1.3 - table 2. Reference to parallel Mux stream removed. Table 3. Footnote concerning bugged ISSYI removed. Issyi -> yes. Dummy frame insertion -> Yes. 2, 3, 4 - no change 5-Demod, Many minor updates. AEP section revised. 6.0- DVB-S1 FEC. No change 7.0-DVB-S2 FEC. 7.5.7 BCH check added 8, 9, 10 TS, DiSEqC and FSK. No change 11.3 - GPIO: STREAM_STATUS bits updated in table 17. Table 18 added. 12 IRQ. No change. 13: JTAG identifiers updated for cut 3.0. 14: Elec spec. No change 15 Package. No change 16 Appli: No change. 17.0-Register list regenerated and revised (applicable to cut 3.0 only). 18.0 Rev history: Rev F changes are added.

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