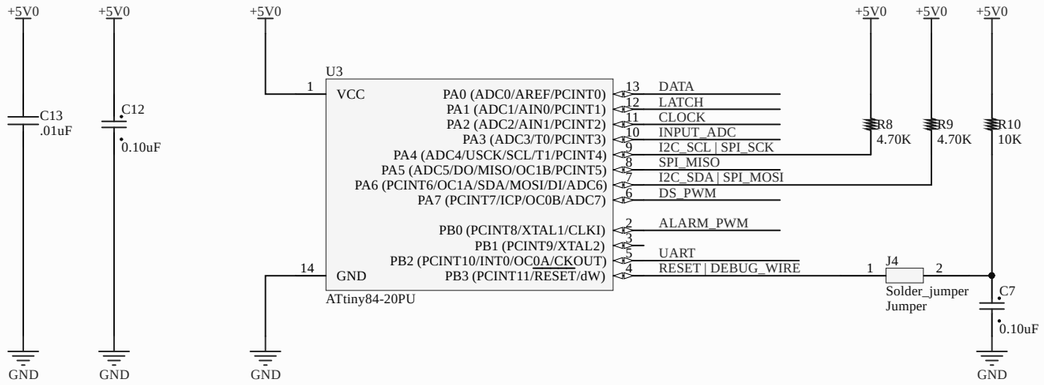
# TinyClock

CONFIDENTIAL

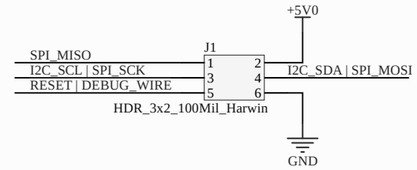
Project Name: TinyClock

| | | | |
|---|---|---|---|
| Title ***Preamble*** | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 1 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Preamble.SchDoc | |
| Engineer(s): | | | |

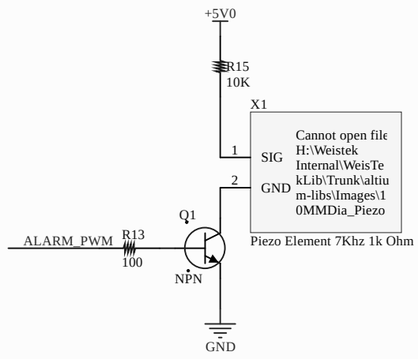
# MICROCONTROLLER



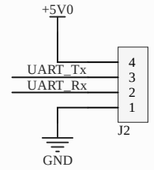

# ICSP PROG HEADER



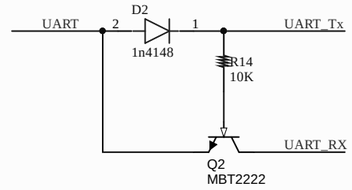

# ALARM




# UART DEBUG




# Tx/Rx Single Pin

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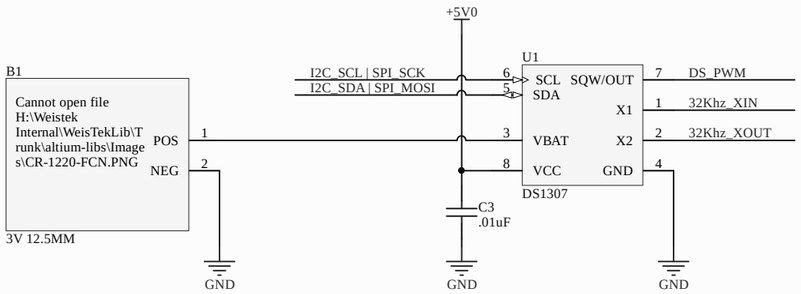
Project Name: TinyClock

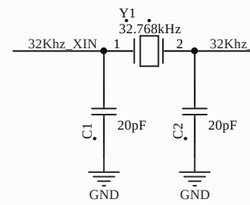
| | | | |
|---|---|---|---|
| Title *Micro Controller ATTiny84* | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 2 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Microcontroller_ATTINY84.SchDoc | |
| Engineer(s): | | | |

| Date | Revision |
|---|---|
| MM/DD/YYYY | |
| 4/27/2018 | 0.2 |

# DS1307 RTC




# 32Khz CRYSTAL

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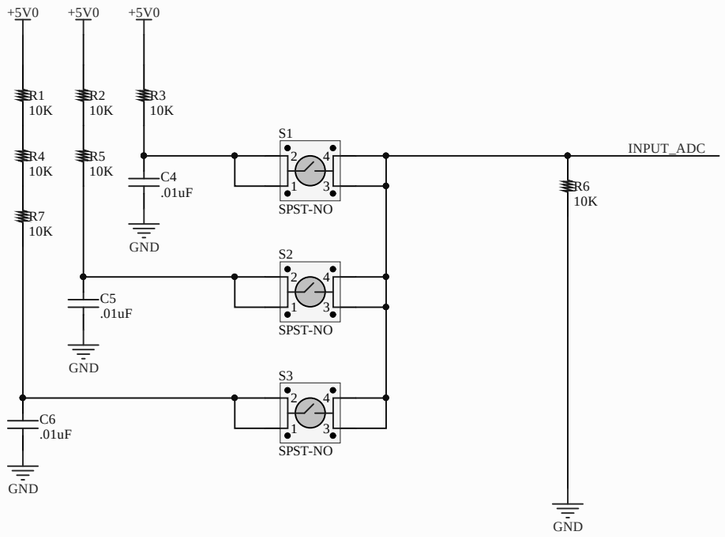
Project Name: TinyClock

| | | |
|---|---|---|
| Title: ***Clock DS1307 RTC*** | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 |
| Variant: [No Variations] | | Sheet 3 of 1 |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Clock_DS1307.SchDoc |
| Engineer(s): | | |

# USER INPUT

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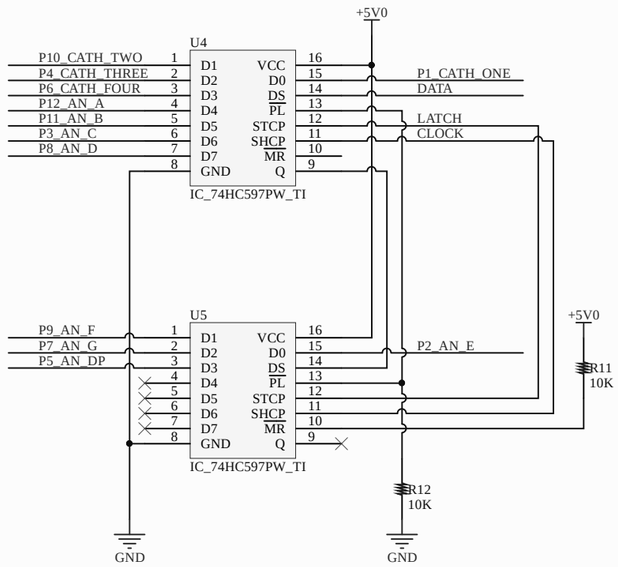
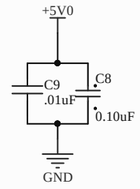
|---|---|---|---|
| CONFIDENTIAL | Project Name: TinyClock | | |
| Title ***Inputs*** | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 4 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Inputs.SchDoc | |
| Engineer(s): | | | |

# MULTIPLEX 74HC595

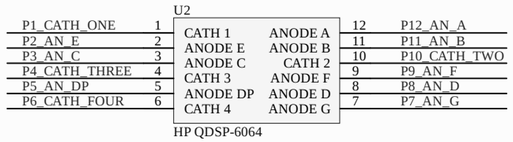



CONFIDENTIAL

Project Name: TinyClock

| | | | |
|---|---|---|---|
| Title: ***Multiplexer 74HC595*** | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 5 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Multiplex_74HC595.SchDoc | |
| Engineer(s): | | | |

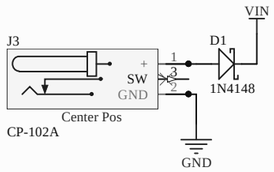



CONFIDENTIAL

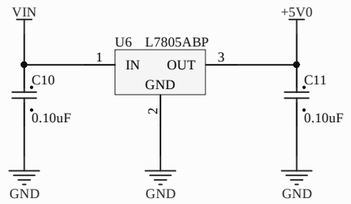
Project Name: TinyClock

| | | | |
|---|---|---|---|
| Title ***Display HP QDSP-6064*** | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 6 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Display_HP QDSP-6064.SchDoc | |
| Engineer(s): | | | |

# POWER INPUT




# +5V0

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Project Name: TinyClock

| | | | |
|---|---|---|---|
| Title ***Power*** | | | *Weistek Engineering* |
| Size: 11x17 | Number: 0.2 | Revision: 0.2 | |
| Variant: [No Variations] | | Sheet 7 of 1 | |
| Date: 4/27/2018 Time: 10:16:02 PM | | File: Power.SchDoc | |
| Engineer(s): | | | |