25 Watt USB Charger Power Supply

Theory of Operation

V1.1

Introduction

This project originated with the need for a high capacity USB charger power supply as part of my solar panel evaluation. I needed a supply that could provide full power simultaneously to two devices, delivering at least 10W to each. In usual fashion I preferred to build my own vs. buy and a quick scan of the market didn't reveal anything suitable that wouldn't require modification anyway.

The power requirement was set at 25 watts (5A @ 5VDC). At this level a freewheeling diode would produce significant loss so a synchronous buck would be far more efficient. At the time I was working on a full bridge inverter using the PIC16F1769 MPU and realized that it could easily be adapted to a buck converter with the same controller, a single high/low gate drive in a half bridge configuration (the low side driving the freewheeling or synchronous switch), and the same MOSFET transistors. The controller software rewrite would be easy; this was good since I didn't want to spend significant time on it.

Footnote: the synchronous buck control requires more work to realize peak efficiency across the load spectrum. While it achieves efficiencies exceeding 90% at moderate & higher loads it suffers at lower values, particularly below the inductor's critical current value. This is because the low-side switch is left on too long. Refinement of this control is likely possible but requires a reconfiguration of some PIC peripherals (again, reference 125vbuck-theory_op-sync_buck-pic16f1769.docx).

Description of Operation

The 125 is a 12VDC to 5VDC non-isolated, fixed frequency (100kHz), synchronous buck power supply (PS) capable of delivering 25 watts of continuous power at 5VDC with efficiencies exceeding ninety percent. It is designed to be used with 12-volt photo-voltaic and windmill off-grid power generating systems to charge smartphones, tablets, and other USB rechargeable devices. Features:

- 11-20V DC Input voltage range
- Input reverse polarity protection
- Input over / under volt protection
- Input fuse (5A) protection
- Output over-current protection
- Output over / under volt protection
- Output Solid State Relay (SSR) to prevent discharge of connected device when power supply is off
- Soft start
- Auto-recovery from most fault conditions
- On/off switch
- Status indicator LED
- Screw terminal connectors

Unlike most PS that use a dedicated controller the 125 uses the PIC16F1769 MCU. The on-chip peripherals are configured to autonomously handle all real-time functions (modulator, gate drive signals, over-current, etc.) while the processor performs oversight functions including startup and abnormal condition recovery.

Specifications

Input voltage:	11 – 20V DC
Input current:	3A
Output voltage:	5V DC
Output current:	0 – 5A
Ripple:	27mV peak-peak max
Transient response:	2.58mS to be within 100mV of specified output voltage
Regulation:	1%
Operating temperature:	-20C – 50C (characterized but not tested)

Input Power

The PS derives power for operation from a set of input terminals. A SPDT switch connects power from the terminals to the inrush limit circuit. The inrush circuit limits current to a maximum of 200mA to prevent nuisance opening of the input protection fuse, F1. This is necessary due to the large input bulk capacitance of the PS. U2, a SSR, bypasses inrush limiting after a predetermined amount of time and is controlled by the PIC MPU, U1.

Power is distributed to the switching section and 5V LDO regulator U3. The LDO provides a regulated 5V for the PIC and logic side of the gate controllers.

Anticipating that the PS will be connected to a power source with long leads, the LDO and power switch section bulk capacitors C5, C16, and C18 are sufficiently sized to minimize input ripple and ensure glitch-free operation at higher operating power levels. High frequency noise decoupling is provided by C6, C7, and C19.

Buck Section

The power section consists of high side switch Q2 and free-wheeling (synchronous) switch Q3 in a half bridge configuration. Gate driver U4 drives both switches using a bootstrap configuration for the high side and direct drive for low. T1 is a uni-directional current transformer that provides high-side pulse-level current sensing. R18 is the burden resistor and sets the mV/A value and R17 ensures that the core resets prior to the next period.

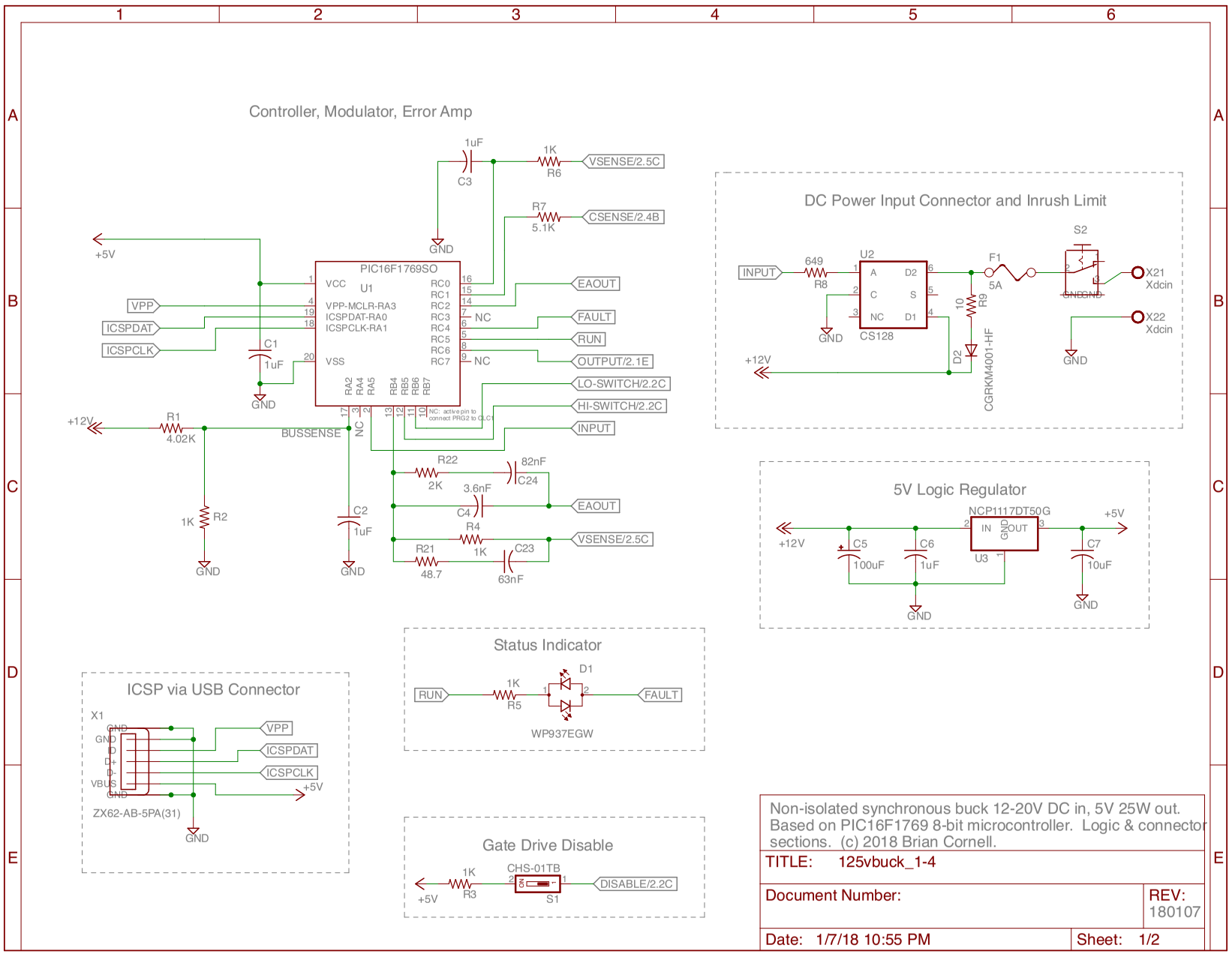
L2 is wound on an MPP core and is designed for continuous mode operation; the critical current value is ~ 200mA with a maximum DC of approximately 48% at minimum input voltage & maximum load. It is wound with four strands of 22AWG wire (polyfilar) for minimum DC loss.

Output Section

Bulk output & ripple filtering is provided by C20; it is sized to provide less than 50mV max. C21 & C22 provide high frequency decoupling.

Because the PS is not isolated there is risk that a battery powered device left connected to the supply when it is off could bias the supply. This could lead to damage the PS as well as draining the battery. To prevent this a discrete SSR is used.

A custom SSR is used on the output because of the higher current output of the PS and the very low on-state resistance of MOSFET (>6mΩ) Q4; monolithic SSR solutions would require heatsinking and reduce PS efficiency. Because this switch remains on (e.g. not switched), conventional gate drives don't work. A very low power isolated flyback supply drives the gate. The PWM signal operates at 100kHz with a fixed pulse width. R12 functions as a burden resistor. The combination of duty cycle and R12 are set to deliver a voltage that saturates the gate but is well under the maximum value. The gate capacitance is augmented by C14 to keep ripple voltage at ~ 1V or less. R12 also discharges the gate with the PWM is switched off.


Controller, Modulator, Error Amp
PIC16F1769SO
U1
VCC
VPP-MCLR-RA3
ICSPDAT-RA0
ICSPCLK-RA1
VSS
RC0
RC1
RC2
RC3
RC4
RC5
RC6
RC7
NC
NC: active pin to connect PRG2 to CLC
+5V
VPP
ICSPDAT
ICSPCLK
C1
1uF
GND
C3
1uF
R6
1K
VSENSE/2.5C
R7
5.1K
CSENSE/2.4B
EAOUT
FAULT
RUN
OUTPUT/2.1E
LO-SWITCH/2.2C
HI-SWITCH/2.2C
INPUT
+12V
R1
4.02K
BUSSENSE
R2
1K
C2
1uF
R22
2K
82nF
C24
3.6nF
C4
R4
1K
R21
48.7
C23
63nF
DC Power Input Connector and Inrush Limit
INPUT
649
R8
U2
CS128
A
C
NC
D2
S
D1
F1
5A
S2
GNDGND
X21
Xdcin
X22
Xdcin
10
R9
D2
CGRKM4001-HF
+12V
5V Logic Regulator
NCP1117DT50G
IN
GND
OUT
U3
+12V
C5
100uF
C6
1uF
C7
10uF
+5V
Status Indicator
RUN
1K
R5
D1
FAULT
WP937EGW
ICSP via USB Connector
X1
GND
GND
ID
D+
D-
VBUS
GND
VPP
ICSPDAT
ICSPCLK
+5V
ZX62-AB-5PA(31)
Gate Drive Disable
+5V
1K
R3
CHS-01TB
S1
DISABLE/2.2C
Non-isolated synchronous buck 12-20V DC in, 5V 25W out.
Based on PIC16F1769 8-bit microcontroller. Logic & connector sections. (c) 2018 Brian Cornell.
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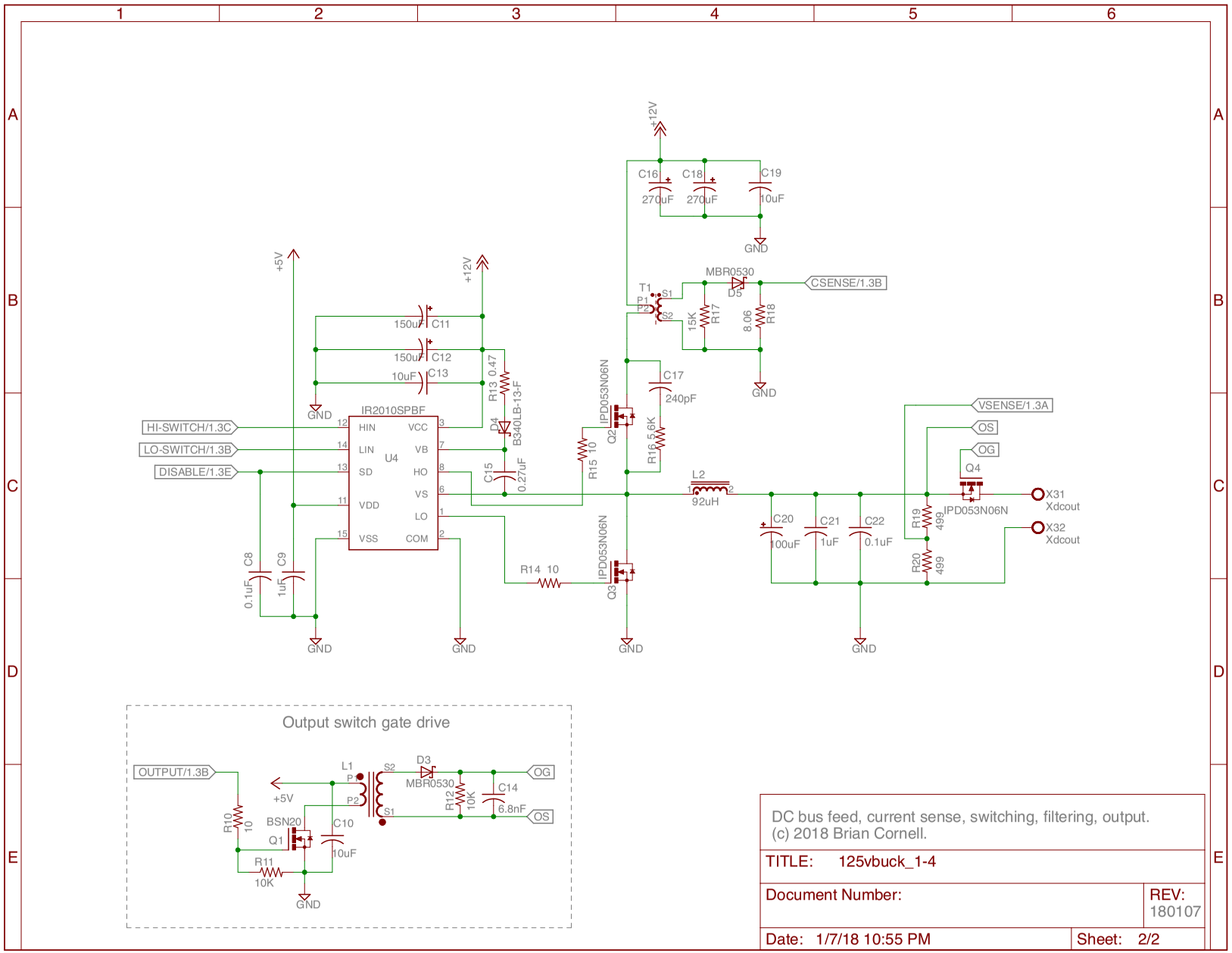
1
2
3
4
5
6
A
B
C
D
E
+12V
C16
270uF
C18
270uF
C19
10uF
GND
MBR0530
D5
CSENSE/1.3B
T1
P1
P2
S1
S2
15K
R17
8.06
R18
+5V
+12V
150uF
C11
150uF
C12
10uF
C13
R13 0.47
B340LB-13-F
D4
C17
240pF
IPD053N06N
Q2
R16 5.6K
R15 10
IR2010SPBF
HI-SWITCH/1.3C
LO-SWITCH/1.3B
DISABLE/1.3E
HIN
LIN
SD
VDD
VSS
VCC
VB
HO
VS
LO
COM
U4
C15
0.27uF
L2
92uH
VSENSE/1.3A
OS
OG
Q4
IPD053N06N
X31
Xdcout
X32
Xdcout
C20
100uF
C21
1uF
C22
0.1uF
R19
499
R20
499
C8
0.1uF
C9
1uF
R14 10
IPD053N06N
Q3
Output switch gate drive
OUTPUT/1.3B
L1
D3
MBR0530
R12
10K
C14
6.8nF
R10
10
BSN20
Q1
C10
10uF
R11
10K
DC bus feed, current sense, switching, filtering, output.
(c) 2018 Brian Cornell.
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Q1 provides the primary side drive and is driven directly by the PIC. C10 provides charge for the flyback to minimize noise on the 5V supply.

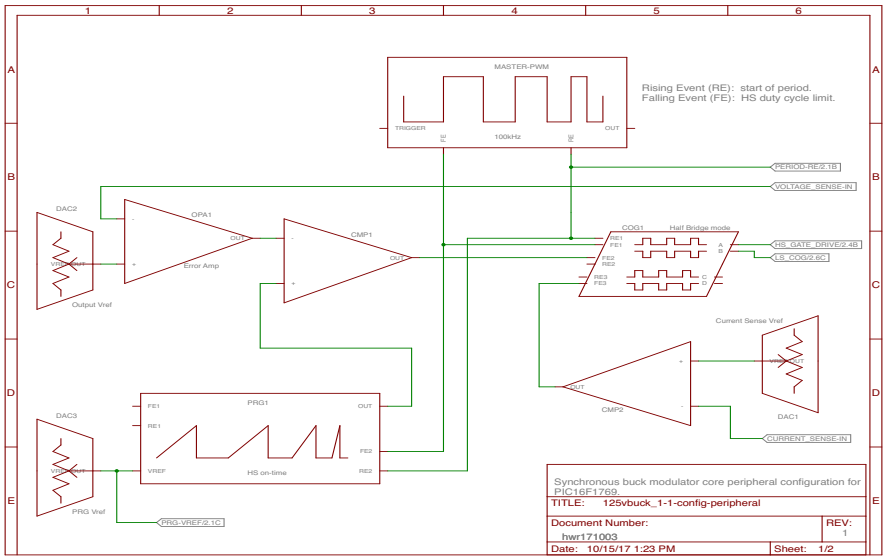
Control Loop

The PS is designed for continuous (inductor) mode operation with a maximum DC < 50% at minimum input voltage and maximum load and so the control loop is designed around this premise. It is constructed using PIC on-board peripherals to form a conventional analog control loop.

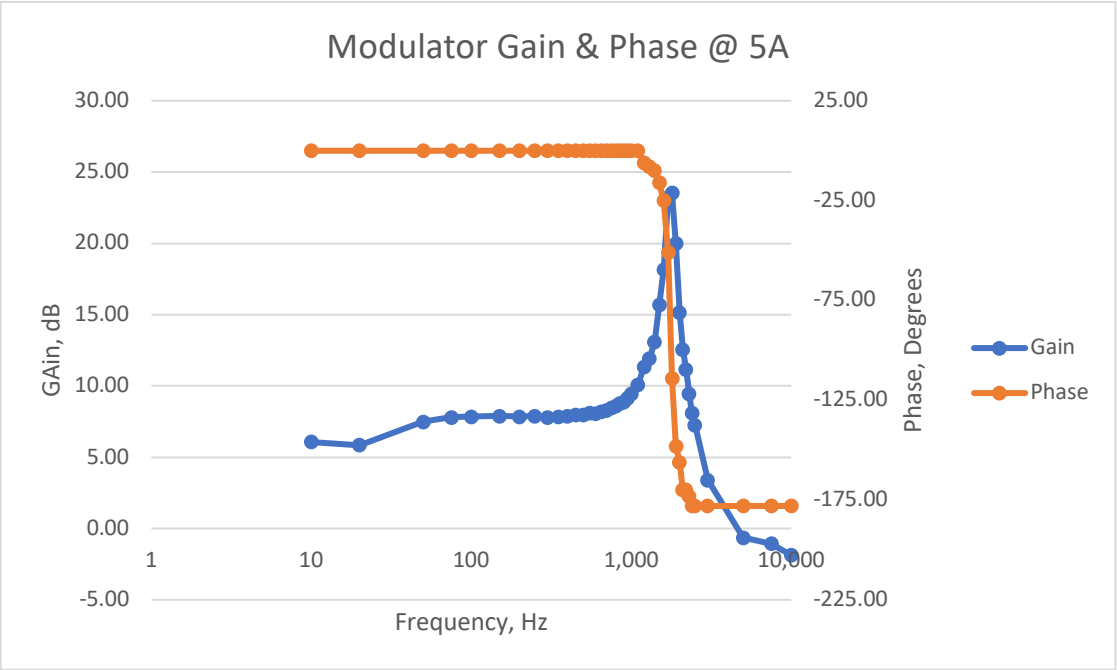
A PIC timer generates a 100kHz signal that is used by the PWM for the operating frequency of the PS. During normal operation the DC of the PWM is fixed at a DC value (approximately 50%). This is slightly above the expected DC at maximum load and minimum input, and provides the Rising & Falling Event (RE, FE) necessary for loop operation.

The Complementary Output Generator is configured to operate in half-bridge (complementary) mode: its HS output drives the HS switch and the LS output is connected to the synchronous control (LS) logic (refer to 125vbuck-theory_op-sync_buck-pic16f1769.docx for a complete discussion of the LS / synchronous control methodology). A RE from the PWM marks the start of the period and COG1 sets its HS output TRUE. A FE from the PWM or Comparator one / two (CMP1/2) marks the end of the DC and COG1 sets HS output FALSE and LS TRUE; LS will remain TRUE until start of next period. Note that the first FE to occur terminates the COG HS output (e.g. DC of the PS); hence the PWM DC sets the maximum DC.

The Programmable Ramp Generator one (PRG1) generates the linear ramp that is used to time the DC for a given period. A RE from the PWM begins the ramp and a FE from the PWM terminates (discharges). The PRG requires a voltage referenced that is used to set the voltage from which ramp generation begins. Digital to Analog Converter three (DAC3), a 5-bit DAC, is set to 0V (GND).

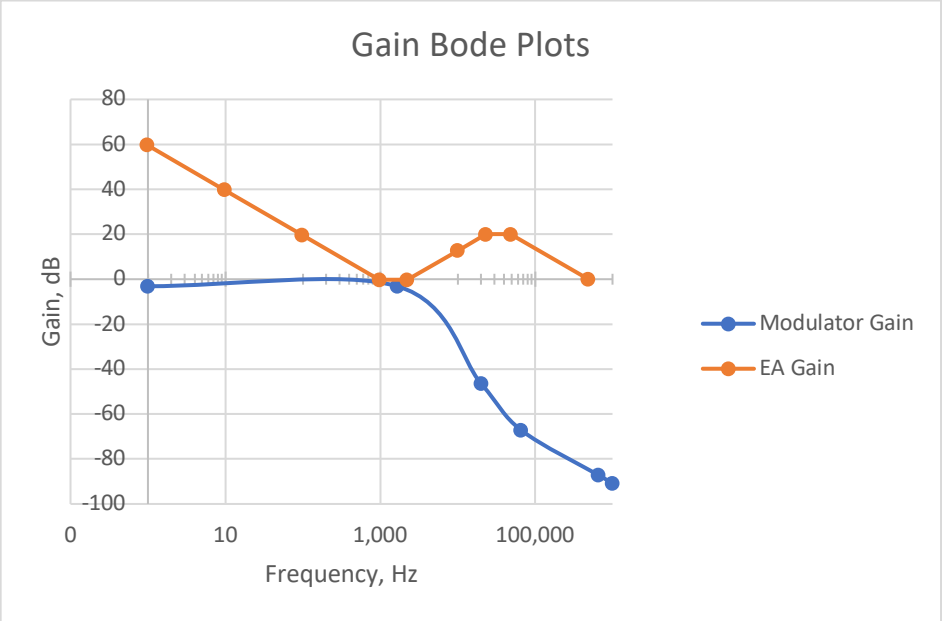


As is depicted by the open loop bode plot of the modulator, below, and the use of low ESR output capacitor C20 (ESR zero at 66kHz), Operational Amplifier one (OPA1) is configured as a type 3[1] error amplifier. Note that the gain curve is inaccurate above 3kHz due to inability to accurately measure with available equipment.



The figure below plots the calculated gain for the modulator and error amp.

[1] Venable, H. D. (1983) The K Factor: A new mathematical tool for stability analysis and synthesis. Proceedings of Powercon10, https://venable.biz/tech-pubs/The%20K%20Factor%20a%20New%20Mathematical%20Tool%20for%20Stability%20Analysis.pdf



The gain curve is designed for a cut-off frequency, Fco, of 10kHz with a phase boost of 133 degrees. R22 sets the first zero at 970Hz and C23 the second at 2.2kHz. The first pole is set by C4 at 23kHz and R21 sets the second at 48kHz.

R19 & R20 halve the output voltage and provide the sense input to OPA1. DAC2, a 10-bit DAC, provides a 2.5V reference for OPA1 and allows for fine adjustment of the output voltage. CMP1 compares OPA1 and PRG1 output values and generates a FE signal to COG1 when the ramp value > error value.

CMP2 provides pulse-pulse current limiting by monitoring the current sense signal via R7 and comparing to the voltage reference provided by DAC1, also a 10-bit DAC. A FE signal is generated if the sense value exceeds the reference. Like the output voltage, the current limit value can be dynamically adjusted in software.

At the start of a period the PWM goes high which generates a rising event: the COG LS output is switched off, HS switched on, and linear ramp is started. OPA1 compares the output voltage to the reference provided by DAC2 and outputs an error correction voltage. CMP1 compares OPA1's output to the ramp value and when the ramp exceeds CMP1 generates a falling event. COG1 turns off HS and turns on LS (synchronous control logic ultimately determines turn-on/off of LS). At 50% DC the PWM generates another falling event which resets PRG1 so it's ready at the start of the next period.

Should an over-current event occur CMP2 will generate a FE that will terminate the DC early. The voltage & current sense loops operate in parallel which means that during a sustained over-current condition the voltage sense loop will demand maximum DC but the current sense loop will limit to a much lower value. Without intervention from the controller the characteristic behavior will be maximum allowable current at some lower voltage.

Controller

The controller is a PIC16F1769 8-bit MPU that contains most of the components used in the control loop along with its processor, flash program memory, and RAM. The controller's functions are to manage startup, abnormal conditions, and restart.

Startup

During initialization all peripherals are configured for operation. During this time the PS output and inrush bypass are off and the Fault pin is set TRUE. Prior to entering the main control loop the input voltage is read from the BUSSENSE pin (via voltage divider R1 & R2) using the Analog to Digital Converter (ADC). The input voltage must be <20 & >11 VDC. If greater than the PS is permanently disabled: inrush bypass is left off to limit dissipation on the 5V LDO U3 and the Fault pin flashes an error code. The PS must be power-cycled to recover from this condition (voltages much higher than 20V DC will likely result in permanent damage to U3 and possibly other components).

If the input voltage is low the unit will turn inrush bypass on but will not start: the Fault pin will flash an error code. Input voltage will be continuously monitored and when it exceeds the Under-Volt-Lock-Out (UVLO) recovery voltage (12V DC) the PS will attempt to start.

The PS employs a software controlled soft start. The PWM DC is initially set to zero and the control loop enabled. DC is then incremented to the maximum in one degree increments with a fixed delay between each. When maximum is reached the PS is considered to be in Run state and the run loop assumes control. During the start cycle current limiting is active (as is the entire control loop).

Run Loop

During normal operation the MPU is not active in the PS' performance. Several parameters are monitored:

- Input (bus) voltage – high/low
- Output voltage – high/low
- Over-current

Parameter monitoring and action employs a hysteresis algorithm that ensures glitch-free operation. Example – connecting a low-impedance load to the output may cause an instantaneous over-current but goes away once the device charges up. The PS would be useless if it shutdown under such a circumstance. Hence, the hysteresis sets thresholds for the number of events that must occur before an action is taken. An event is defined as a discrete sampling of input or output voltage or, for the case of over-current, an interrupt generated by CMP2. The thresholds vary by parameter and are a balance between protecting the PS and/or attached device(s) and user intervention.

Abnormal Handling & Recovery

When a monitored parameter exceeds its threshold the control loop intervenes:

- Input over-volt – disables PS and requires power cycle to recover
- Input under-volt – stops PS, monitors input voltage & restarts when it exceeds recovery limit
- Output over/under-volt – stops PS, attempts restart
- Over-current – stops PS, attempts restart

All conditions will flash an error code on the status LED via the Run/Fault pins. The LED will remain solid red momentarily and then flash a set number of times to indicate the fault. The sequence will then repeat.

```
2       //Stopped - bus under-volt lockout
3       //Stopped - over-current lockout
4       //Stopped - output under-volt lockout
5       //Stopped - output over-volt lockout
6       //Disabled - bus over-volt lockout
```

For all conditions except input over/under-volt, the PS will continually attempt to recover using this sequence:

1. Detect error
2. Stop PS
3. Display error code
4. Restart

An input over-volt condition was previously discussed. For Input-under-volt the controller will attempt a restart when the input voltage recovers. Note that this value is higher than the shutdown value to allow the power source (presumably a battery storage system) to recover.

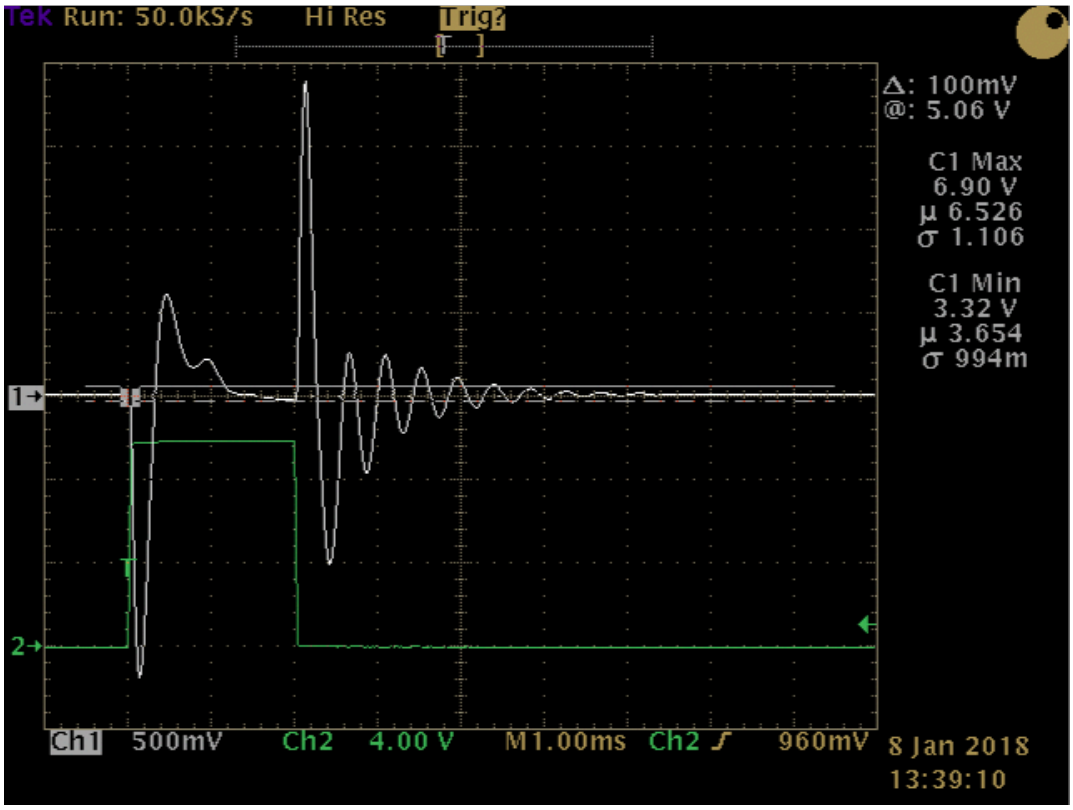
Thermal Protection

The design does not incorporate thermal protection because of its high efficiency. Maximum temperature rise at minimum voltage and full load is 25C above ambient. The design is not intended to be operated in environments with ambient temperatures above 50C.

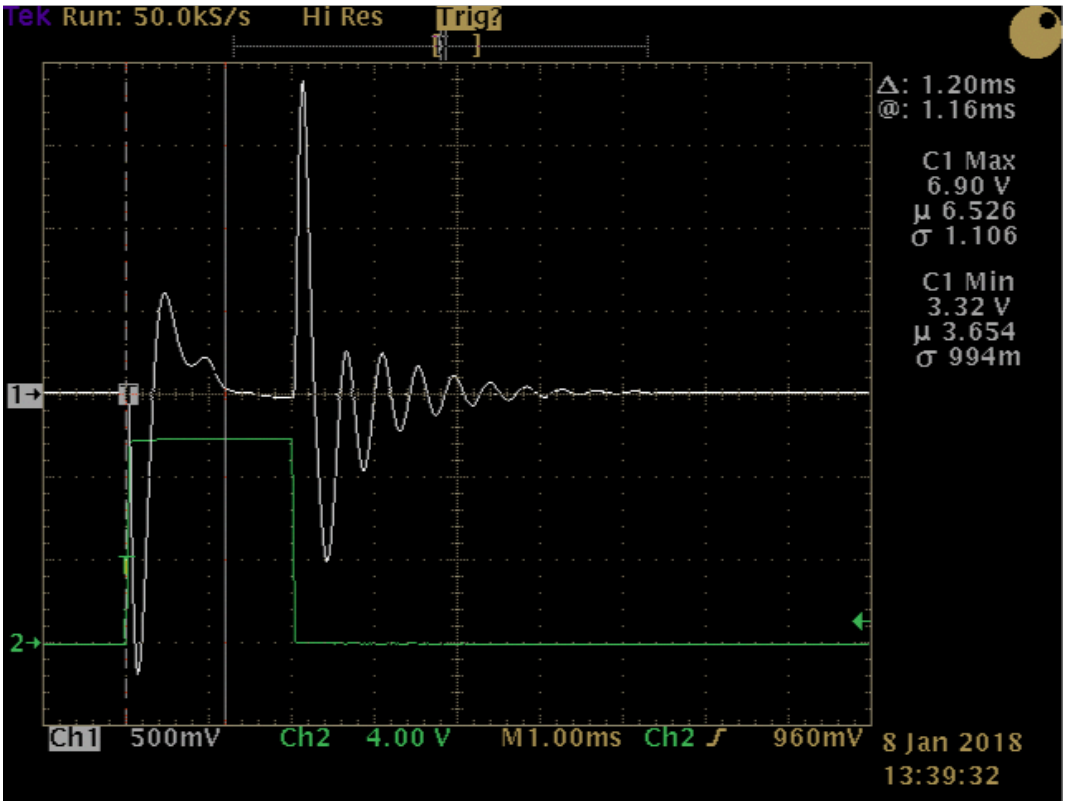
Transient Performance

Transient testing was performed using fixed resistances connected directly to the supply's output. One resistance attached directly to the supply output terminals set the baseline load at 1A, approximately 20% of rated output. The second load is also attached directly to the output but is switched through a MOSFET driven by a function generator. The switched resistance moves the supply load to 4.3A, about 87% of rated output. Pulse rise time was not rate-limited so the load application rate is higher than 5A/µS.

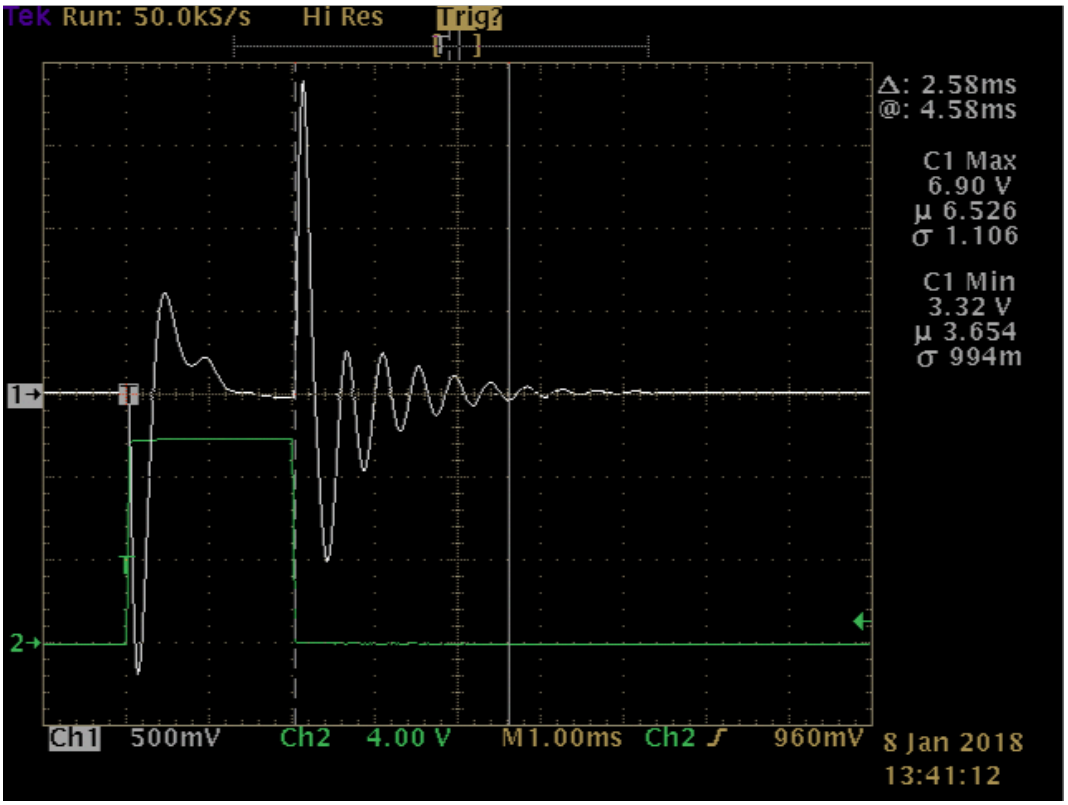
The figures below show the design's response to a 2mS pulse at minimum input voltage (transient response improves with increased input voltage). Channel one is DC coupled and shows the DC output (channel has 5V offset to measure at sufficient resolution). Channel two is the MOSFET drive pulse and is the trigger for the trace.



The horizontal cursor is the reference for the tolerance band: 100mV.



The trace above shows recovery time at transient start: 1.2mS



And the final trace shows recovery time at termination: 2.58mS.

The large over-shoot at termination is due to C20, 100uF, not being of sufficient value to absorb the energy stored in L2 (load dump at end of transient). For example, to limit over-shoot to 250mV when going from full to zero load C20's value would need to be:

$$\frac{LI^2}{V_{max}^2 - V_{out}^2} \approx C$$

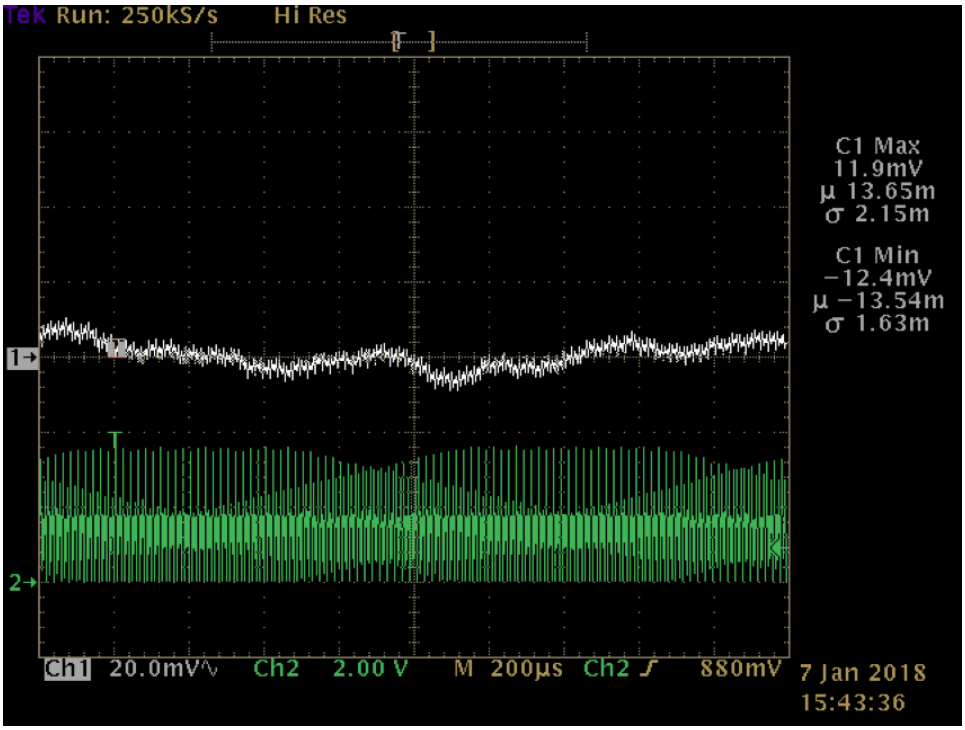
where L=filter inductor value,
I=instantaneous current in inductor at end of transient,
V_{max}=maximum allowable output voltage overshoot
V_{out}=rated output voltage.

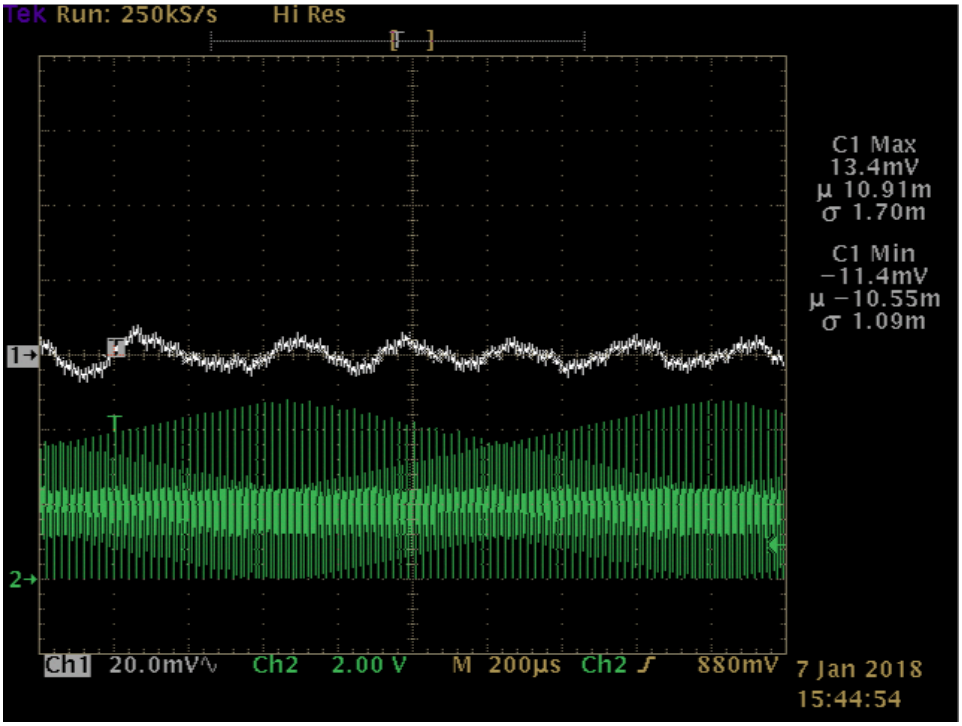
Substituting,

$$\frac{.000092 \times 5^2}{5.25^2 - 5^2} \approx 898uF$$

Ripple

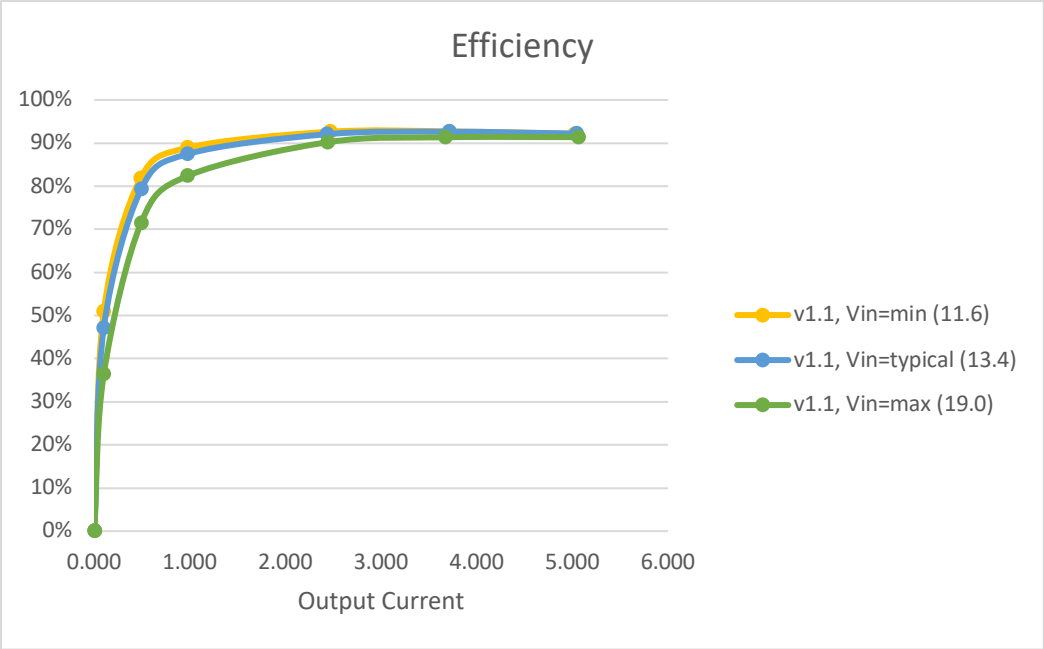
Ripple was measured at no & full load and is depicted in the following two traces. Channel 1 is AC coupled to the output and channel 2 is HS switch signal that serves as the trigger. Ripple is slightly higher, 27mV P-P, at no-load than at full, 21mV P-P.





Efficiency

Design efficiency was measured at minimum (11V), maximum (20V), and typical (13.4V) input voltages with static loads ranging from 100mA to 5A. At 50% load and higher the design achieves better than 90% efficiency. Efficiency runs above 80% for loads above 1A Below this efficiency drops due to light load inefficiencies in the synchronous (LS) switch algorithm and the use of an LDO for the logic supply (this is most impactful at high input voltages).



Conclusion

The design objectives have been met and the unit provides modest performance without the use of monolithic power supply controller chips. Advantages are flexibility in design & features and the ability to experiment. Disadvantages are increased component count & complexity and perhaps some loss of efficiency.

This basic design could be scaled up to provide upwards of 40-plus watts without significant modification. Changes would include the use of 2oz copper PCB traces, increased fuse size, and a higher rated input SSR. The inductor is operating at a peak of ~ 0.4T and should be evaluated for the desired higher power setting to ensure it has sufficient saturation margin. Regardless, it will run hotter (current design current density ~ 425A/cm^2).

It goes without saying that active thermal management will likely be required and some form of thermal protection should be incorporated.