Using the PIC 16F1769 as a Synchronous Buck Controller

14 August 2017

Introduction

Using the PIC16F1769 in a non-isolated buck synchronous topology presents a challenge to effectively control the low-side (LS) switch in a cost-effective manner.

The LS switch must be on long enough to allow the transfer of energy from the output inductor. In continuous mode above the critical inductor current this isn't a problem: the LS can be left on for the duration of the period post high-side (HS) duty cycle (DC). However, below this, or in abnormal situations (start-up, short circuit, etc.), the LS must be commutated off prior to the end of the period to prevent discharge of the output filter capacitor(s) thru the LS.

The most effective method to accomplish this would be to monitor current thru the LS, but this adds cost & complexity. A cost-effective alternative is to time the LS on-time to approximate that of the HS. This is based on the premise that the inductor charge / discharge cycle is a linear ramp with similar slopes. There will be situations, such as those previously mentioned or with a high input voltage, that this approach will prematurely turn the LS switch off but, in those cases the body diode of the switch will provide an alternate path with minimal loss of efficiency. The approach presented here also allows for some tuning to the operating environment to address these affects.

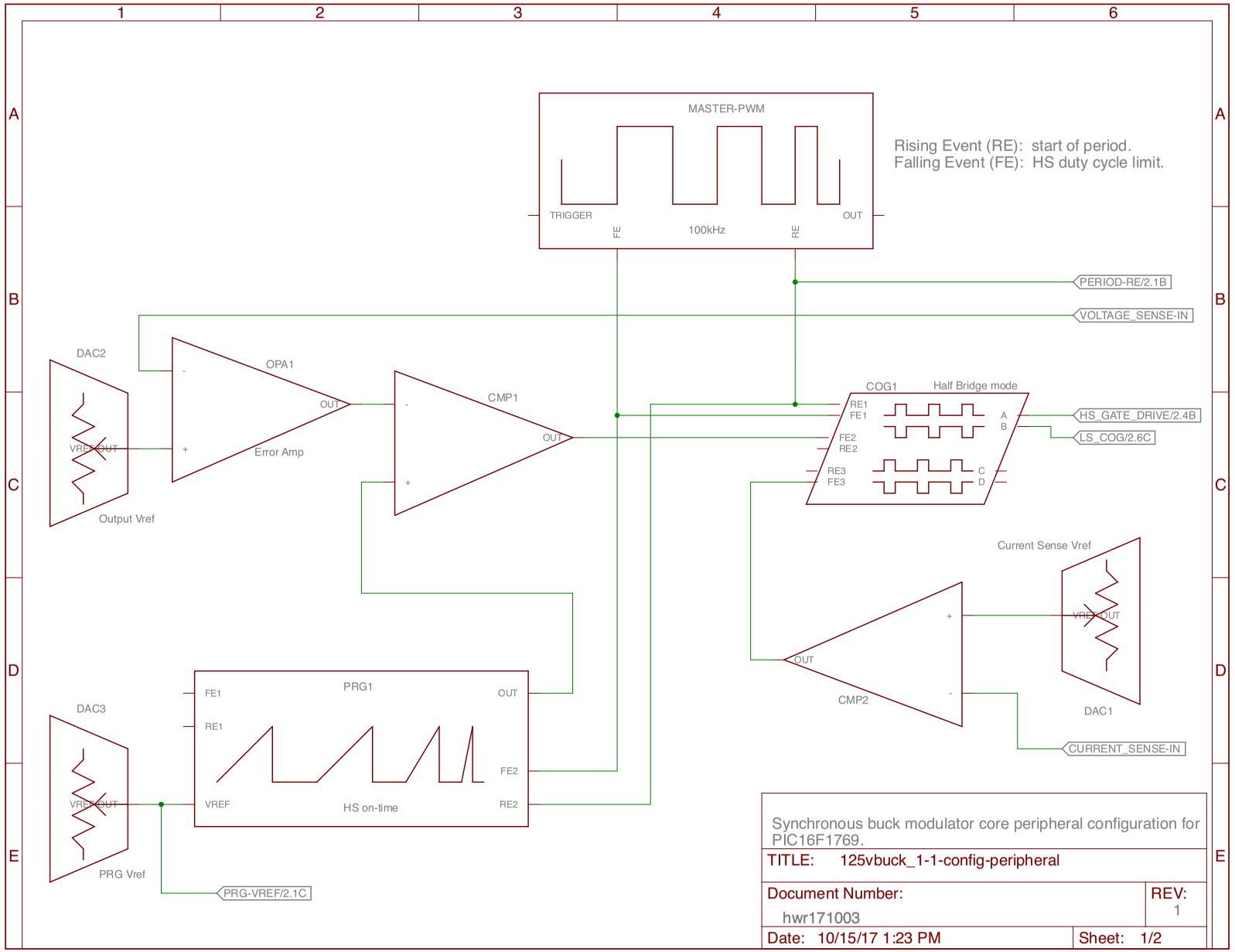
To approximate the LS on-time to that of the HS, the HS must be timed on a per-cycle basis and then used to limit the LS on-time. Given the speed of the design (100kHz) all of this must be done in hardware. The only peripheral to support this is the Programmable Ramp Generator (PRG) in charge / discharge mode. But for this to work it is imperative for the ramp to be fully discharged by the end of the period; otherwise the ramp will 'walk off center' and fail to provide the proper timing. Hence, the PRG must be used with support from other peripherals to provide a stable operating environment.

The modulator core and HS control are discussed first and then LS control is addressed.

Modulator Core

The core consists of a master PWM signal, Complementary Output Generator (COG), PRG, error amp, and comparator. The PWM period is the operating frequency of the design with a DC set to the maximum permissible for the design. The PWM signal is directed to the COG as both rising & falling events. The COG is configured in half bridge mode so that the 'A' and 'B' outputs provide the HS & LS gate drive signals respectively.

The master PWM signal is also directed to the PRG as rising & falling events. The PRG is configured as a rising ramp and provides the timing signal against which the error amp value is compared to control HS DC.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A
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C
D
E
MASTER-PWM
TRIGGER
OUT
FE
100kHz
RE
Rising Event (RE): start of period.
Falling Event (FE): HS duty cycle limit.
PERIOD-RE/2.1B
VOLTAGE_SENSE-IN
DAC2
VREF OUT
Output Vref
OPA1
Error Amp
CMP1
COG1
Half Bridge mode
RE1
FE1
FE2
RE2
RE3
FE3
A
B
C
D
HS_GATE_DRIVE/2.4B
LS_COG/2.6C
Current Sense Vref
VREF OUT
DAC1
CMP2
CURRENT_SENSE-IN
DAC3
PRG1
FE1
RE1
VREF
HS on-time
FE2
RE2
PRG Vref
PRG-VREF/2.1C
Synchronous buck modulator core peripheral configuration for PIC16F1769.
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A conventional error amp (PIC op amp) is used to generate a correction value to the inverting input of the comparator. The non-inverting input connects to the PRG output and produces a falling event signal for the COG to terminate the HS on-time.

Fixed Voltage Reference (FVR) and Digital Analog Converters (DAC) provide the reference voltages for the PRG and error amp. The PRG ramp begins at 0V so a 5-bit DAC is used. The error-amp uses a 10-bit for more granularity.

Low Side Control

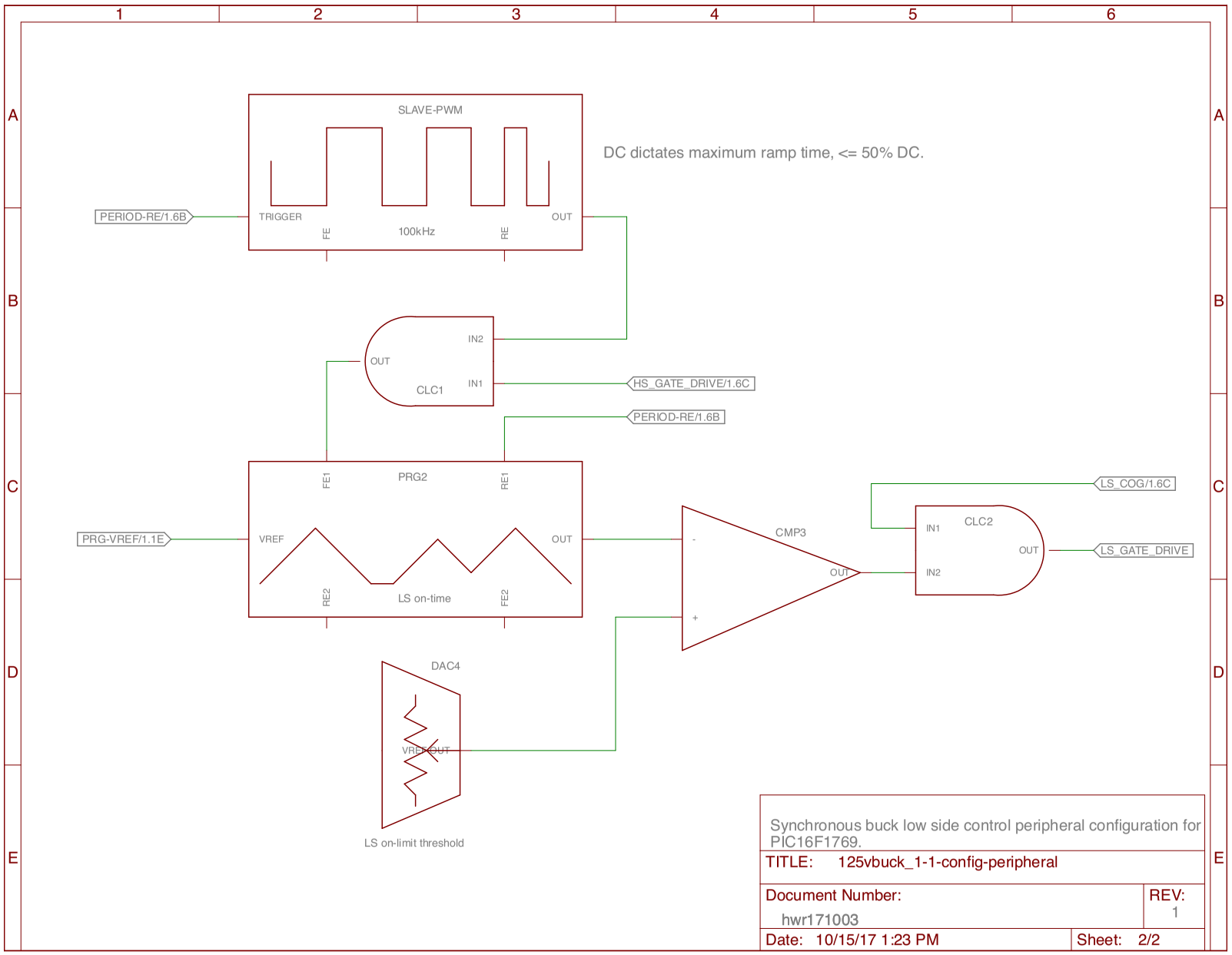
The modulator core provides timing to coordinate LS function. LS consists of a slave PWM, two Configurable Logic Cells (CLC), a second PRG, and second comparator (CMP-2).

The slave PWM is synchronized to the master and has the same period. The DC of the slave is set to a value less than 50% to limit the rising ramp. This is necessary to ensure that the falling portion of the ramp will have sufficient time to fully discharge (e.g. reset) by the end of the period. The PWM output is routed to an input of CLC-1 which is configured as a 2-input AND gate. The second input is connected to the COG 'A' (HS) signal. So the CLC-1 output will only be TRUE when both COG 'A' & slave PWM are TRUE. This provides the Falling Event (FE) signal to PRG-2.

PRG-2 is configured as a rising / falling ramp. The Rising Event (RE) is the master PWM. The FE from CLC-1 ensures that the ramp begins to discharge no later than at 50% DC. PRG-2's ramp is also referenced to 0V and so uses the same 5-bit DAC as the modulator PRG.

PRG-2's output connects to the inverting input of CMP-2. The non-inverting input connects to a DAC voltage reference. This reference value can be adjusted to terminate the LS on-time prior to the ramp being completely discharged.

The LS gate drive signal comes from CLC-2 and not the COG. Also configured as an 2-input AND gate, CLC-2 takes CMP-2 as one input and the COG LS as the other. The output connects to the LS gate driver. This is necessary to ensure that the LS signal is only active when the HS has terminated since CMP-2's output will be TRUE while the ramp is charging (e.g. rising).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A
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SLAVE-PWM
DC dictates maximum ramp time, <= 50% DC.
PERIOD-RE/1.6B
TRIGGER
OUT
FE
100kHz
RE
IN2
OUT
CLC1
IN1
HS_GATE_DRIVE/1.6C
PERIOD-RE/1.6B
FE1
PRG2
RE1
PRG-VREF/1.1E
VREF
OUT
RE2
LS on-time
FE2
LS_COG/1.6C
CLC2
IN1
OUT
LS_GATE_DRIVE
IN2
CMP3
-
OUT
+
DAC4
VREF OUT
LS on-limit threshold
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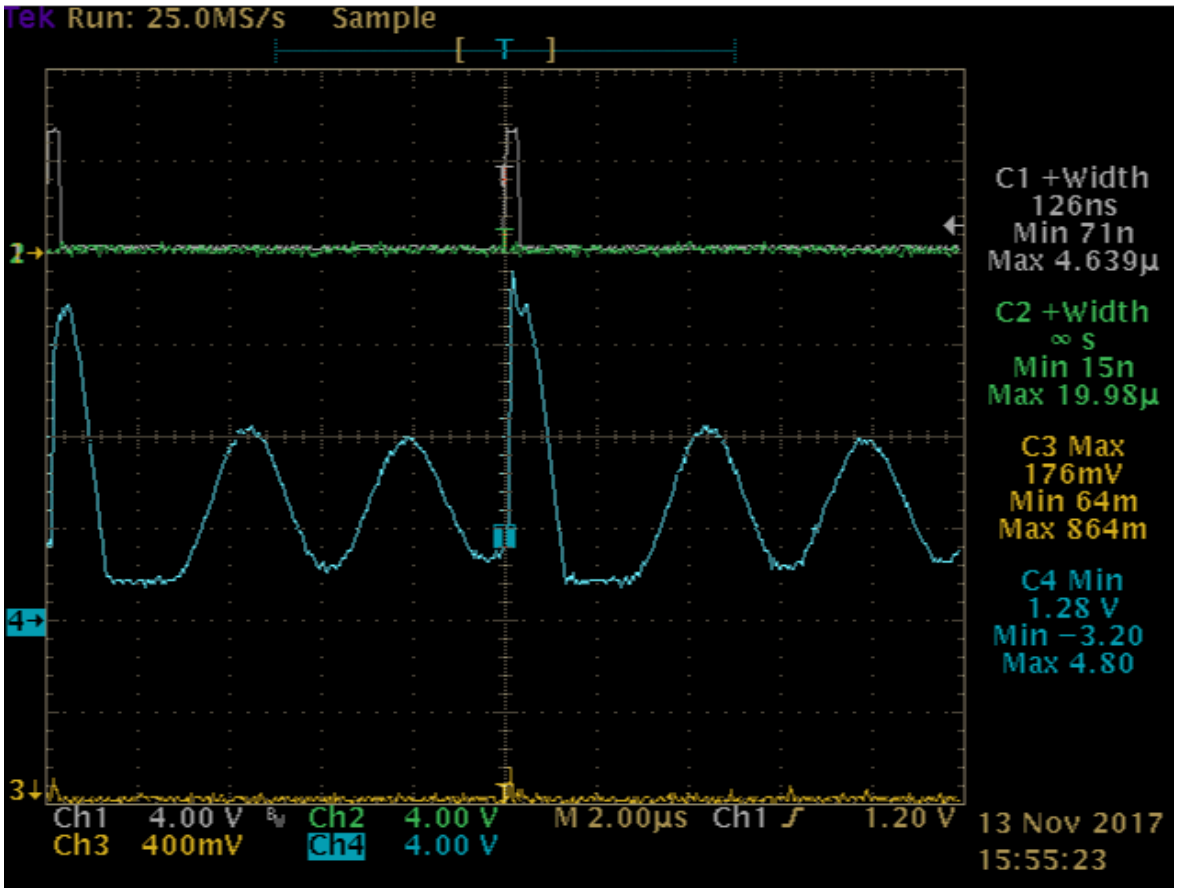
Validation

This approach was employed in a working design documented in 125vbuck_1-1-theory_of_operation.docx. This should be reviewed first to fully understand this discussion.

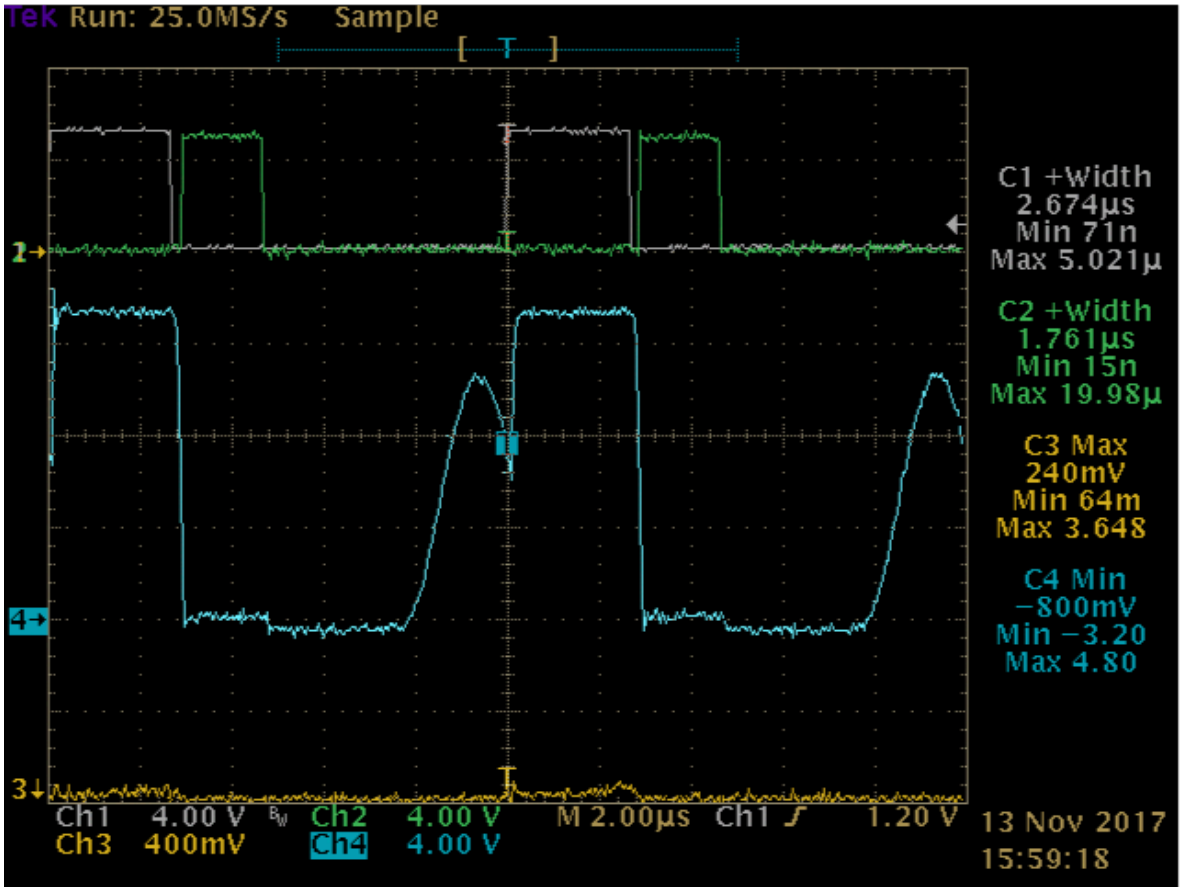
A series of scope measurements were taken to observe performance across the operating spectrum. Channel assignments:

- 1=HS measured at gate driver logic input
- 2=LS measured at gate driver logic input
- 3=current sense signal measured at controller input
- 4=inductor voltage measured across the LS switch (e.g. D-S with S=GND)

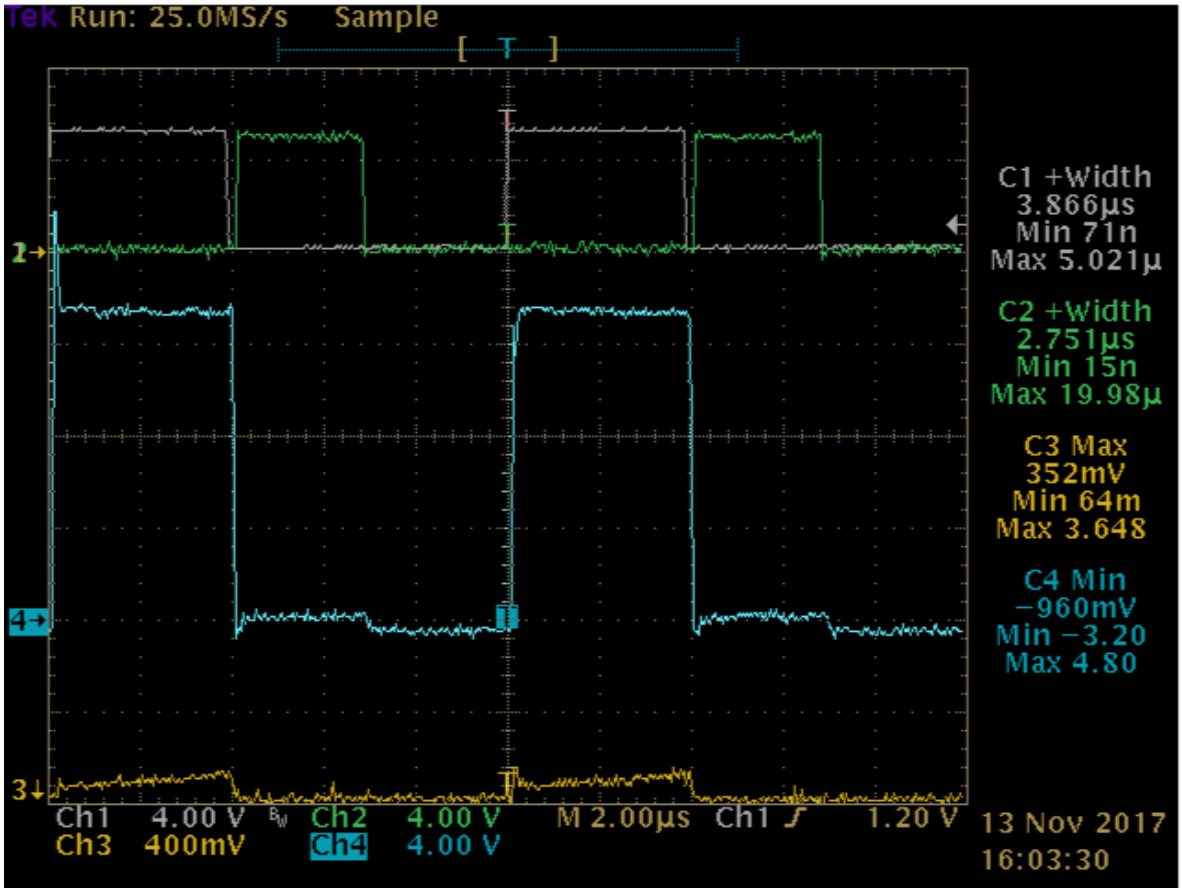
At no load the inductor is discontinuous as is the modulator. Hence, LS conduction time is zero. This is an efficient mode of operation since there is no power demand at the output.



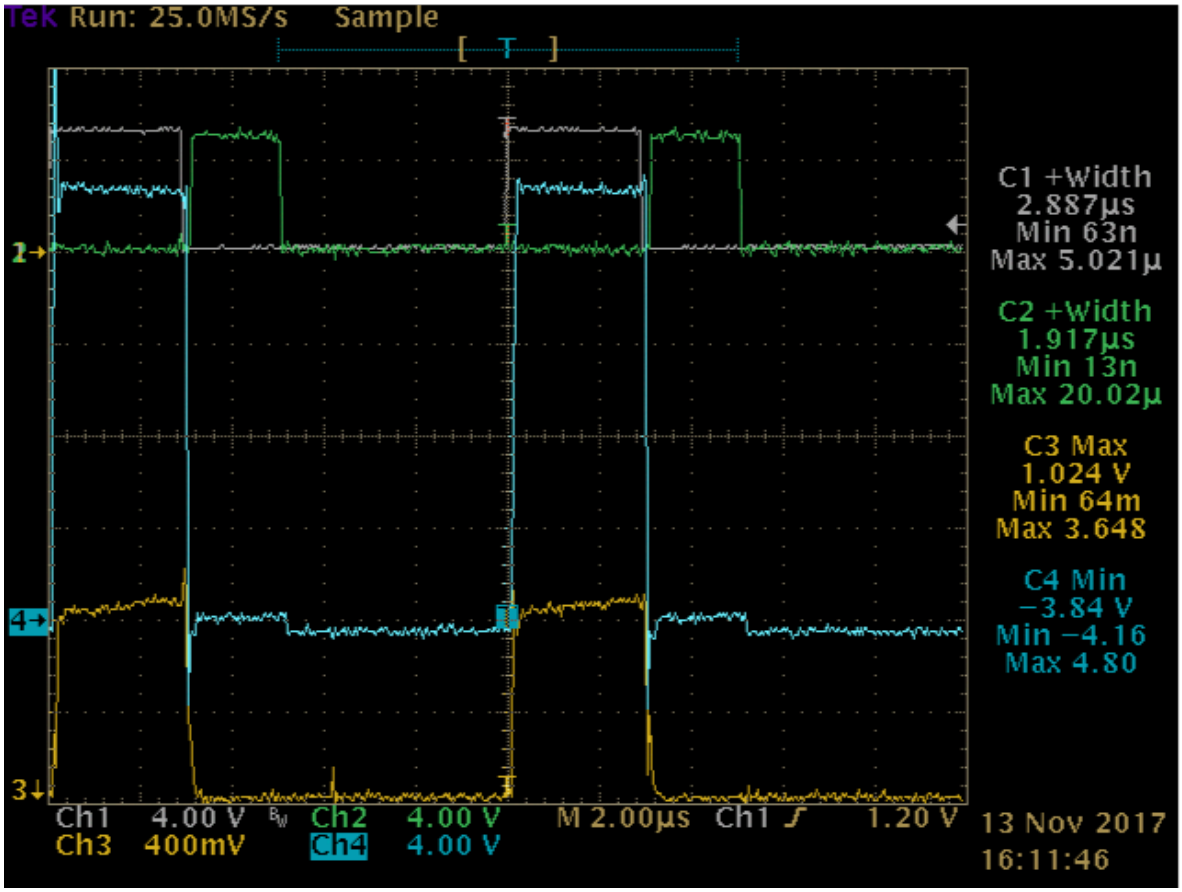
With a 100mA load the inductor is still discontinuous but the LS is not conducting long enough. Note that channel four goes negative when the LS switch turns off due to the increased impedance of the LS body diode. This represents a small loss of approximately $IE(\frac{Tc(LSoff)}{T}$ 24mW where $T_{c(LSoff)}$ is the time the inductor continues to discharge while the LS switch is off and T is the switching time in uS.



With a 500mA load the inductor is in continuous conduction mode. LS on-time has increased but, due to the symmetrical timing relationship with the HS the conduction time is insufficient. This is particularly pronounced in this PS design since the inductor was designed for continuous conduction (starting at ~ 200mA) and a maximum HS duty cycle of ~ 4.7uS when at full load and low line input. The loss is now ~ 144mW.

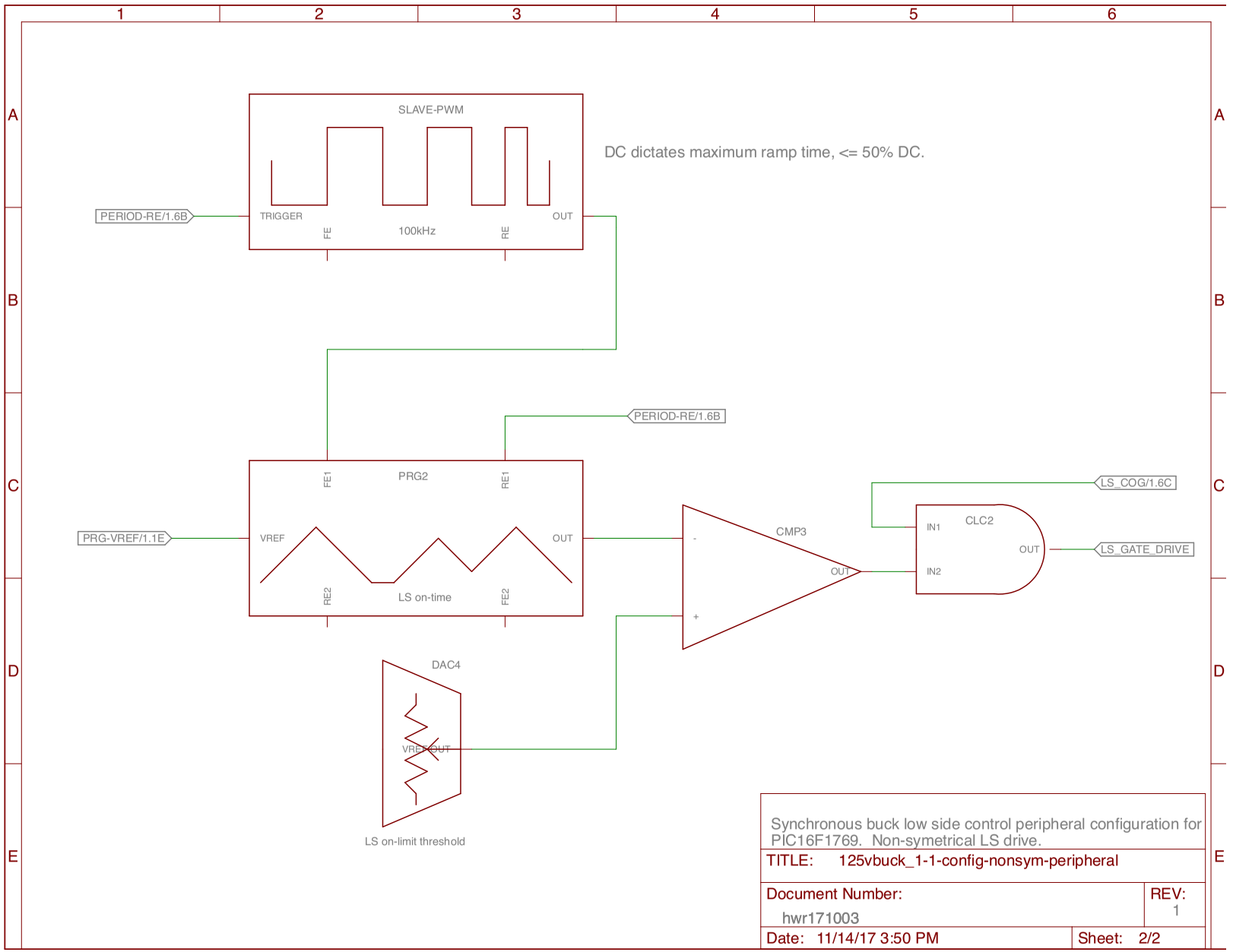


At maximum load (5A) and the input line close to maximum (19V DC) the losses induced by symmetrical LS drive are more pronounced. Here they are ~ 2.25W. Note that the C4 Min voltage was not used for this calculation since that is likely ground bounce; rather the transistor data sheet's body diode forward voltage, Vsd, of one volt was used. This corresponds to the observed rise above ambient of the LS switch of 45C (measured with FLIR thermometer).



These results demonstrate that symmetrical control is acceptable with larger HS on-times (e.g. smaller difference between input & output voltages). It would likely work well in a discontinuous design but that was not evaluated.

For the PS that this scheme was evaluated in the losses were deemed unacceptable due to the losses at higher input voltages and power levels. The LS on-time needed to be increased to reduce conduction losses.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A
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SLAVE-PWM
TRIGGER
OUT
FE
100kHz
RE
PERIOD-RE/1.6B
DC dictates maximum ramp time, <= 50% DC.
PERIOD-RE/1.6B
FE1
PRG2
RE1
PRG-VREF/1.1E
VREF
OUT
RE2
LS on-time
FE2
CMP3
-
+
OUT
LS_COG/1.6C
CLC2
IN1
IN2
OUT
LS_GATE_DRIVE
DAC4
VREF
OUT
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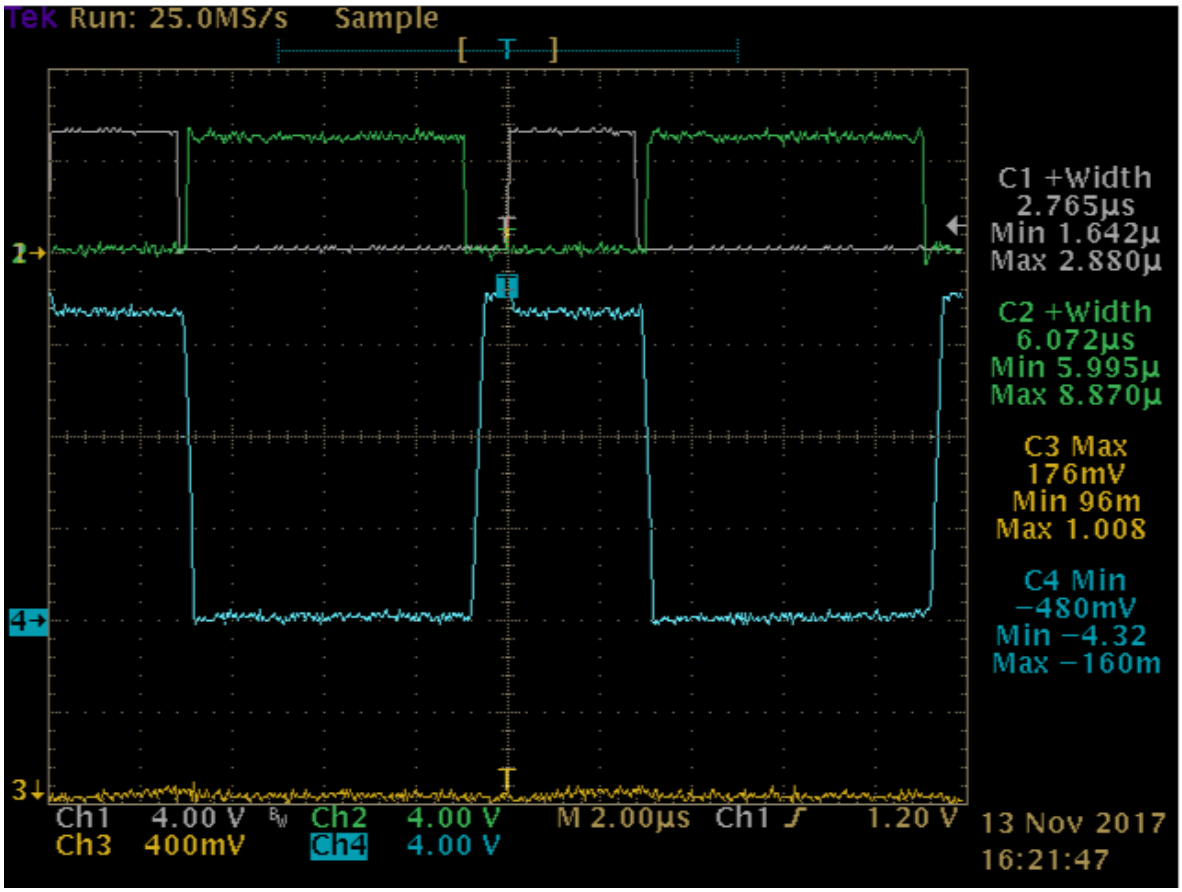
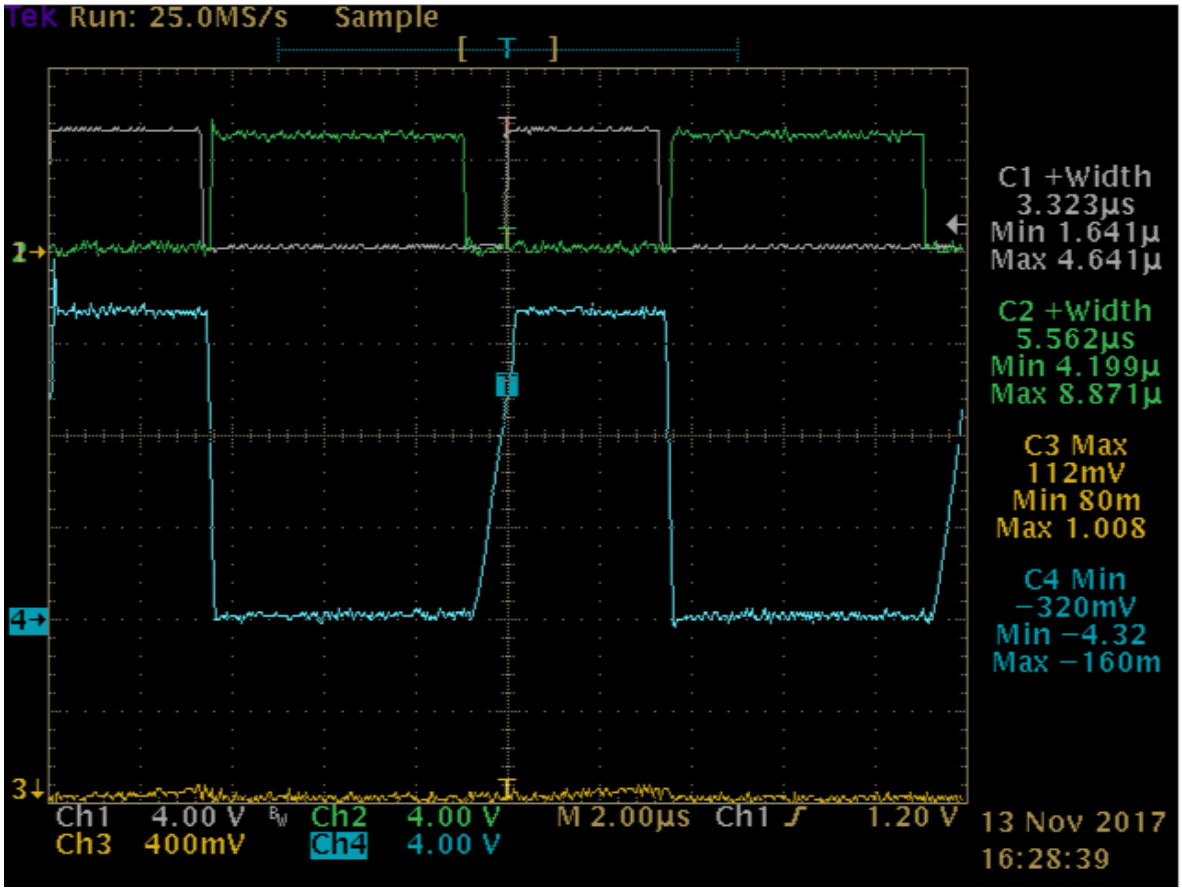
A simple modification was made to the LS peripheral logic in the PIC: the CLC1 AND gate was removed and the slave PWM connected directly to PRG2's falling event input. This effectively extended the LS on-time for the entire time available to the LS across the load spectrum. In practice, the LS needs to be terminated prior to the end of the period as a compromise for improved light load efficiency; DAC4's value was adjusted to terminate the LS at 1µS.

At the onset there was concern that this approach could cause problems, particularly when the inductor was discontinuous, by discharging the output filter capacitor and possible ringing. The PS controller was updated with revised software and the same set of tests were repeated.

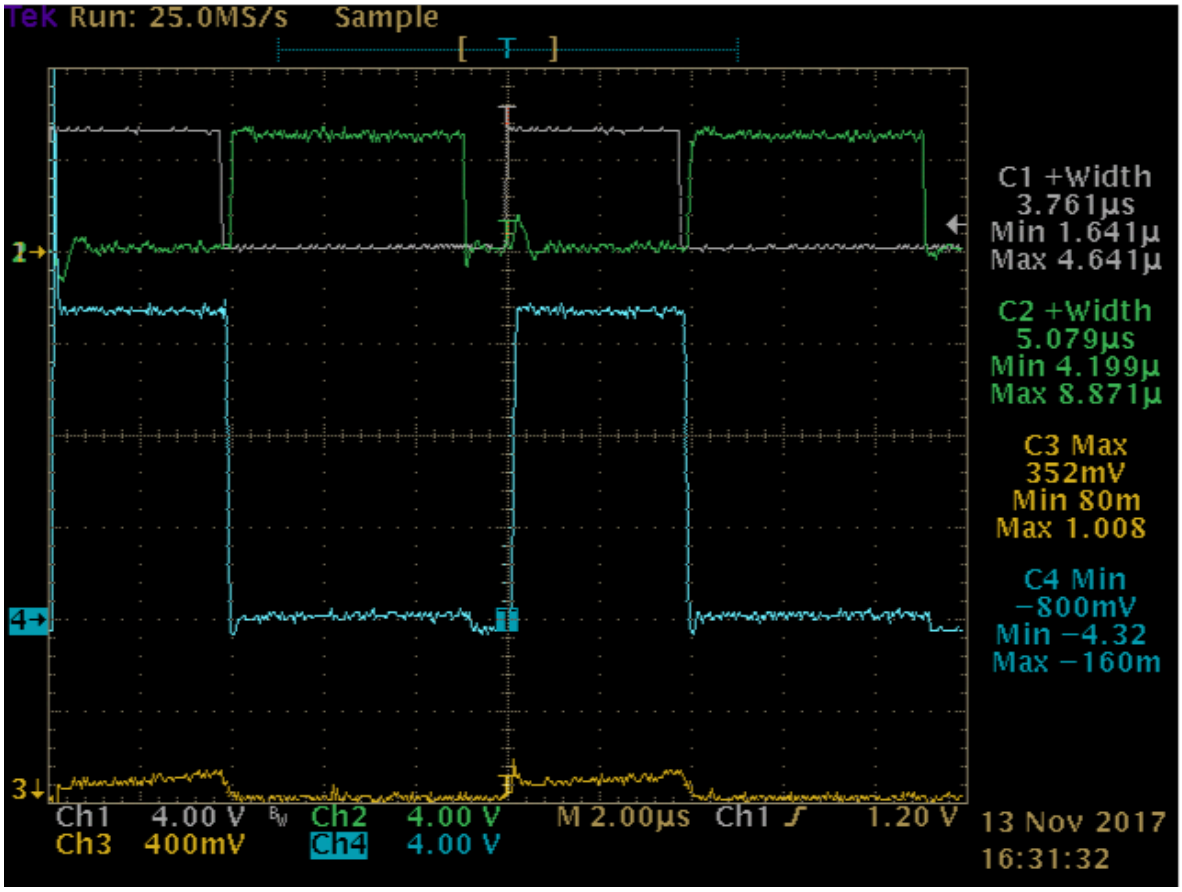
At no load there is no ring but a small lip appears on the inductor's input pin when the LS switches off that suggests some energy had started flowing from the output capacitor back into the inductor. The small bump in the current sense signal (CH 3) confirms this since it isn't seen on the symmetrical no-load test. Efficiency testing data shows that the worst-case loss is 67mW although this doesn't account for other power-consuming modifications made (inrush bypass relay).



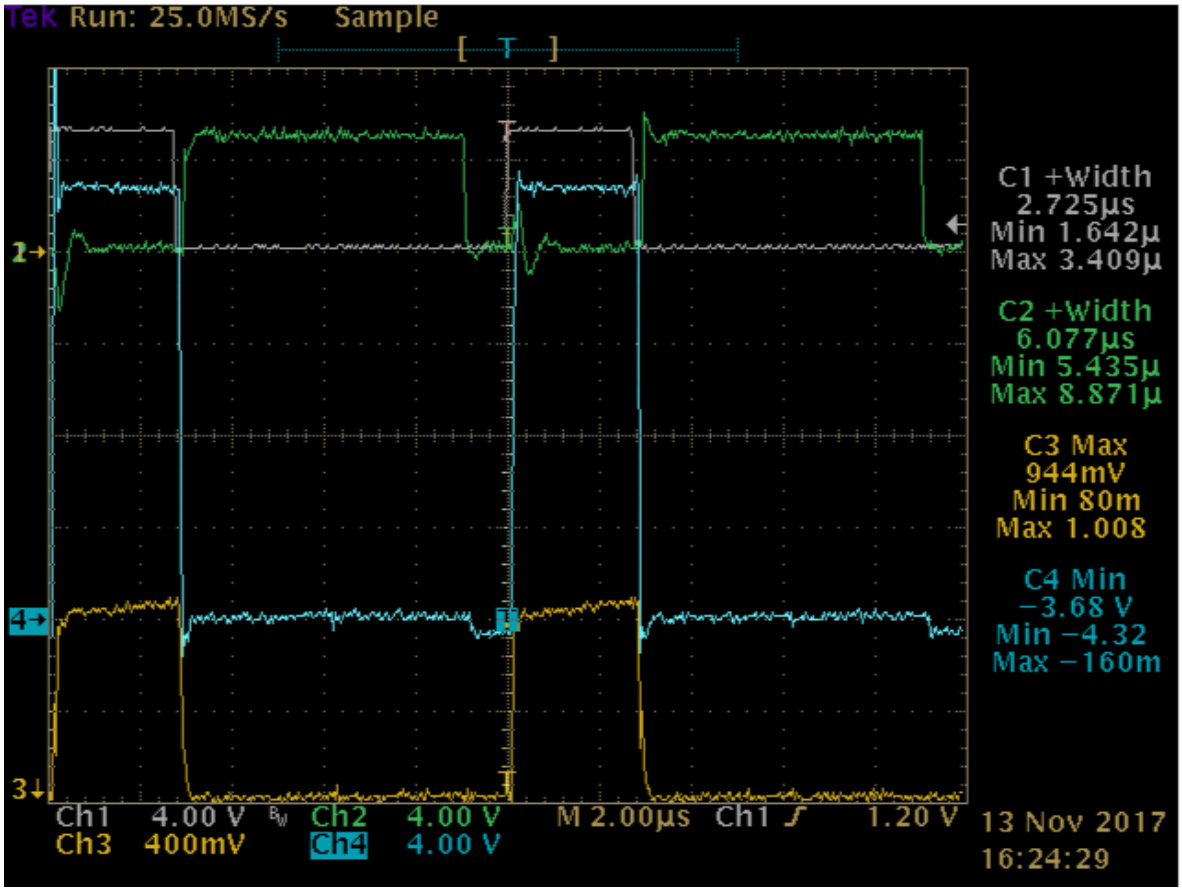
At 100mA the inductor is still discontinuous but there is still an estimated loss of 53mW (using efficiency data). Note that the LS is no longer going negative since adequate conduction time is provided.



At 500mA the inductor is continuous and does go negative for the short time that the LS is off prior to the start of the next duty cycle. Using the formula from the symmetrical measurements the loss is ~ 40mW.



With a 5A load at high line input the duty cycle is 162nS shorter than the symmetrical drive and loses due to body diode conduction at the end of the LS on-time are only 500mW; a significant improvement. The LS switch confirms this with a temperature rise above ambient of only 25C.



Conclusion

Testing shows that the basic scheme is viable. In the PS that this scheme was tested in overall efficiencies as high as 92% were achieved at moderate and higher loads without the need for cooling or heat sinks. Which scheme is most appropriate depends on the conduction mode chosen for the inductor.

Additional refinement may be possible. A third option, combining both approaches depending on operating regime would improve operating efficiencies across the operating spectrum. But to do so without requiring additional hardware the following must happen:

- The DAC controlling LS termination must be freed up; instead use the slave PWM to control LS by adjusting DC
- Validate that the comparator will reliably terminate the LS by using ground reference only; if not then an additional external voltage reference will be required

- Configure another comparator to monitor current sense against the DAC: this defines the threshold for switching between operating schemes (based on when inductor moves from discontinuous)
- Monitor comparator state in the SW run loop and reconfigure scheme as appropriate – a hysteresis algorithm would be employed

In circuit testing must be performed to validate. Depending on the design, a software table or transfer function may also be required that 'slides' the slave PWM DC based on input voltage or other factors. Without additional hardware to supplement the scheme will not be perfect; and if going that far then a reliable LS current sense should be implemented to provide a precise method for LS control.

Last, be sure that the hardware design can safely accommodate a software failure to properly switch modes.

Summary

This approach demonstrates that a general purpose microcontroller, equipped with suitable on-board peripherals, can implement synchronous buck capability in either discontinuous or continuous modes without external components or active software intervention.