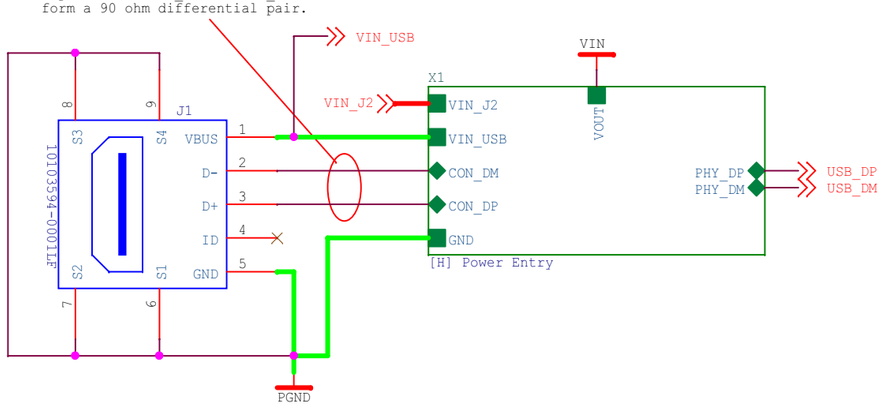
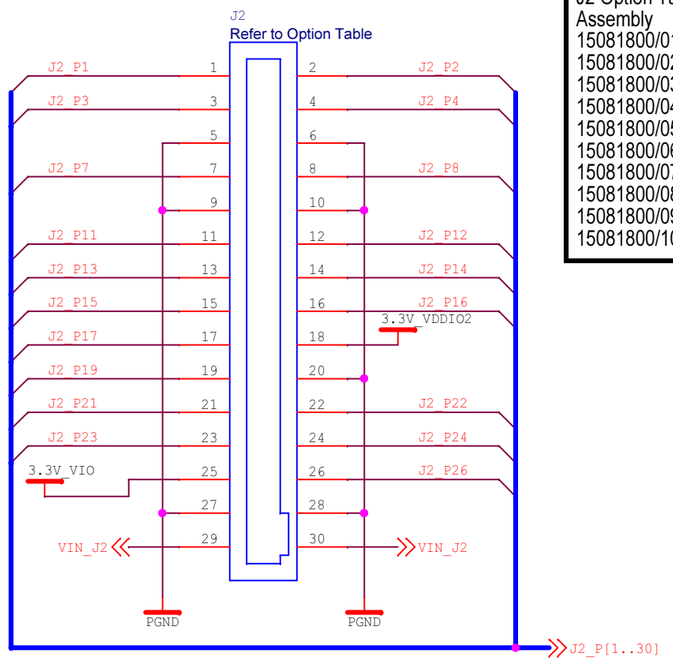
Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha 2 Prototype	00001	09/01/2015	JJW	BEH
3	Beta 3 Prototype	00007	04/26/2016	JJW	BEH
4	Gamma 4 Prototype	00010	07/11/2016	JJW	BEH
4.1	snickerdoodle blue	00014	10/25/2016	JJW	BEH
4.11	Layout corrections	000xx	1/10/2018	JJW	BEH

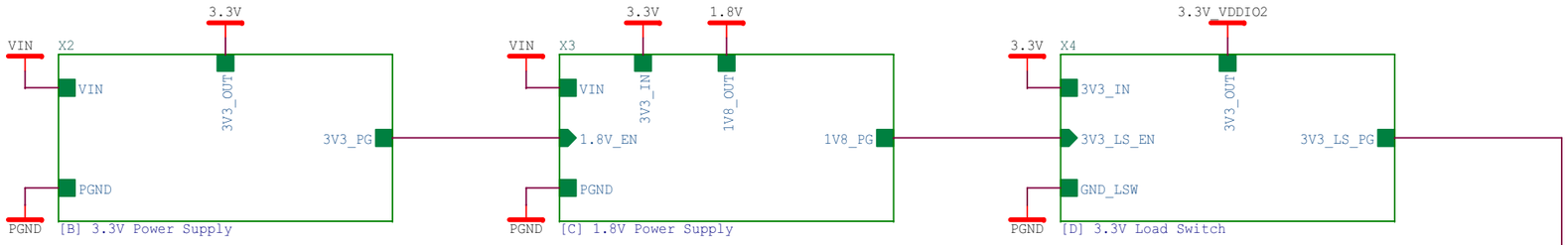
Power/JTAG/SWD/BT Audio/I2C/DAC/ADC

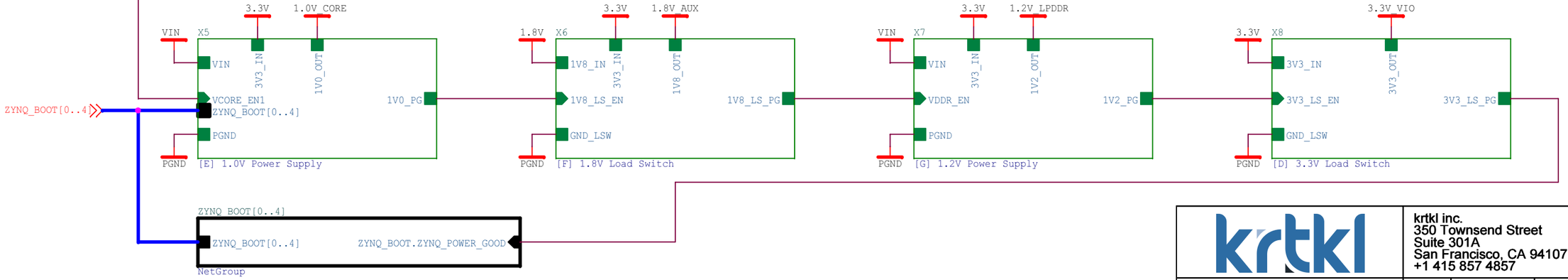
Layout Note: CON_DP and CON_DM
form a 90 ohm differential pair.





J2 Option Table	
Assembly	Part Number
15081800/01-22	TFM-115-01-F-D-A
15081800/02-22	SFM-115-L3-F-D-A
15081800/03-22	TFM-115-01-F-D-A
15081800/04-22	SFM-115-L3-F-D-A
15081800/05-22	TFM-115-01-F-D-A
15081800/06-22	SFM-115-L3-F-D-A
15081800/07-22	SFM-115-L3-F-D-A
15081800/08-22	SFM-115-L3-F-D-A
15081800/09-22	TFM-115-01-F-D-A
15081800/10-22	SFM-115-L3-F-D-A





Minimum Trace Ratings	
	6000mA
	4000mA
	2000mA
	1000mA
	200mA

Minimum Plane Ratings	
+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA

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	NAME	DATE
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CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 1 OF 30

Warning: snickerdoodle rev 3 and earlier have 1.8V on pin 1 and an unconnected pin 3. Please confirm compatibility of 3.3V default on pin 1 and 1.8V on pin 3 prior to connection of external hardware.

J3 Option Table

Assembly	Part Number
15081800/01-22	TFM-120-01-F-D-A
15081800/02-22	SFM-120-L3-F-D-A
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	SFM-120-L3-F-D-A
15081800/09-22	TFM-120-01-F-D-A
15081800/10-22	SFM-120-L3-F-D-A

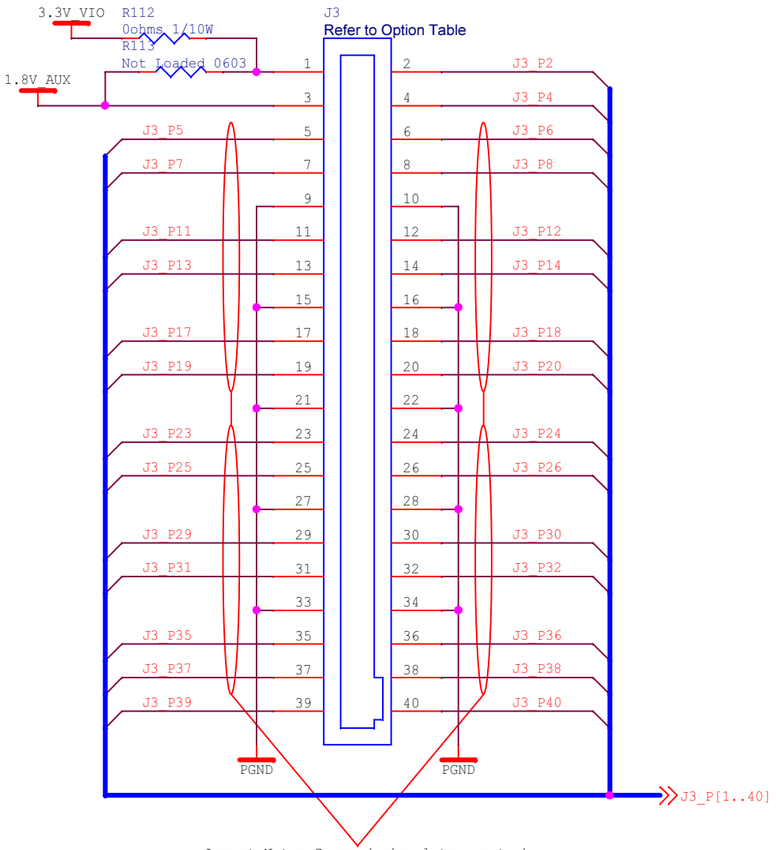
JC1 Option Table

Assembly	Part Number
15081800/01-22	Not Loaded
15081800/02-22	Not Loaded
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	Not Loaded
15081800/09-22	Not Loaded
15081800/10-22	Not Loaded

JA1 Option Table

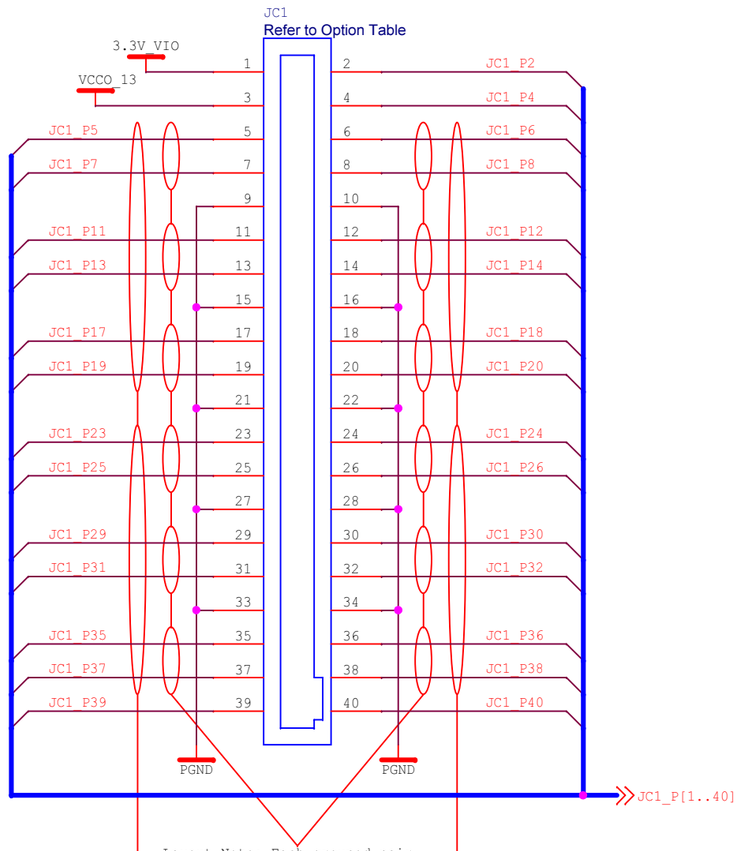
Assembly	Part Number
15081800/01-22	TFM-120-01-F-D-A
15081800/02-22	SFM-120-L3-F-D-A
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	SFM-120-L3-F-D-A
15081800/09-22	TFM-120-01-F-D-A
15081800/10-22	SFM-120-L3-F-D-A

CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN



Layout Note: Grouped signal traces to be length matched to within 5mils with 50ohm single-ended characteristic impedance.

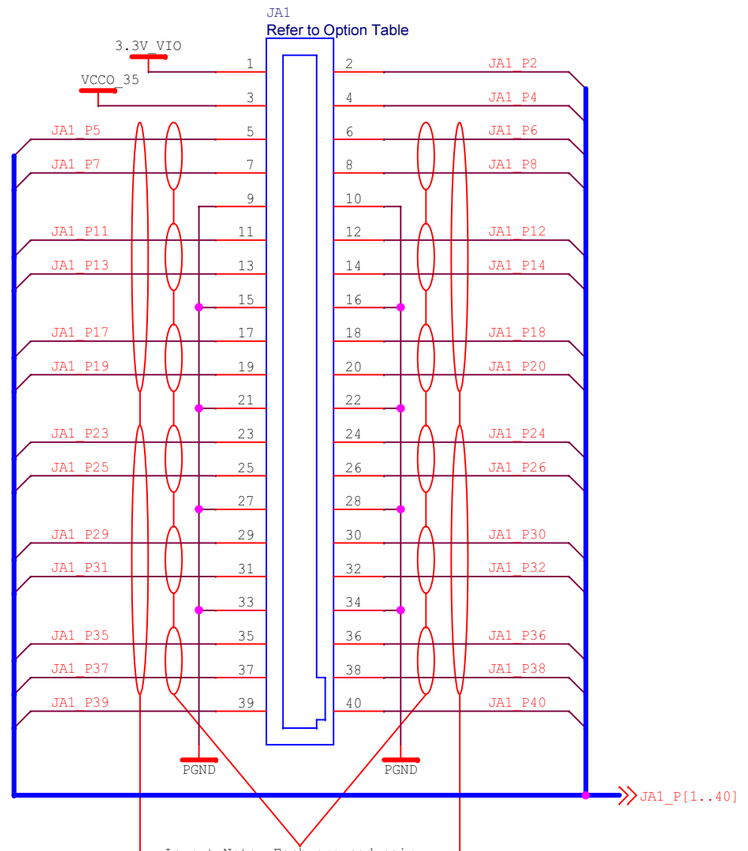
FPGA I/O



Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

FPGA I/O



Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

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	NAME	DATE
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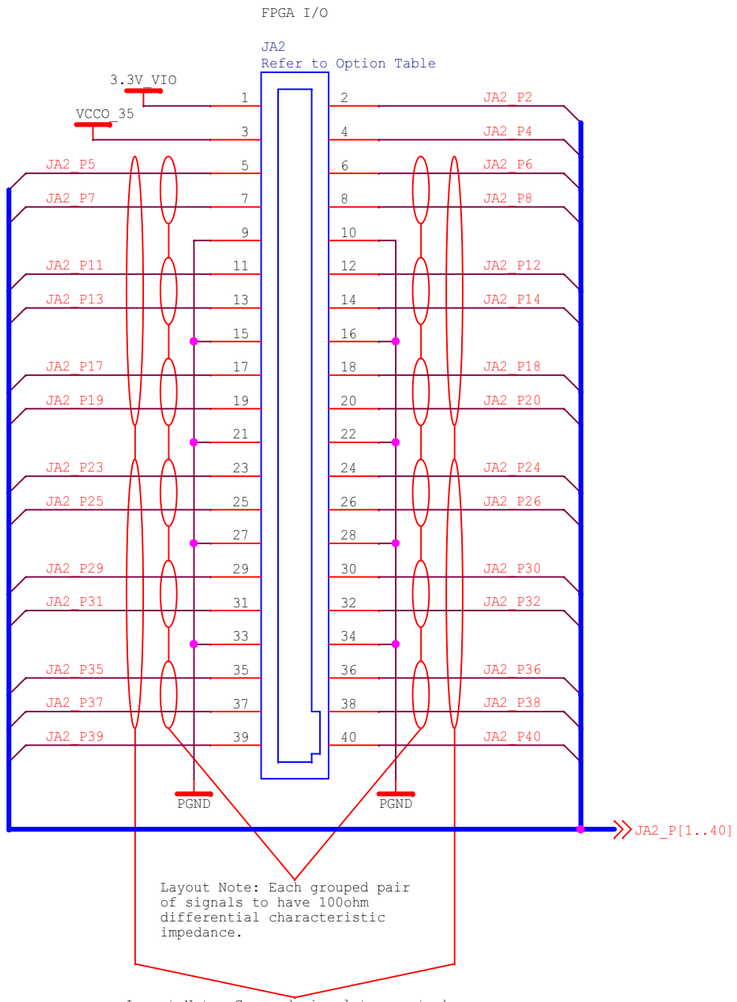
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

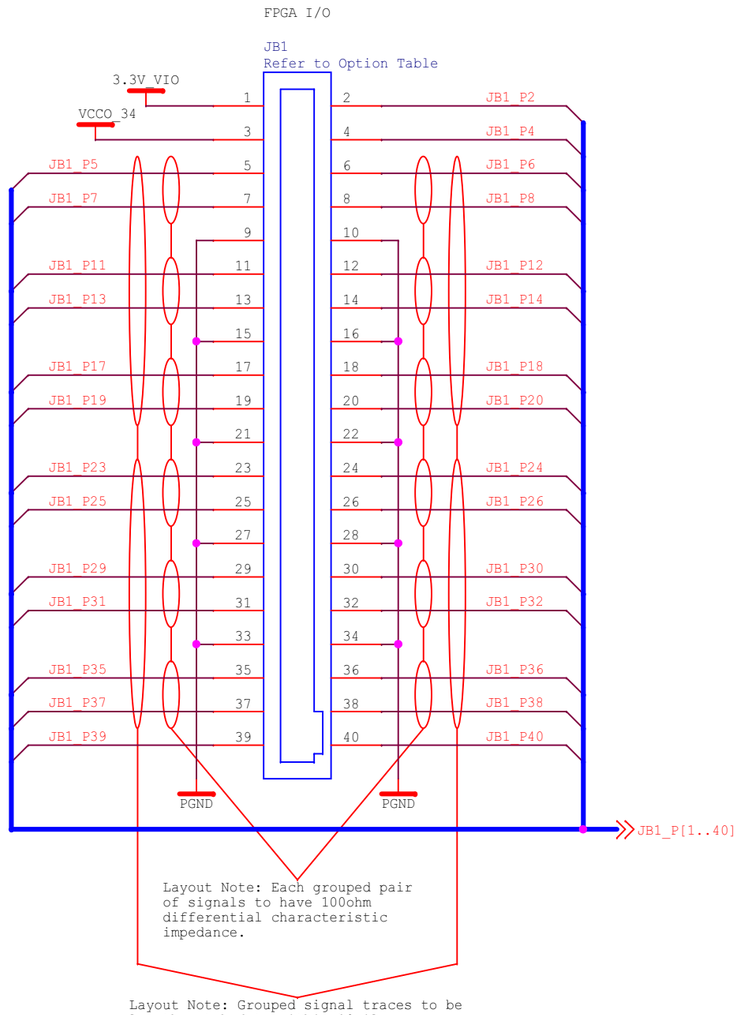
TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 2 OF 30

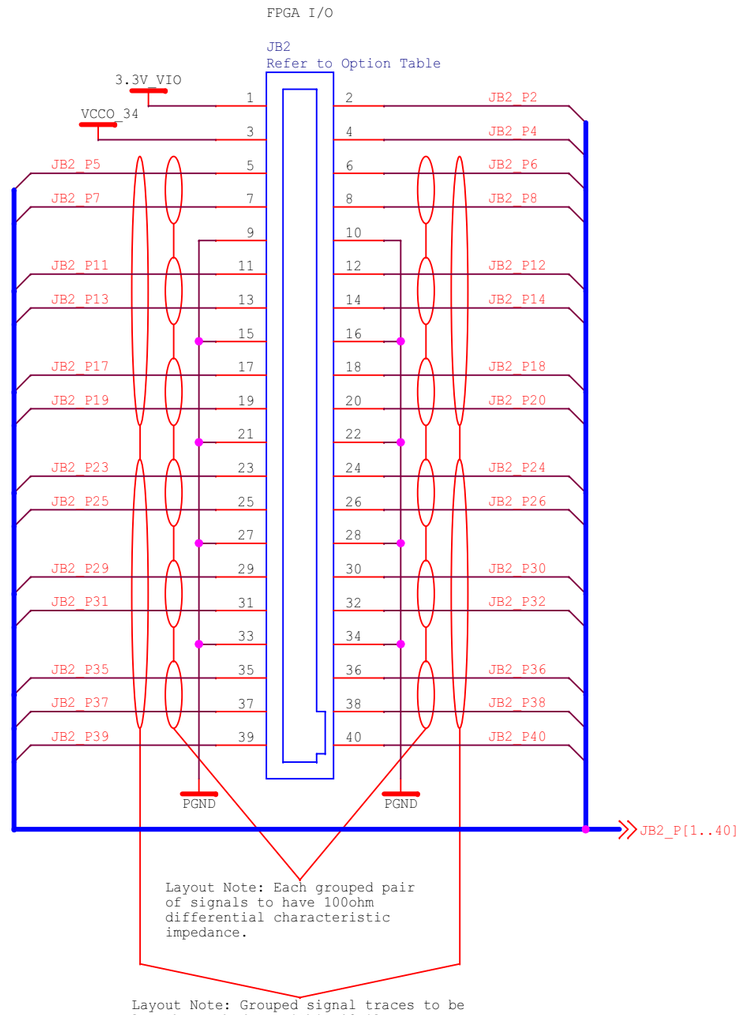
JA2 Option Table	
Assembly	Part Number
15081800/01-22	TFM-120-01-F-D-A
15081800/02-22	SFM-120-L3-F-D-A
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	SFM-120-L3-F-D-A
15081800/09-22	TFM-120-01-F-D-A
15081800/10-22	SFM-120-L3-F-D-A

JB1 Option Table	
Assembly	Part Number
15081800/01-22	TFM-120-01-F-D-A
15081800/02-22	SFM-120-L3-F-D-A
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	SFM-120-L3-F-D-A
15081800/09-22	TFM-120-01-F-D-A
15081800/10-22	SFM-120-L3-F-D-A

JB2 Option Table	
Assembly	Part Number
15081800/01-22	TFM-120-01-F-D-A
15081800/02-22	SFM-120-L3-F-D-A
15081800/03-22	TFM-120-01-F-D-A
15081800/04-22	SFM-120-L3-F-D-A
15081800/05-22	TFM-120-01-F-D-A
15081800/06-22	SFM-120-L3-F-D-A
15081800/07-22	SFM-120-L3-F-D-A
15081800/08-22	SFM-120-L3-F-D-A
15081800/09-22	TFM-120-01-F-D-A
15081800/10-22	SFM-120-L3-F-D-A







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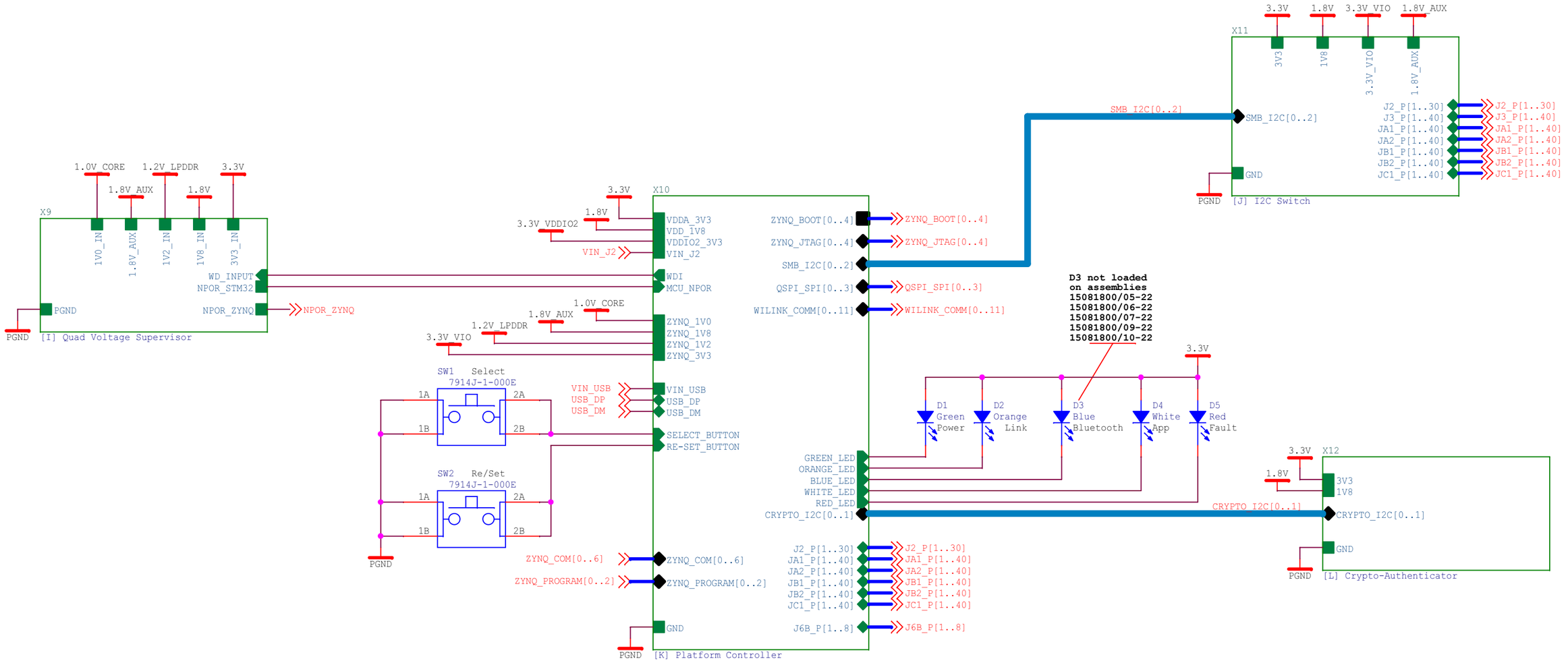
TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram

	NAME	DATE
DRAWN BY	J. Weatherbee	11/21/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 3 OF 30



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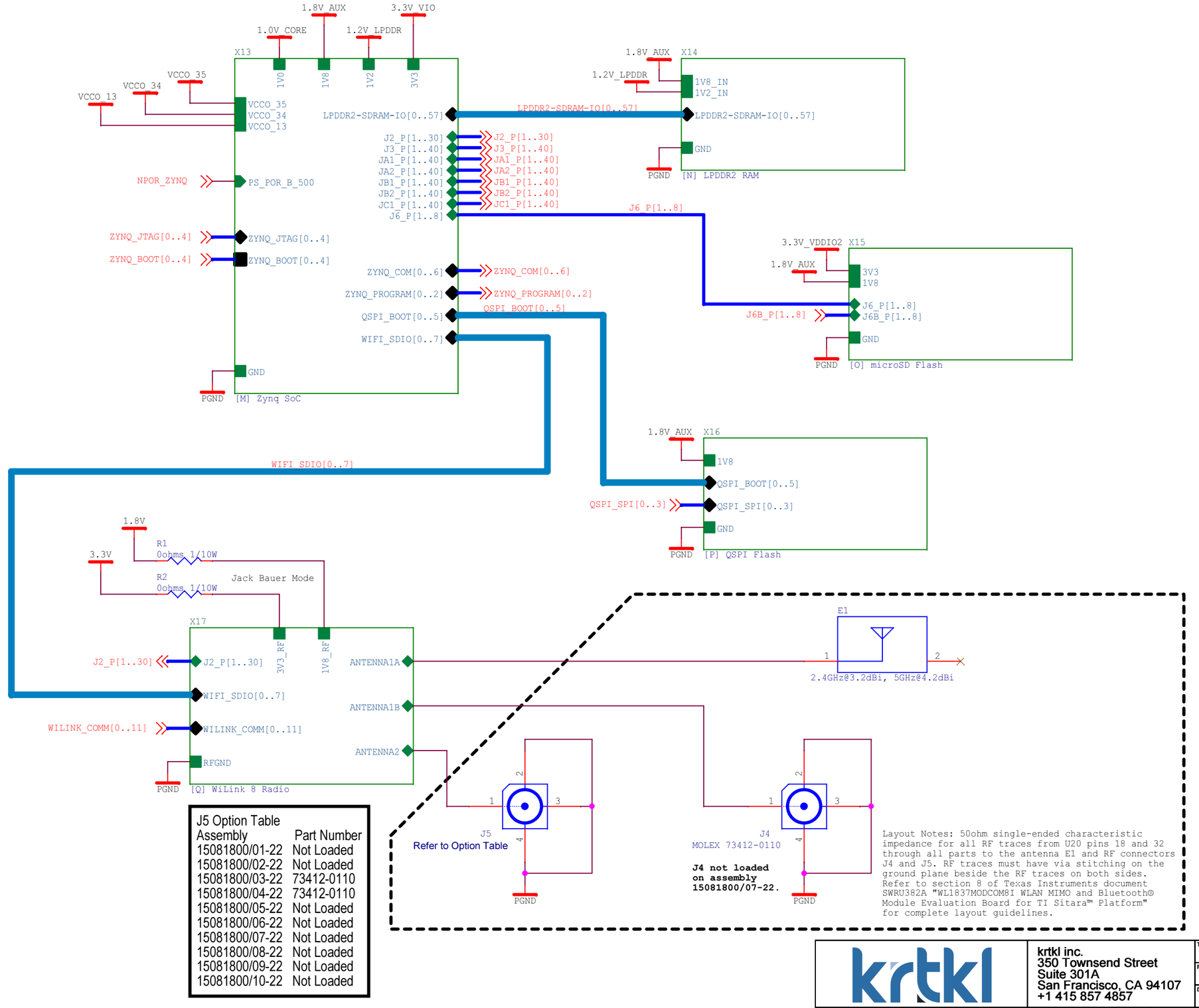
	NAME	DATE
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 4 OF 30



J5 Option Table	
Assembly	Part Number
15081800/01-22	Not Loaded
15081800/02-22	Not Loaded
15081800/03-22	73412-0110
15081800/04-22	73412-0110
15081800/05-22	Not Loaded
15081800/06-22	Not Loaded
15081800/07-22	Not Loaded
15081800/08-22	Not Loaded
15081800/09-22	Not Loaded
15081800/10-22	Not Loaded

Layout Notes: 50ohm single-ended characteristic impedance for all RF traces from U20 pins 18 and 32 through all parts to the antenna E1 and RF connectors J4 and J5. RF traces must have via stitching on the ground plane beside the RF traces on both sides. Refer to section 8 of Texas Instruments document SWRU382A "WL1837MODCOM8I WLAN MIMO and Bluetooth® Module Evaluation Board for TI Sitara™ Platform" for complete layout guidelines.

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	NAME	DATE
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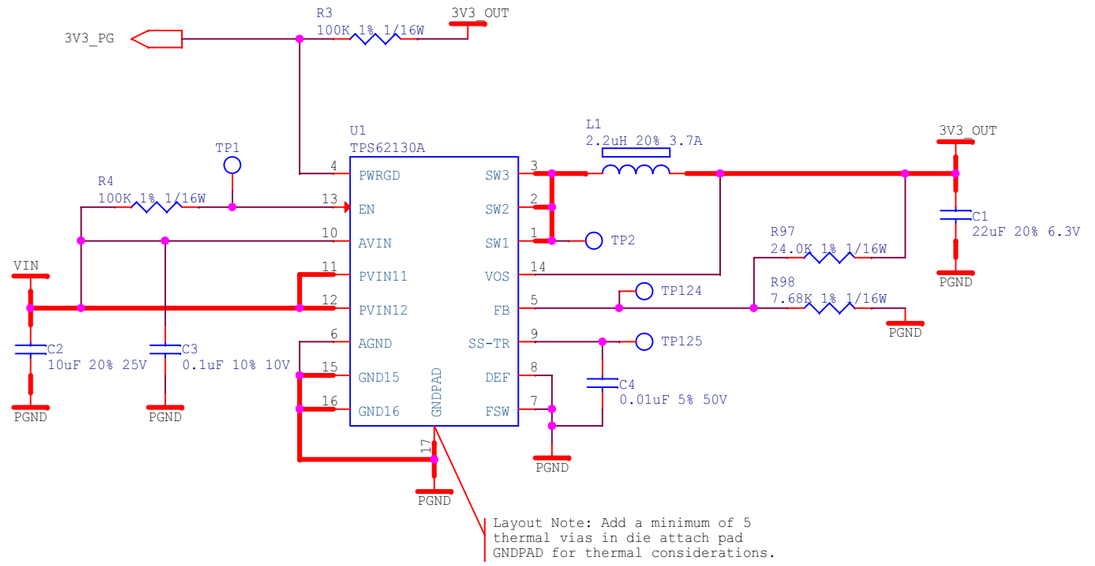
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 5 OF 30



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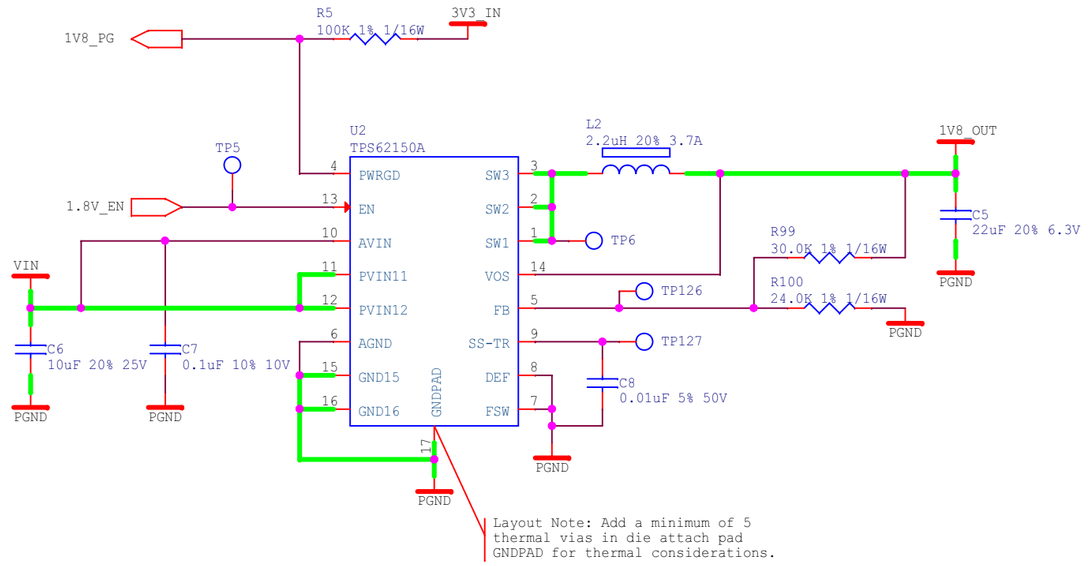
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X2
DESCRIPTION: 3.3V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 6 OF 30



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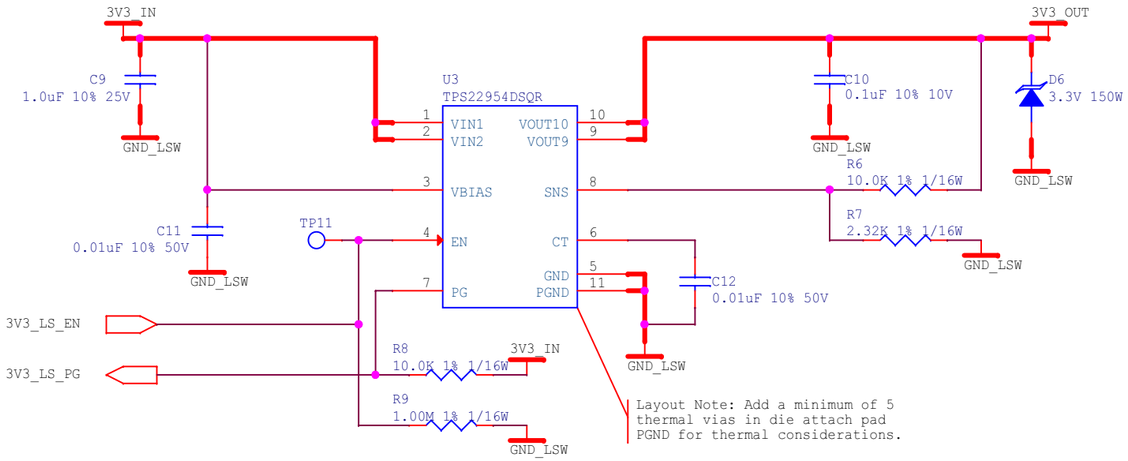
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X3
DESCRIPTION: 1.8V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 7 OF 30



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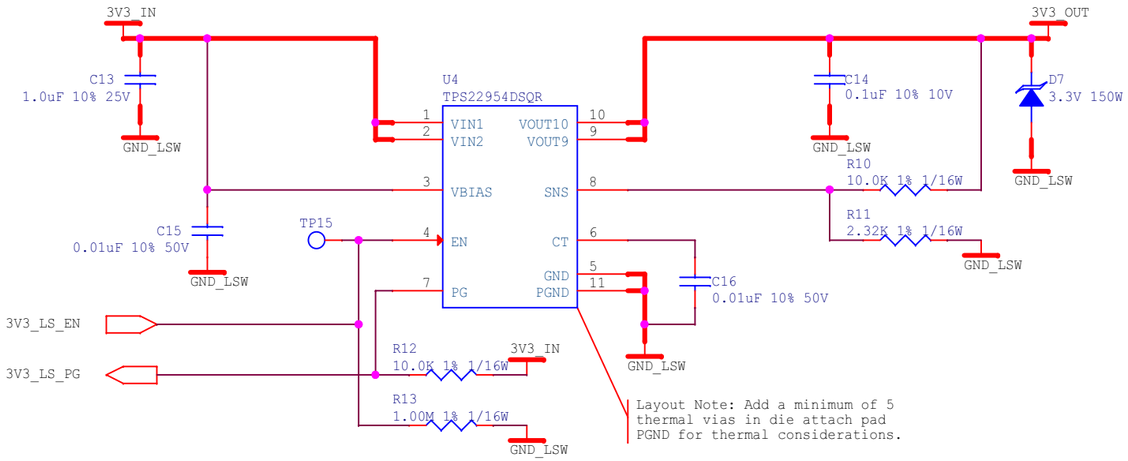
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X4
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 8 OF 30



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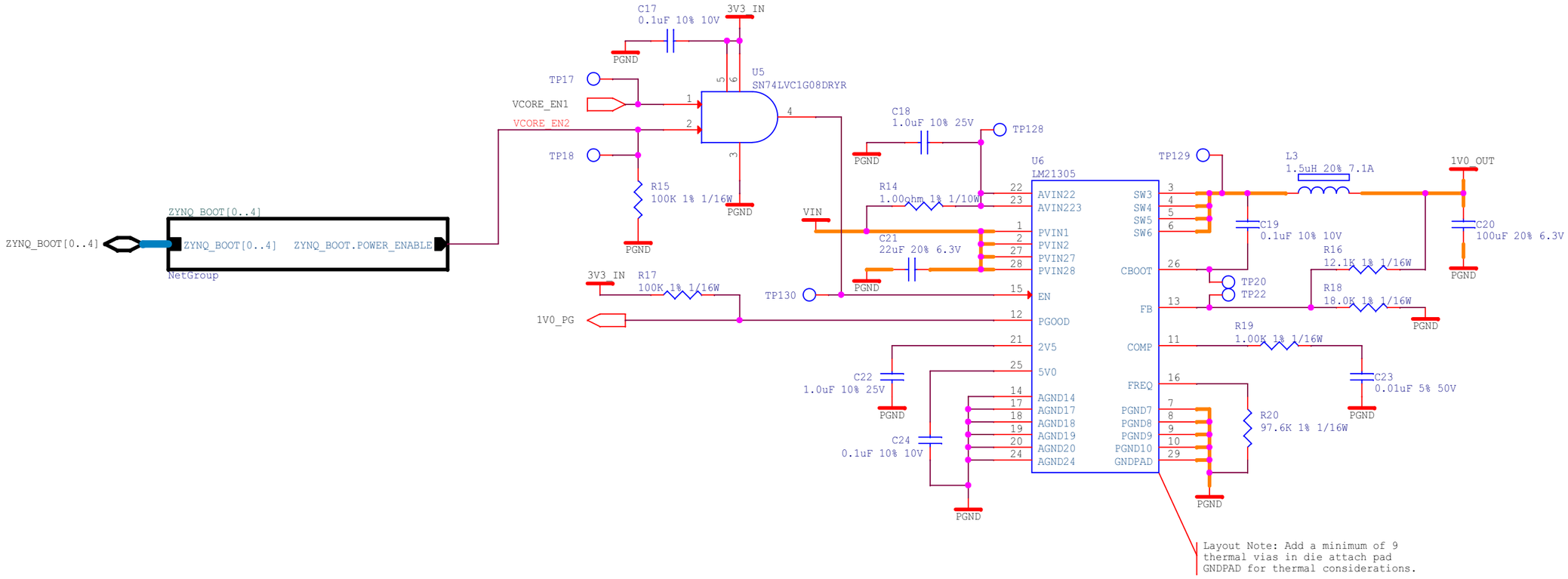
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X8
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 9 OF 30



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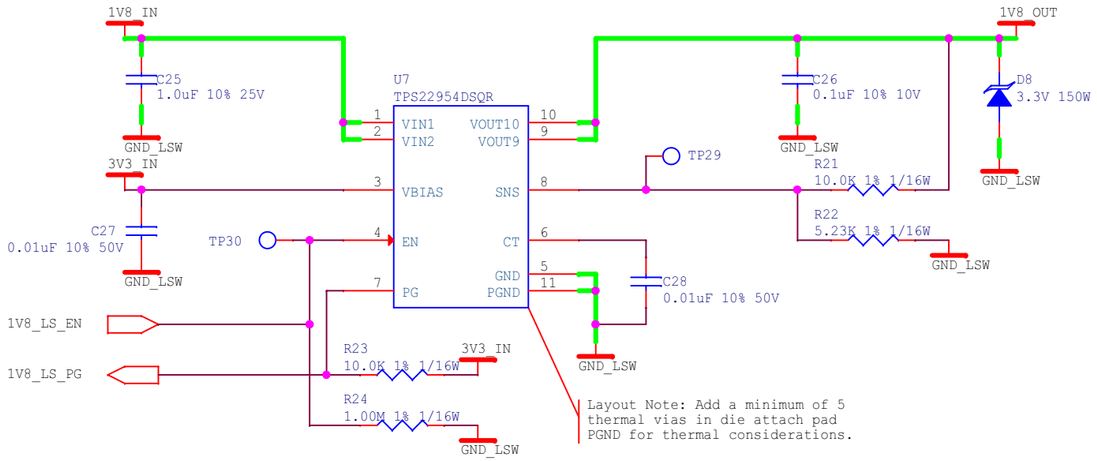
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X5
DESCRIPTION: 1.0V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 10 OF 30



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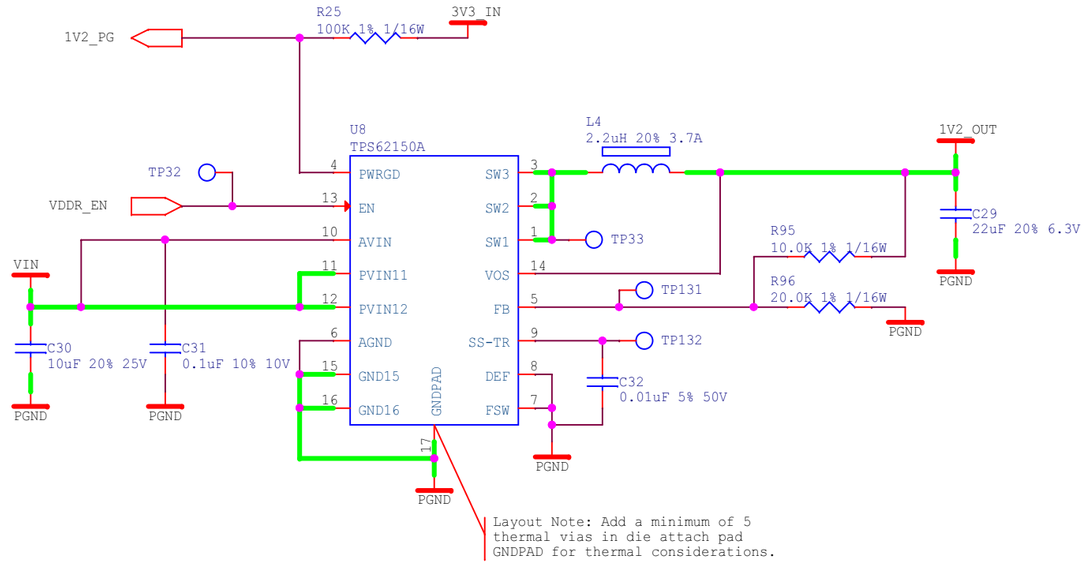
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X6
DESCRIPTION: 1.8V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 11 OF 30



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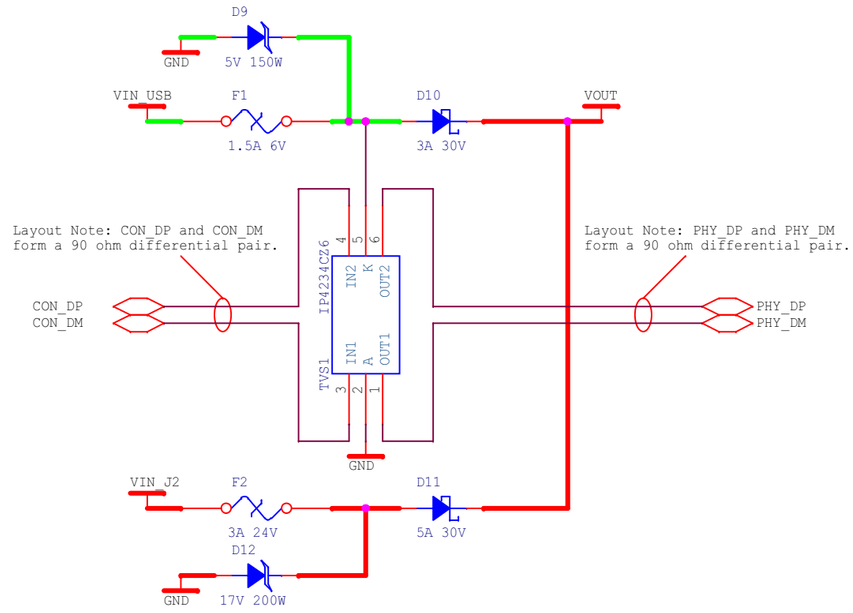
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X7
DESCRIPTION: 1.2V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 12 OF 30



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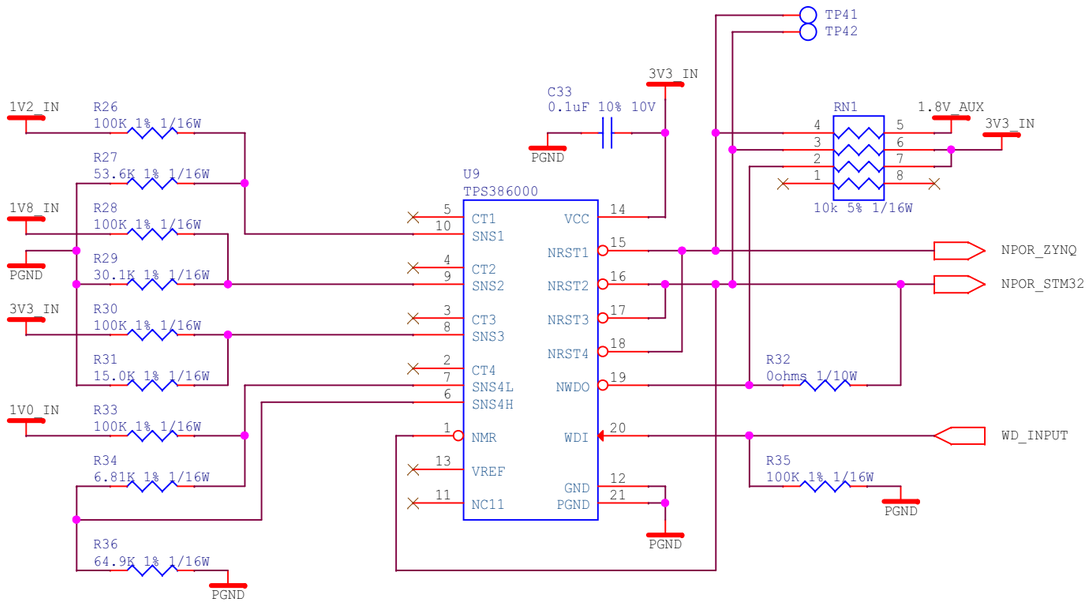
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X1
DESCRIPTION: Power Entry
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 13 OF 30



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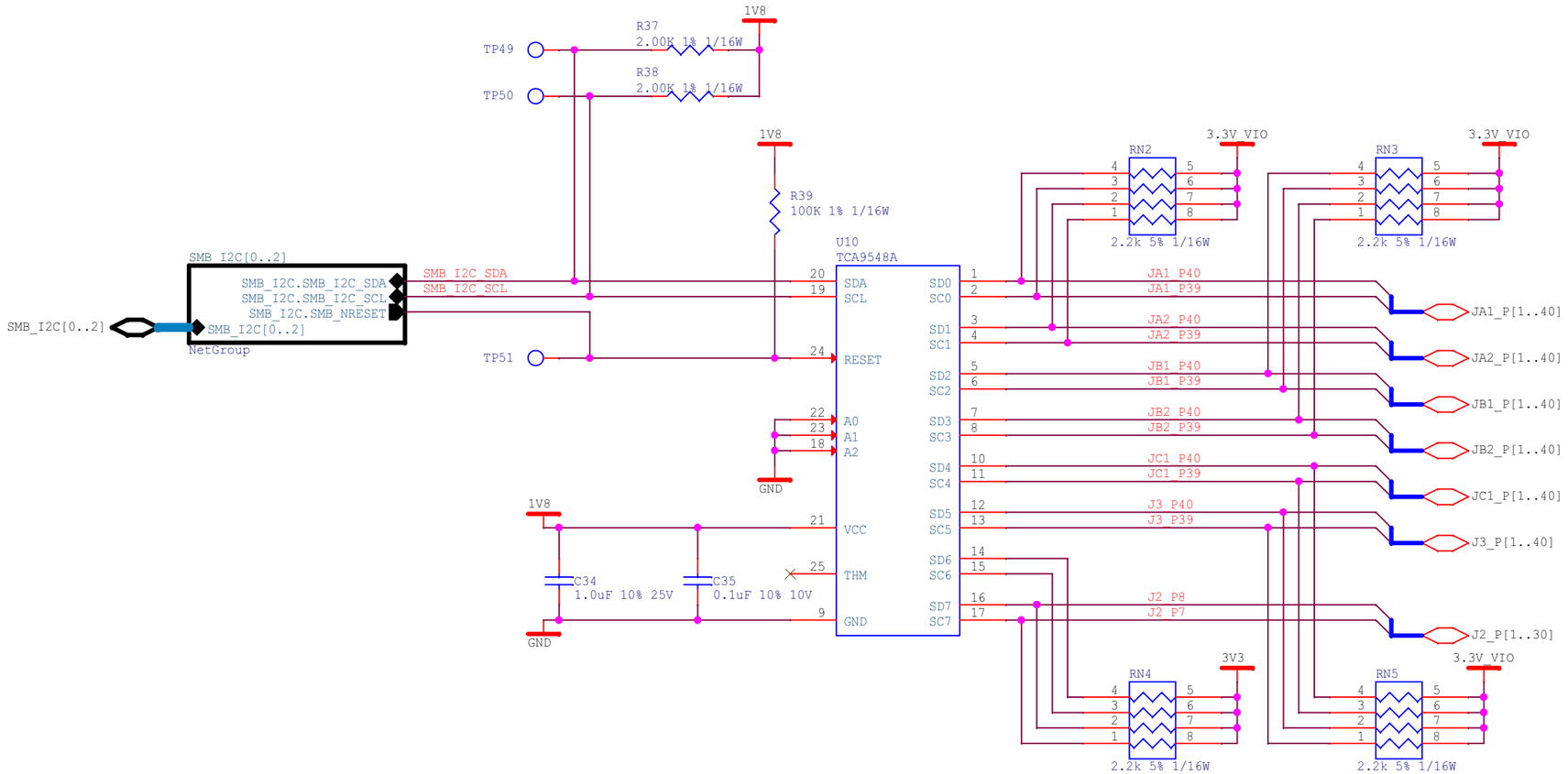
TITLE: snickerdoodle FPGA Module
PATH: /X9
DESCRIPTION: Quad Voltage Supervisor

	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 14 OF 30



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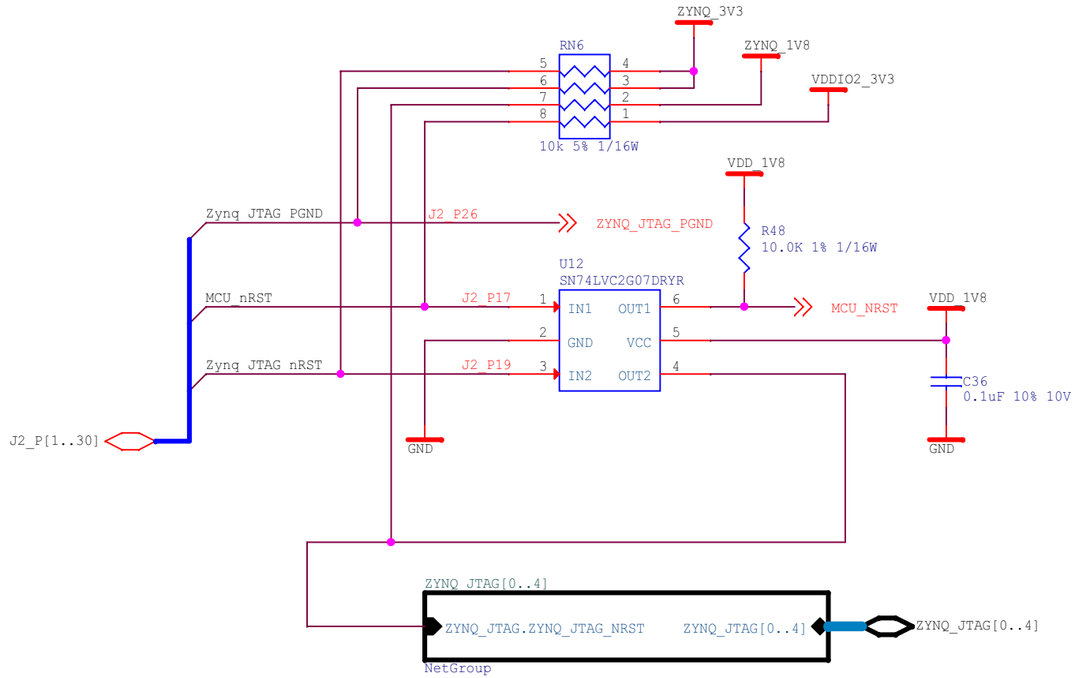
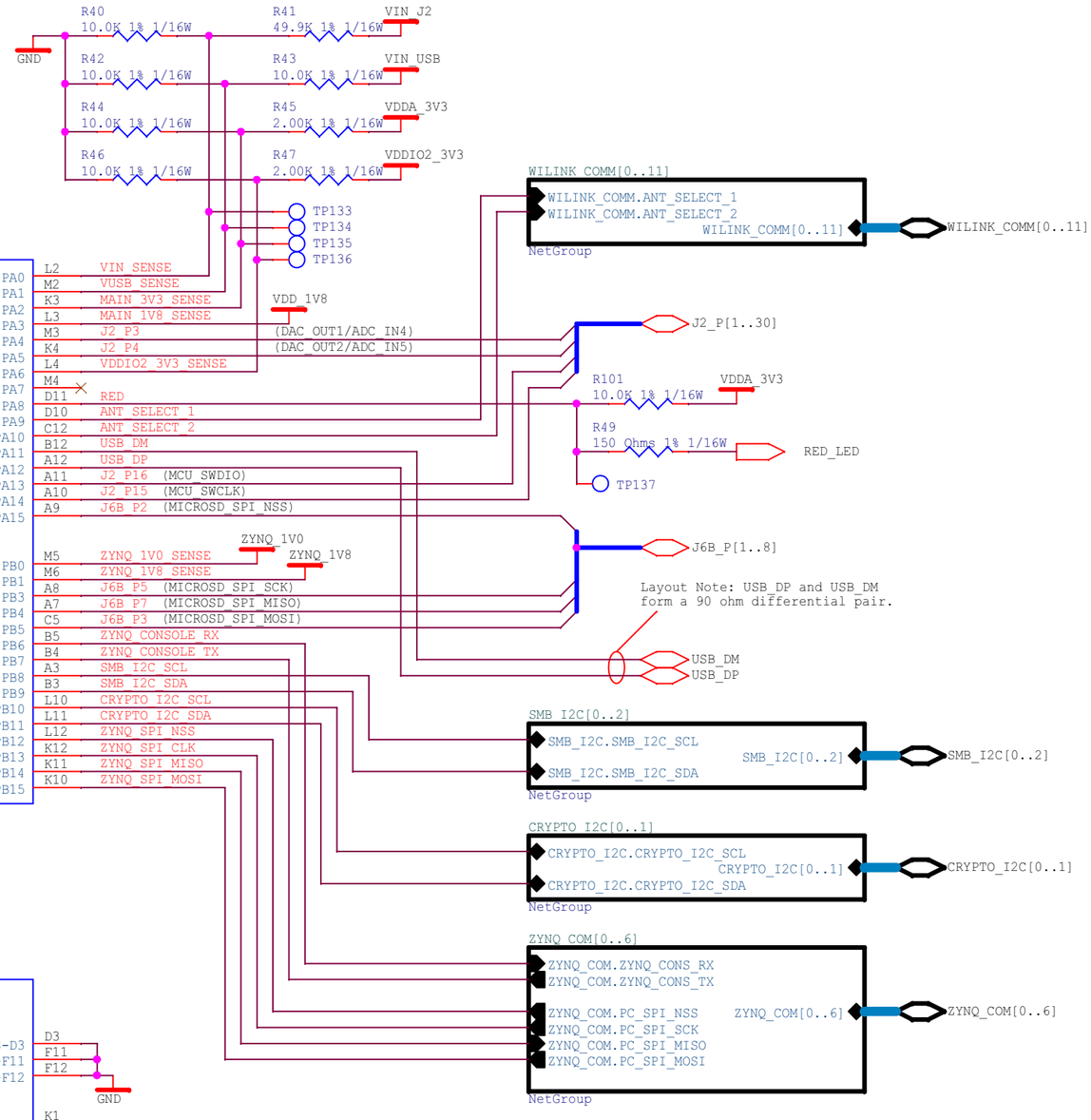
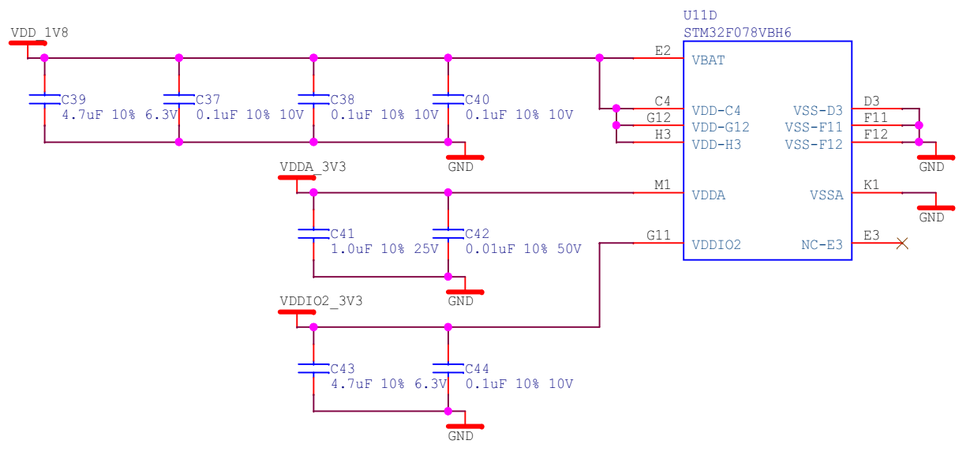
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X11
DESCRIPTION: I2C Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 15 OF 30







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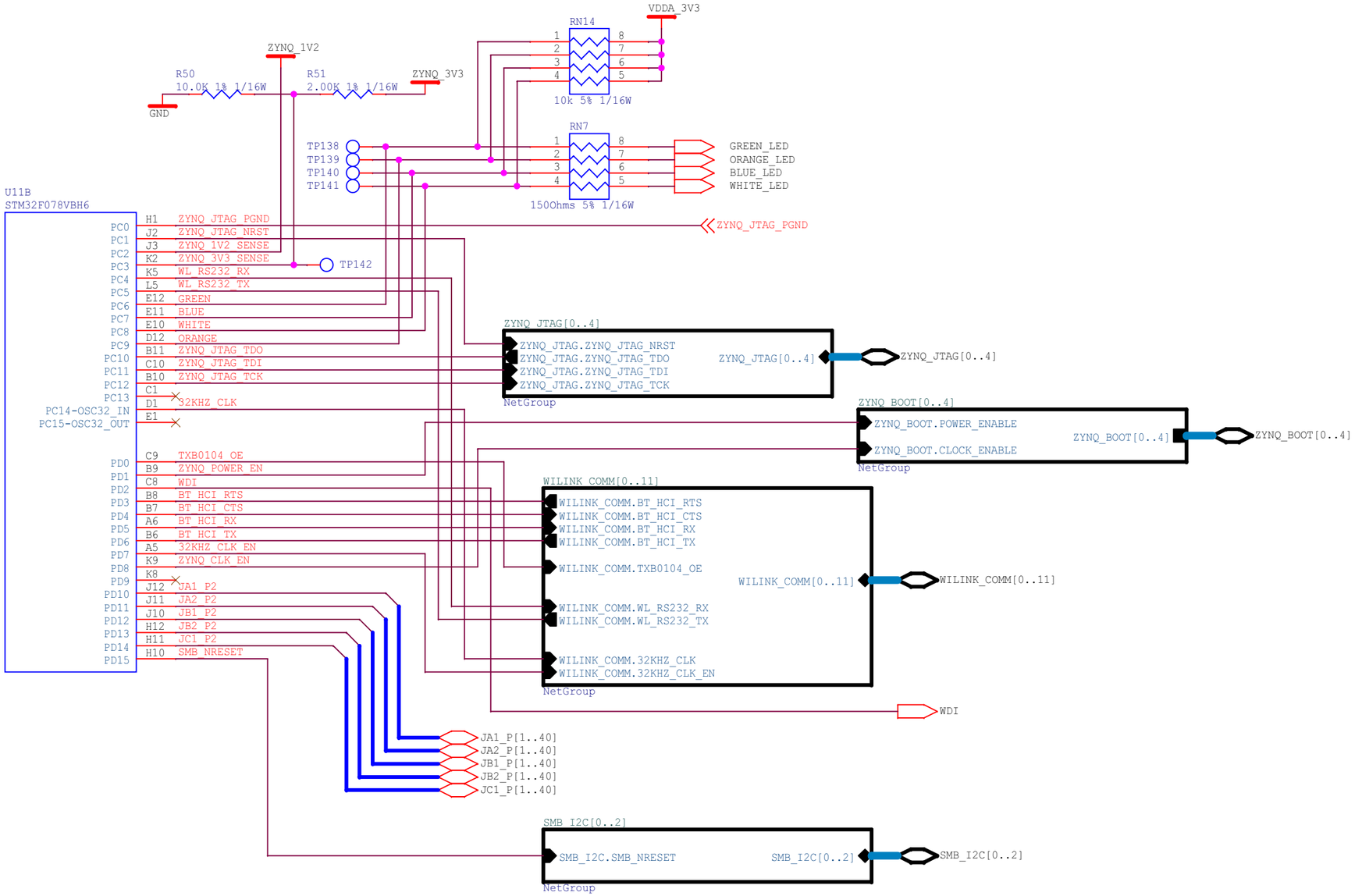
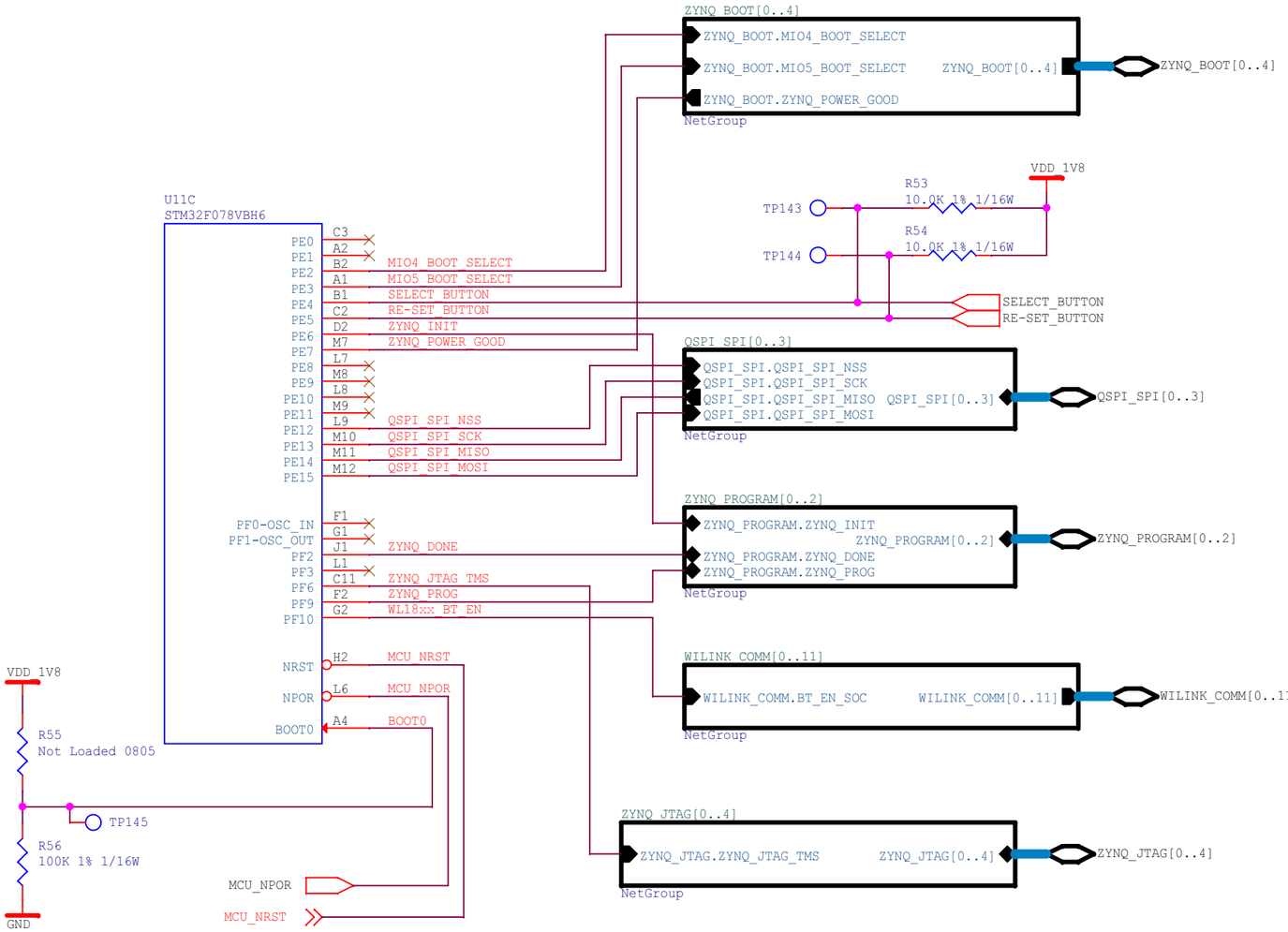
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 16 OF 30



krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857	TITLE: snickerdoodle FPGA Module PATH: /X10 DESCRIPTION: Platform Controller	
	NAME / DATE DRAWN BY: B. Hammond / 11/22/2015 CHECKED BY: J. Weatherbee / 11/23/2015 APPROVED BY: J. Weatherbee / 11/23/2015	SIZE: B DRAWING NO.: 15081800-01 REV: 4.11 SHEET 17 OF 30



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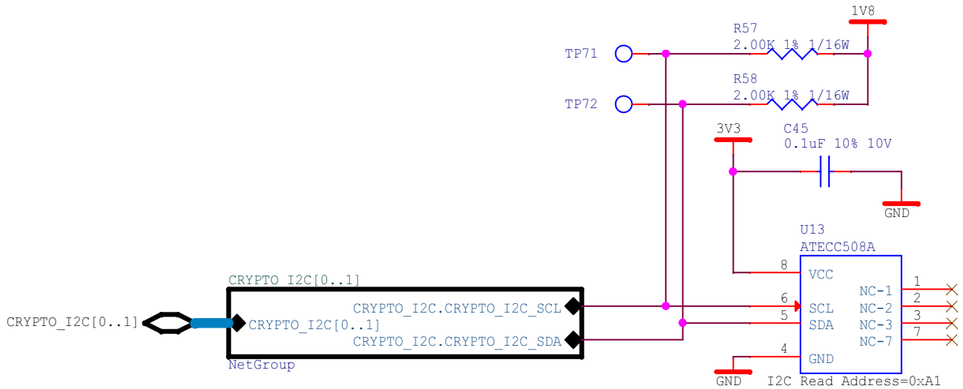
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 18 OF 30



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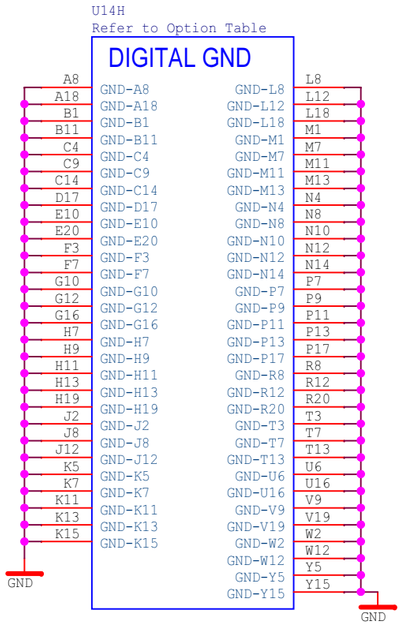
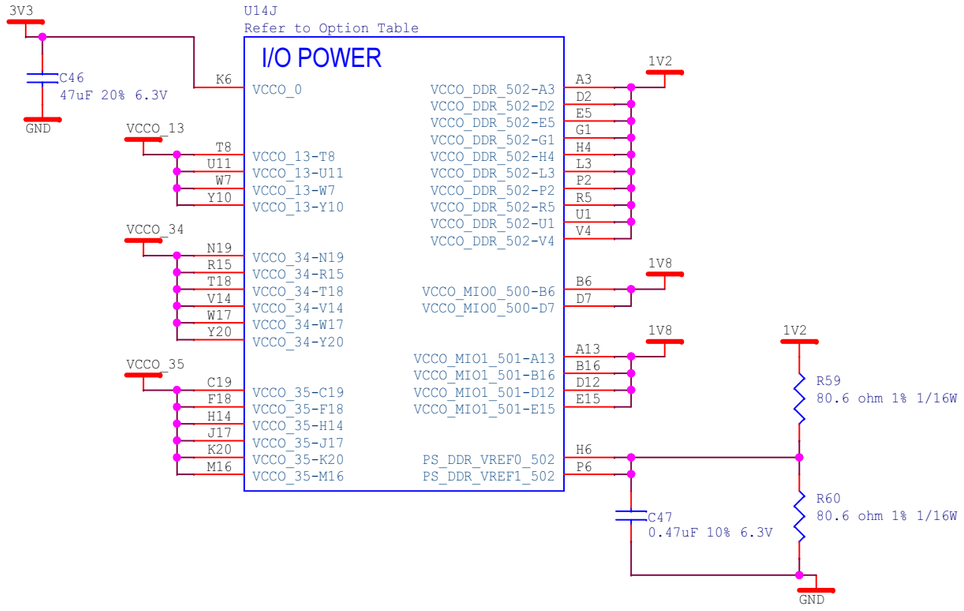
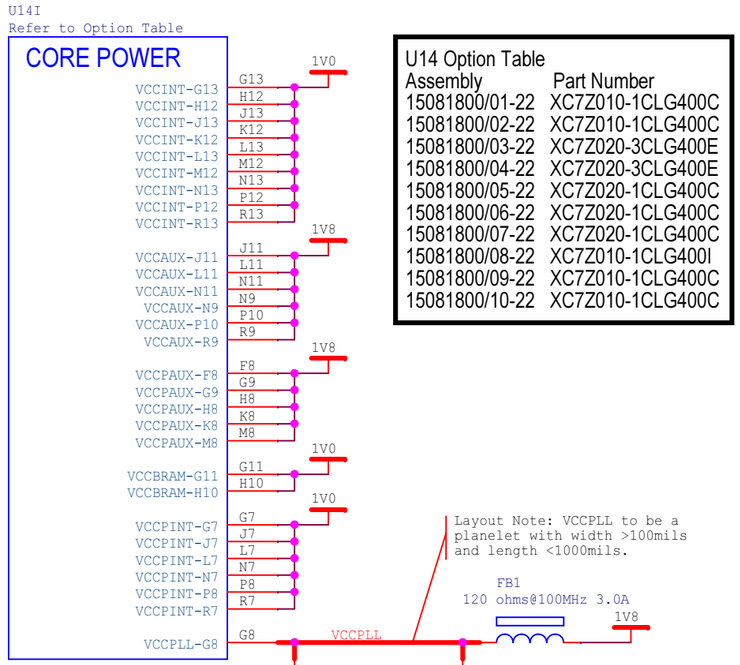
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

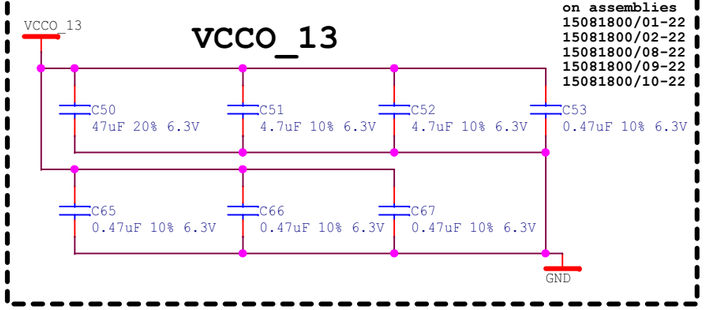
TITLE: snickerdoodle FPGA Module
PATH: /X12
DESCRIPTION: Crypto-Authenticator
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 19 OF 30

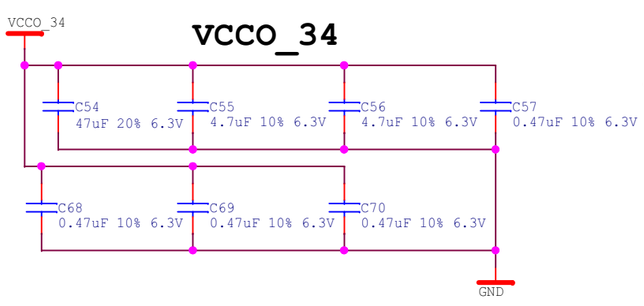


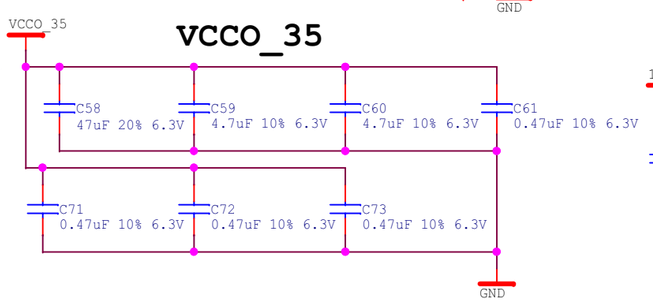


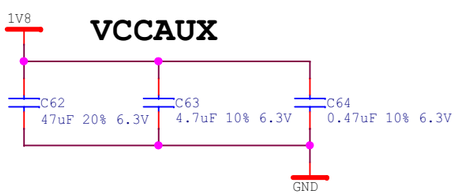


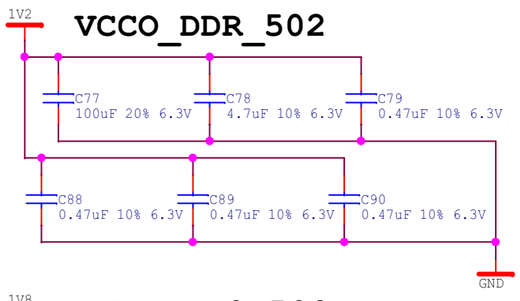
U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C

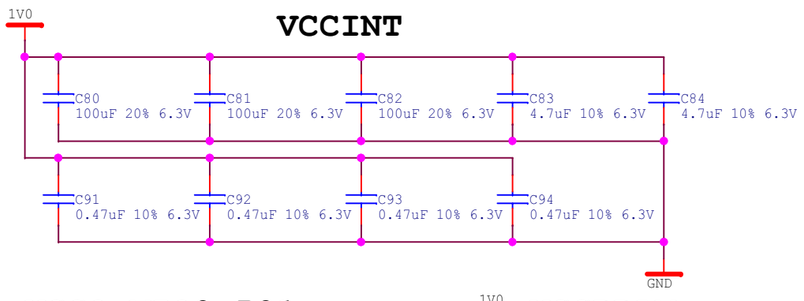


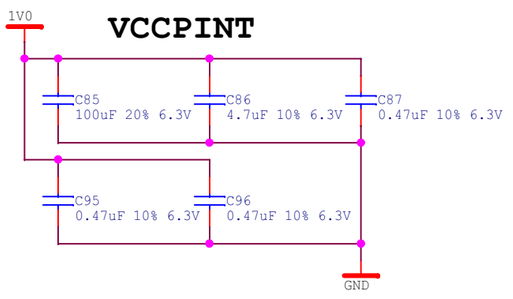


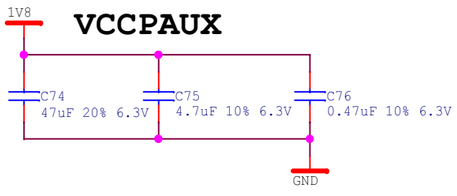


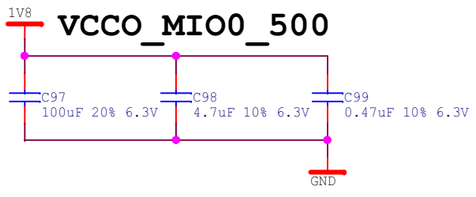


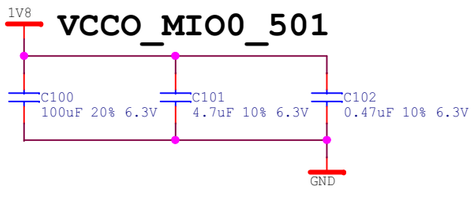


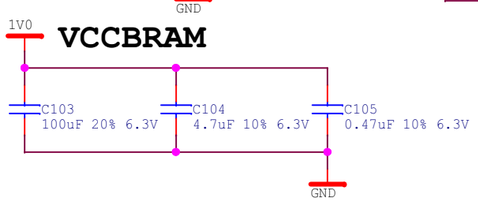












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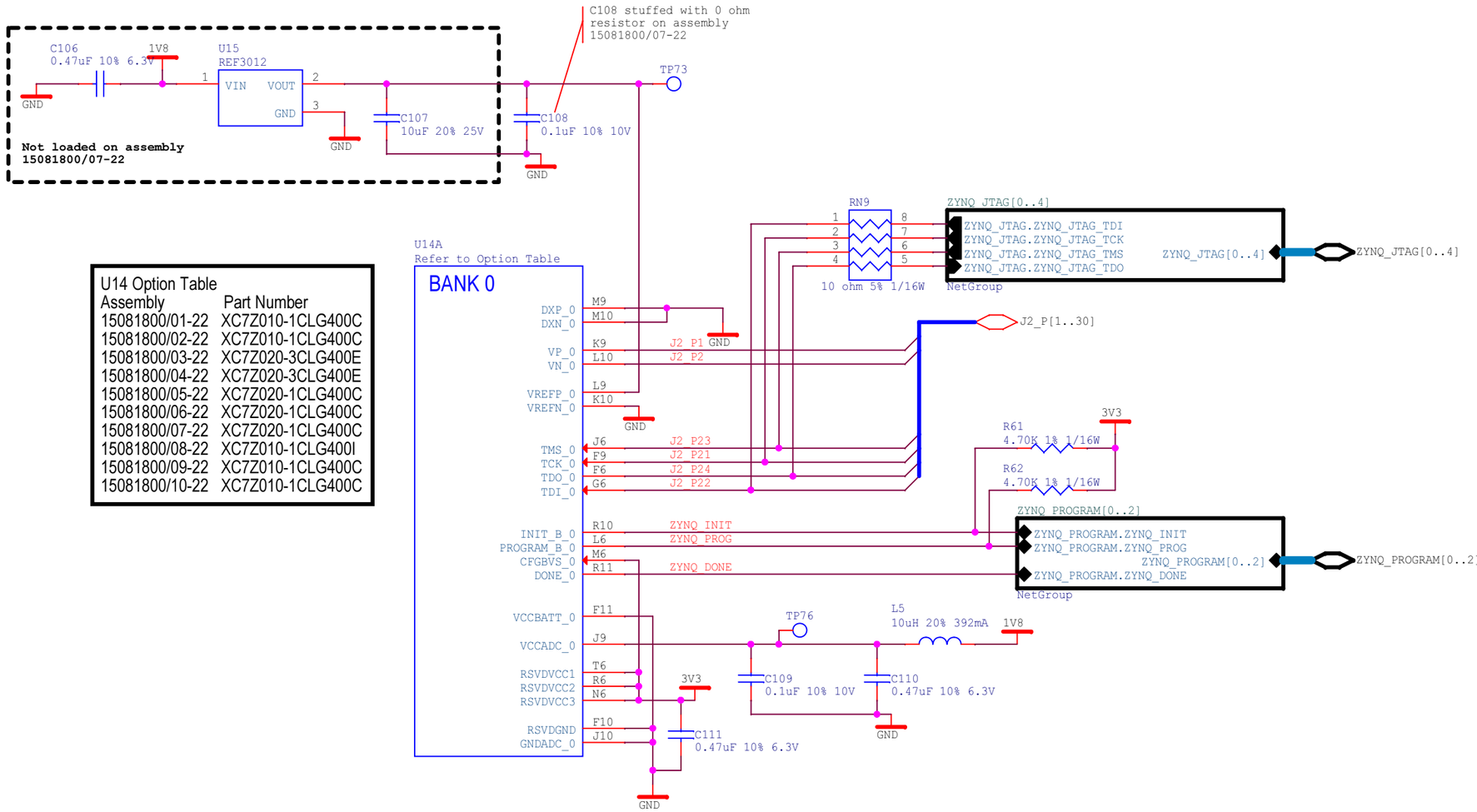
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE	snickerdoodle FPGA Module
PATH	/X13
DESCRIPTION	Zynq SoC
SIZE	B
DRAWING NO.	15081800-01
REV	4.11
SHEET	20 OF 30



U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C

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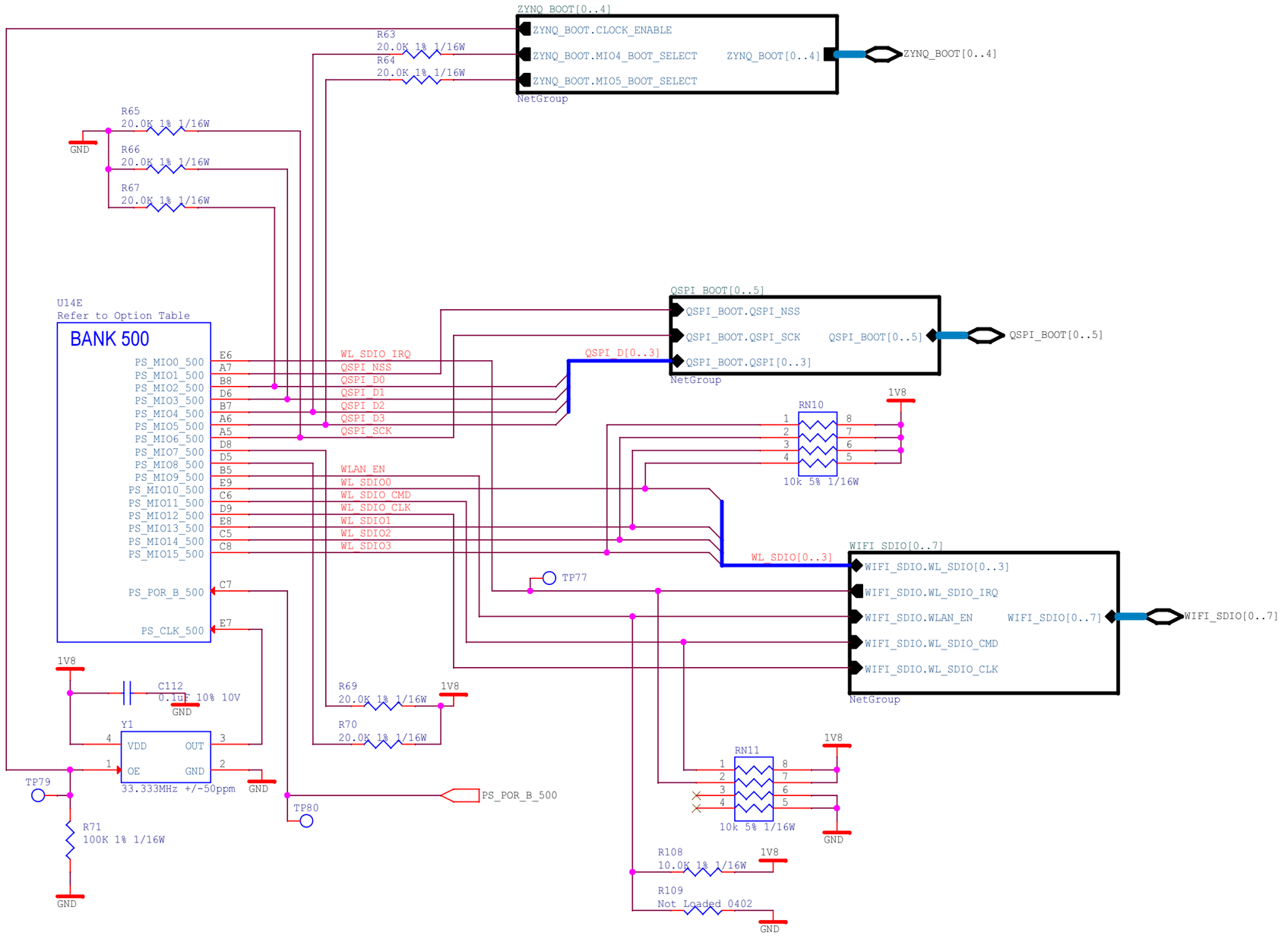
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 21 OF 30

U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C



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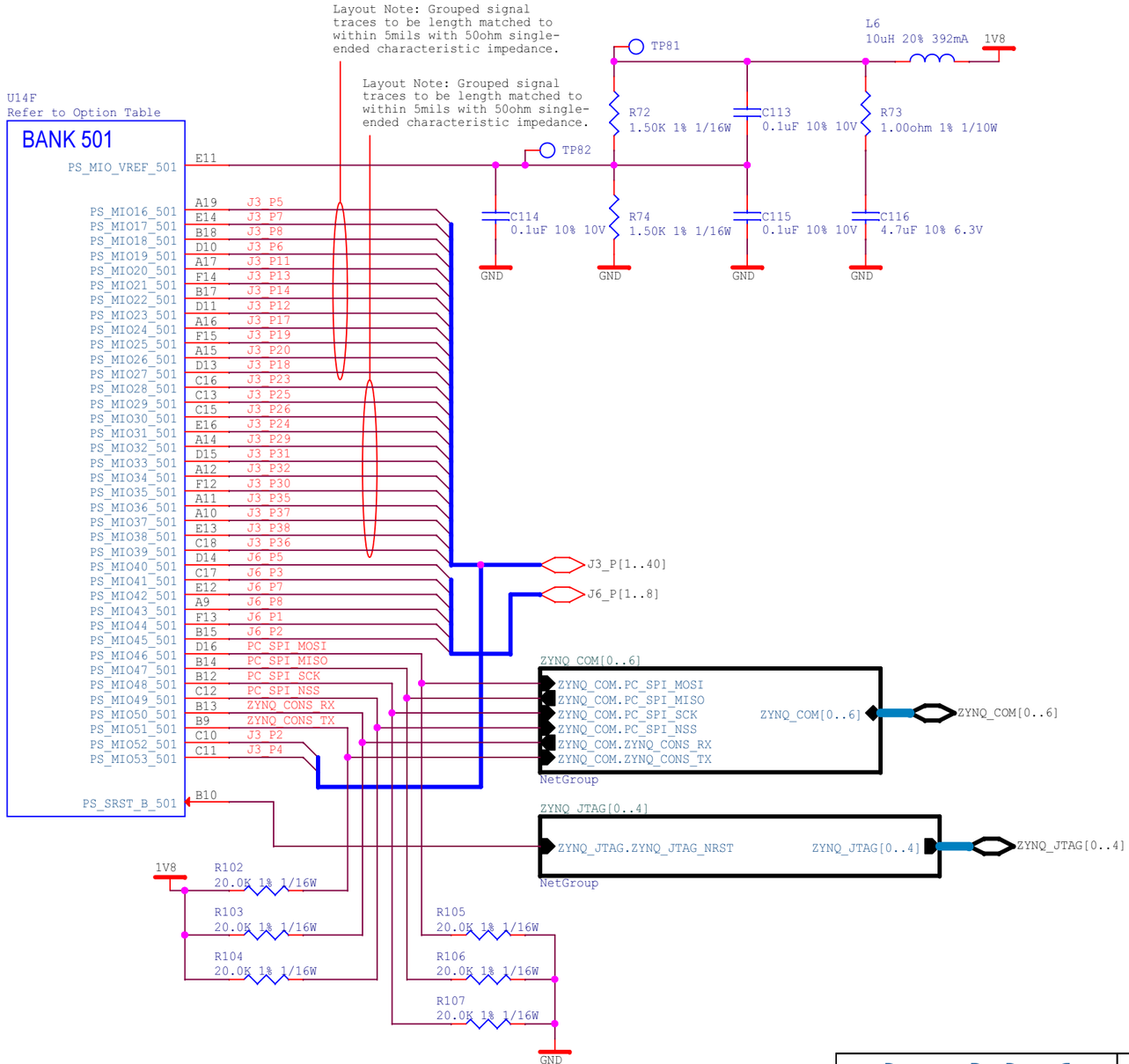
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE	snickerdoodle FPGA Module
PATH	/X13
DESCRIPTION	Zynq SoC
SIZE	B
DRAWING NO.	15081800-01
REV	4.11
SHEET	22 OF 30

U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 23 OF 30

U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C

U14G
Refer to Option Table

BANK 502

PS_DDR_DQ0_502	C3	DQ0
PS_DDR_DQ1_502	B3	DQ1
PS_DDR_DQ2_502	A2	DQ2
PS_DDR_DQ3_502	A4	DQ3
PS_DDR_DQ4_502	D3	DQ4
PS_DDR_DQ5_502	D1	DQ5
PS_DDR_DQ6_502	C1	DQ6
PS_DDR_DQ7_502	E1	DQ7
PS_DDR_DQ8_502	E2	DQ8
PS_DDR_DQ9_502	E3	DQ9
PS_DDR_DQ10_502	G3	DQ10
PS_DDR_DQ11_502	H3	DQ11
PS_DDR_DQ12_502	J3	DQ12
PS_DDR_DQ13_502	H2	DQ13
PS_DDR_DQ14_502	H1	DQ14
PS_DDR_DQ15_502	J1	DQ15
PS_DDR_DQ16_502	P1	DQ16
PS_DDR_DQ17_502	P3	DQ17
PS_DDR_DQ18_502	R3	DQ18
PS_DDR_DQ19_502	R1	DQ19
PS_DDR_DQ20_502	T4	DQ20
PS_DDR_DQ21_502	U4	DQ21
PS_DDR_DQ22_502	U2	DQ22
PS_DDR_DQ23_502	U3	DQ23
PS_DDR_DQ24_502	V1	DQ24
PS_DDR_DQ25_502	Y3	DQ25
PS_DDR_DQ26_502	W1	DQ26
PS_DDR_DQ27_502	Y4	DQ27
PS_DDR_DQ28_502	Y2	DQ28
PS_DDR_DQ29_502	W3	DQ29
PS_DDR_DQ30_502	V2	DQ30
PS_DDR_DQ31_502	V3	DQ31
PS_DDR_A0_502	N2	A0
PS_DDR_A1_502	K2	A1
PS_DDR_A2_502	M3	A2
PS_DDR_A3_502	K3	A3
PS_DDR_A4_502	M4	A4
PS_DDR_A5_502	L1	A5
PS_DDR_A6_502	L4	A6
PS_DDR_A7_502	K4	A7
PS_DDR_A8_502	K1	A8
PS_DDR_A9_502	J4	A9
PS_DDR_A10_502	F5	
PS_DDR_A11_502	G4	
PS_DDR_A12_502	E4	
PS_DDR_A13_502	D4	
PS_DDR_A14_502	F4	
PS_DDR_DQS_P0_502	C2	DQS_P0
PS_DDR_DQS_N0_502	B2	DQS_N0
PS_DDR_DQS_P1_502	G2	DQS_P1
PS_DDR_DQS_N1_502	F2	DQS_N1
PS_DDR_DQS_P2_502	R2	DQS_P2
PS_DDR_DQS_N2_502	T2	DQS_N2
PS_DDR_DQS_P3_502	W5	DQS_P3
PS_DDR_DQS_N3_502	W4	DQS_N3
PS_DDR_CKP_502	L2	CKP
PS_DDR_CKN_502	M2	CKN
PS_DDR_BA0_502	L5	
PS_DDR_BA1_502	R4	
PS_DDR_BA2_502	J5	
PS_DDR_DM0_502	A1	DM0
PS_DDR_DM1_502	F1	DM1
PS_DDR_DM2_502	T1	DM2
PS_DDR_DM3_502	Y1	DM3
PS_DDR_CS_B_502	N1	CS_B
PS_DDR_WE_B_502	M5	
PS_DDR_CAS_B_502	P5	
PS_DDR_RAS_B_502	P4	
PS_DDR_CKE_502	N3	CKE
PS_DDR_ODT_502	N5	
PS_DDR_DRST_B_502	B4	
PS_DDR_VRP_502	H5	
PS_DDR_VRN_502	G5	

R75 40.2 Ohms 1% 1/16W
R76 40.2 Ohms 1% 1/16W
1V2
GND

Layout Note: Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

LPDDR2-SDRAM-IO[0..57]
DQ[0..31]
A[0..9]
DQS_P[0..3]
DQS_N[0..3]
DM[0..3]
LPDDR2-SDRAM-IO.DQ[0..31]
LPDDR2-SDRAM-IO.A[0..9]
LPDDR2-SDRAM-IO.DQS_P[0..3]
LPDDR2-SDRAM-IO.DQS_N[0..3]
LPDDR2-SDRAM-IO.DM[0..3]LPDDR2-SDRAM-IO[0..57]
LPDDR2-SDRAM-IO.CS_B
LPDDR2-SDRAM-IO.CKE
LPDDR2-SDRAM-IO.CKP
LPDDR2-SDRAM-IO.CKN
NetGroup
LPDDR2-SDRAM-IO[0..57]

Layout Note: Route clock on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 24 OF 30

U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C
15081800/07-22	XC7Z020-1CLG400C
15081800/08-22	XC7Z010-1CLG400I
15081800/09-22	XC7Z010-1CLG400C
15081800/10-22	XC7Z010-1CLG400C

U14D
Refer to Option Table

BANK 35

IO_0_35	G14	JA1_P4
IO_L1P_T0_AD0P_35	C20	JA1_P14
IO_L1N_T0_AD0N_35	B20	JA1_P12
IO_L2P_T0_AD8P_35	B19	JA1_P20
IO_L2N_T0_AD8N_35	A20	JA1_P18
IO_L3P_T0_DQS_AD1P_35	E17	JA1_P17
IO_L3N_T0_DQS_AD1N_35	D18	JA1_P19
IO_L4P_T0_35	D19	JA1_P8
IO_L4N_T0_35	D20	JA1_P6
IO_L5P_T0_AD9P_35	E18	JA1_P5
IO_L5N_T0_AD9N_35	E19	JA1_P7
IO_L6P_T0_35	F16	JA1_P11
IO_L6N_T0_VREF_35	F17	JA1_P13
IO_L7P_T1_AD2P_35	M19	JA2_P32
IO_L7N_T1_AD2N_35	M20	JA2_P30
IO_L8P_T1_AD10P_35	M17	JA2_P29
IO_L8N_T1_AD10N_35	M18	JA2_P31
IO_L9P_T1_DQS_AD3P_35	L19	JA2_P23
IO_L9N_T1_DQS_AD3N_35	L20	JA2_P25
IO_L10P_T1_AD11P_35	K19	JA2_P26
IO_L10N_T1_AD11N_35	J19	JA2_P24
IO_L11P_T1_SRCC_35	L16	JA2_P35
IO_L11N_T1_SRCC_35	L17	JA2_P37
IO_L12P_T1_MRCC_35	K17	JA2_P38
IO_L12N_T1_MRCC_35	K18	JA2_P36
IO_L13P_T2_MRCC_35	H16	JA1_P38
IO_L13N_T2_MRCC_35	H17	JA1_P36
IO_L14P_T2_AD4P_SRCC_35	J18	JA1_P35
IO_L14N_T2_AD4N_SRCC_35	H18	JA1_P37
IO_L15P_T2_DQS_AD12P_35	F19	JA1_P23
IO_L15N_T2_DQS_AD12N_35	F20	JA1_P25
IO_L16P_T2_35	G17	JA1_P32
IO_L16N_T2_35	G18	JA1_P30
IO_L17P_T2_AD5P_35	J20	JA1_P29
IO_L17N_T2_AD5N_35	H20	JA1_P31
IO_L18P_T2_AD13P_35	G19	JA1_P26
IO_L18N_T2_AD13N_35	G20	JA1_P24
IO_L19P_T3_35	H15	JA2_P14
IO_L19N_T3_VREF_35	G15	JA2_P12
IO_L20P_T3_AD6P_35	K14	JA2_P20
IO_L20N_T3_AD6N_35	J14	JA2_P18
IO_L21P_T3_DQS_AD14P_35	N15	JA2_P17
IO_L21N_T3_DQS_AD14N_35	N16	JA2_P19
IO_L22P_T3_AD7P_35	L14	JA2_P5
IO_L22N_T3_AD7N_35	L15	JA2_P7
IO_L23P_T3_35	M14	JA2_P11
IO_L23N_T3_35	M15	JA2_P13
IO_L24P_T3_AD15P_35	K16	JA2_P8
IO_L24N_T3_AD15N_35	J16	JA2_P6
IO_25_35	J15	JA2_P4

JA1_P[1..40]

JA2_P[1..40]

U14C
Refer to Option Table

BANK 34

IO_0_34	R19	JB2_P4
IO_L1P_T0_34	T11	JB1_P5
IO_L1N_T0_34	T10	JB1_P7
IO_L2P_T0_34	T12	JB1_P8
IO_L2N_T0_34	U12	JB1_P6
IO_L3P_T0_DQS_PUDC_B_34	U13	JB1_P17
IO_L3N_T0_DQS_34	V13	JB1_P19
IO_L4P_T0_34	V12	JB1_P14
IO_L4N_T0_34	W13	JB1_P12
IO_L5P_T0_34	T14	JB1_P20
IO_L5N_T0_34	T15	JB1_P18
IO_L6P_T0_34	P14	JB1_P11
IO_L6N_T0_VREF_34	R14	JB1_P13
IO_L7P_T1_34	Y16	JB1_P26
IO_L7N_T1_34	Y17	JB1_P24
IO_L8P_T1_34	W14	JB1_P29
IO_L8N_T1_34	Y14	JB1_P31
IO_L9P_T1_DQS_34	T16	JB1_P23
IO_L9N_T1_DQS_34	U17	JB1_P25
IO_L10P_T1_34	V15	JB1_P32
IO_L10N_T1_34	W15	JB1_P30
IO_L11P_T1_SRCC_34	U14	JB1_P35
IO_L11N_T1_SRCC_34	U15	JB1_P37
IO_L12P_T1_MRCC_34	U18	JB1_P38
IO_L12N_T1_MRCC_34	U19	JB1_P36
IO_L13P_T2_MRCC_34	N18	JB2_P38
IO_L13N_T2_MRCC_34	P19	JB2_P36
IO_L14P_T2_SRCC_34	N20	JB2_P35
IO_L14N_T2_SRCC_34	P20	JB2_P37
IO_L15P_T2_DQS_34	T20	JB2_P23
IO_L15N_T2_DQS_34	U20	JB2_P25
IO_L16P_T2_34	V20	JB2_P29
IO_L16N_T2_34	W20	JB2_P31
IO_L17P_T2_34	Y18	JB2_P32
IO_L17N_T2_34	Y19	JB2_P30
IO_L18P_T2_34	V16	JB2_P26
IO_L18N_T2_34	W16	JB2_P24
IO_L19P_T3_34	R16	JB2_P14
IO_L19N_T3_VREF_34	R17	JB2_P12
IO_L20P_T3_34	T17	JB2_P11
IO_L20N_T3_34	R18	JB2_P13
IO_L21P_T3_DQS_34	V17	JB2_P17
IO_L21N_T3_DQS_34	V18	JB2_P19
IO_L22P_T3_34	W18	JB2_P20
IO_L22N_T3_34	W19	JB2_P18
IO_L23P_T3_34	N17	JB2_P5
IO_L23N_T3_34	P18	JB2_P7
IO_L24P_T3_34	P15	JB2_P8
IO_L24N_T3_34	P16	JB2_P6
IO_25_34	T19	JB1_P4

JB1_P[1..40]

JB2_P[1..40]

Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

Layout Note: Grouped signal traces to be length matched to within 10mils.

U14B
Refer to Option Table

BANK 13

IO_L6N_T0_VREF_13	V5	JC1_P4
IO_L11P_T1_SRCC_13	U7	JC1_P5
IO_L11N_T1_SRCC_13	V7	JC1_P7
IO_L12P_T1_MRCC_13	T9	JC1_P8
IO_L12N_T1_MRCC_13	U10	JC1_P6
IO_L13P_T2_MRCC_13	Y7	JC1_P38
IO_L13N_T2_MRCC_13	Y6	JC1_P36
IO_L14P_T2_SRCC_13	Y9	JC1_P35
IO_L14N_T2_SRCC_13	Y8	JC1_P37
IO_L15P_T2_DQS_13	V8	JC1_P23
IO_L15N_T2_DQS_13	W8	JC1_P25
IO_L16P_T2_13	W10	JC1_P32
IO_L16N_T2_13	W9	JC1_P30
IO_L17P_T2_13	U9	JC1_P29
IO_L17N_T2_13	U8	JC1_P31
IO_L18P_T2_13	W11	JC1_P26
IO_L18N_T2_13	Y11	JC1_P24
IO_L19P_T3_13	T5	JC1_P11
IO_L19N_T3_VREF_13	U5	JC1_P13
IO_L20P_T3_13	Y12	JC1_P14
IO_L20N_T3_13	Y13	JC1_P12
IO_L21P_T3_DQS_13	V11	JC1_P17
IO_L21N_T3_DQS_13	V10	JC1_P19
IO_L22P_T3_13	V6	JC1_P20
IO_L22N_T3_13	W6	JC1_P18

JC1_P[1..40]

Not available on assemblies 15081800/01-22 15081800/02-22 15081800/08-22 15081800/09-22 15081800/10-22

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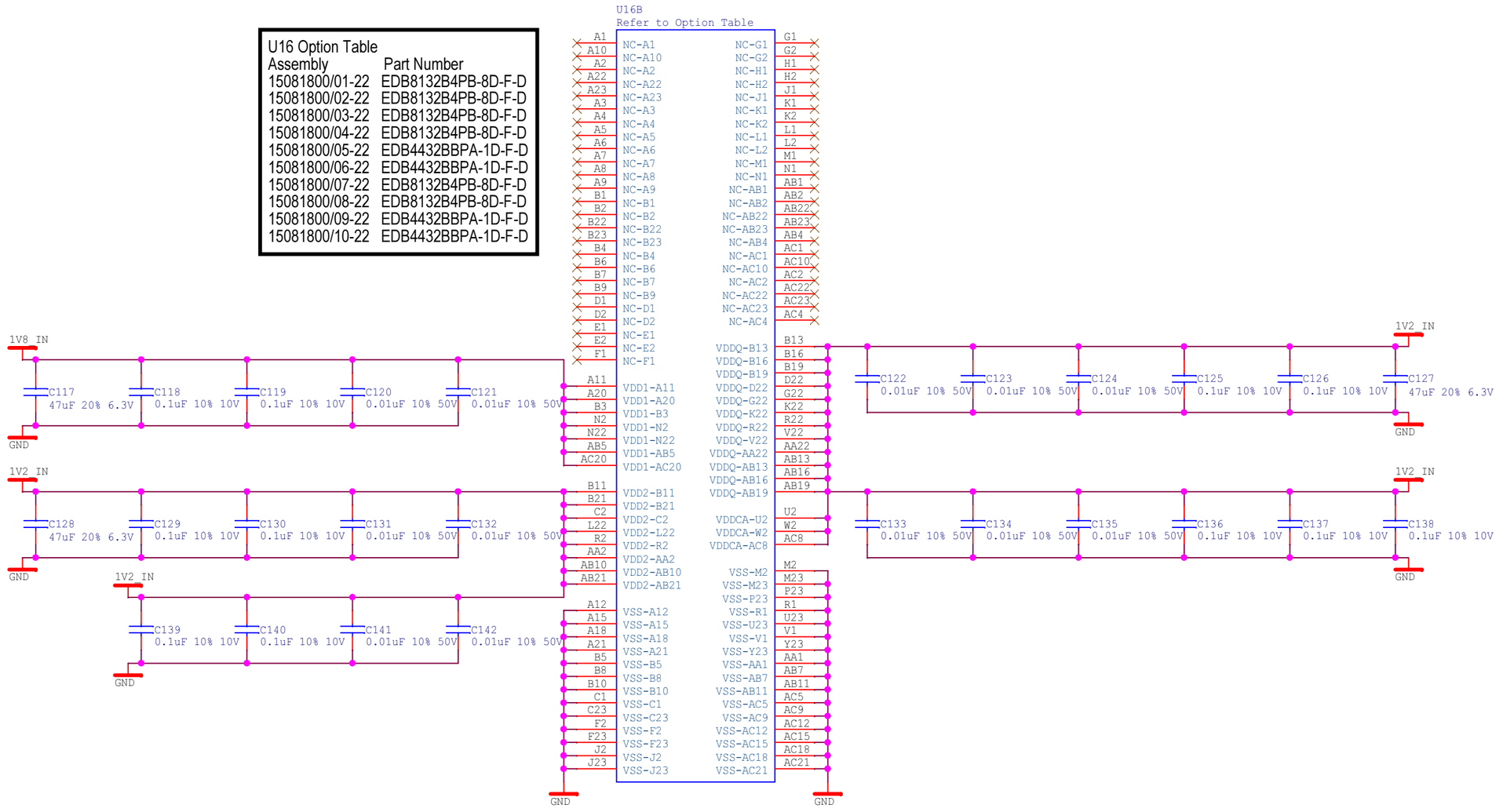
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 25 OF 30

U16 Option Table	
Assembly	Part Number
15081800/01-22	EDB8132B4PB-8D-F-D
15081800/02-22	EDB8132B4PB-8D-F-D
15081800/03-22	EDB8132B4PB-8D-F-D
15081800/04-22	EDB8132B4PB-8D-F-D
15081800/05-22	EDB4432BBPA-1D-F-D
15081800/06-22	EDB4432BBPA-1D-F-D
15081800/07-22	EDB8132B4PB-8D-F-D
15081800/08-22	EDB8132B4PB-8D-F-D
15081800/09-22	EDB4432BBPA-1D-F-D
15081800/10-22	EDB4432BBPA-1D-F-D



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APPROVED BY	J. Weatherbee	11/23/2015

TITLE	snickerdoodle FPGA Module
PATH	/X14
DESCRIPTION	LPDDR2 RAM
SIZE	B
DRAWING NO.	15081800-01
REV	4.11
SHEET	26 OF 30

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

Layout Note: Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

U16 Option Table	
Assembly	Part Number
15081800/01-22	EDB8132B4PB-8D-F-D
15081800/02-22	EDB8132B4PB-8D-F-D
15081800/03-22	EDB8132B4PB-8D-F-D
15081800/04-22	EDB8132B4PB-8D-F-D
15081800/05-22	EDB4432BBPA-1D-F-D
15081800/06-22	EDB4432BBPA-1D-F-D
15081800/07-22	EDB8132B4PB-8D-F-D
15081800/08-22	EDB8132B4PB-8D-F-D
15081800/09-22	EDB4432BBPA-1D-F-D
15081800/10-22	EDB4432BBPA-1D-F-D

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO.DQ[0..31]
LPDDR2-SDRAM-IO.DQS_P[0..3]
LPDDR2-SDRAM-IO.DQS_N[0..3]
LPDDR2-SDRAM-IO.DM[0..3]
LPDDR2-SDRAM-IO.CS_B
LPDDR2-SDRAM-IO.CKE
LPDDR2-SDRAM-IO.CKP
LPDDR2-SDRAM-IO.CKN
LPDDR2-SDRAM-IO.A[0..9]

NetGroup

DQ[0..31]
DQS_P[0..3]
DQS_N[0..3]
DM[0..3]
CS_B
CKE
CKP
CKN
A[0..9]

U16A
Refer to Option Table

DQS_P3	B18	DQ31	B12	DQ31
DQS_P2	AB18	DQ30	A13	DQ30
DQS_P1	J22	DQ29	A14	DQ29
DQS_P0	R23	DQ28	B14	DQ28
		DQ27	B15	DQ27
DQS_N3	A19	DQ26	A16	DQ26
DQS_N2	AC19	DQ25	A17	DQ25
DQS_N1	K23	DQ24	B17	DQ24
DQS_N0	P22	DQ23	AC17	DQ23
		DQ22	AB17	DQ22
DM3	B20	DQ21	AC16	DQ21
DM2	AB20	DQ20	AB15	DQ20
DM1	L23	DQ19	AC14	DQ19
DM0	N23	DQ18	AB14	DQ18
		DQ17	AC13	DQ17
CS_B	AB3	DQ16	AB12	DQ16
CKE	AC3	DQ15	C22	DQ15
CKP	Y2	DQ14	D23	DQ14
CKN	Y1	DQ13	E23	DQ13
		DQ12	E22	DQ12
A9	T1	DQ11	F22	DQ11
A8	T2	DQ10	G23	DQ10
A7	U1	DQ9	H23	DQ9
A6	V2	DQ8	H22	DQ8
A5	W1	DQ7	T23	DQ7
A4	AB9	DQ6	T22	DQ6
A3	AB8	DQ5	U22	DQ5
A2	AC7	DQ4	V23	DQ4
A1	AB6	DQ3	W23	DQ3
A0	AC6	DQ2	W22	DQ2
		DQ1	Y22	DQ1
ZQ1	AC11	DQ0	AA23	DQ0
ZQ0	P1			
VREFCA	P2	VREFDQ	M22	

Layout Note: Route clocks on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10 mil spacing from other nets. Length match all clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

R77
240 ohm 1% 1/16W
R78
240 ohm 1% 1/16W
R79
4.70K 1% 1/16W
GND

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

L7
10uH 20% 392mA 1V2_IN
L8
10uH 20% 392mA 1V2_IN

TP88
TP90

R80
1.00ohm 1% 1/10W
C143
0.1uF 10% 10V
R81
1.50K 1% 1/16W
VREFCA
C145
4.7uF 10% 6.3V
C146
0.1uF 10% 10V
R84
1.50K 1% 1/16W
C147
0.1uF 10% 10V
C148
0.1uF 10% 10V

R82
1.00ohm 1% 1/10W
C144
0.1uF 10% 10V
R83
1.50K 1% 1/16W
VREFDQ
C149
4.7uF 10% 6.3V
C150
0.1uF 10% 10V
R85
1.50K 1% 1/16W
C151
0.1uF 10% 10V
C152
0.1uF 10% 10V

GND

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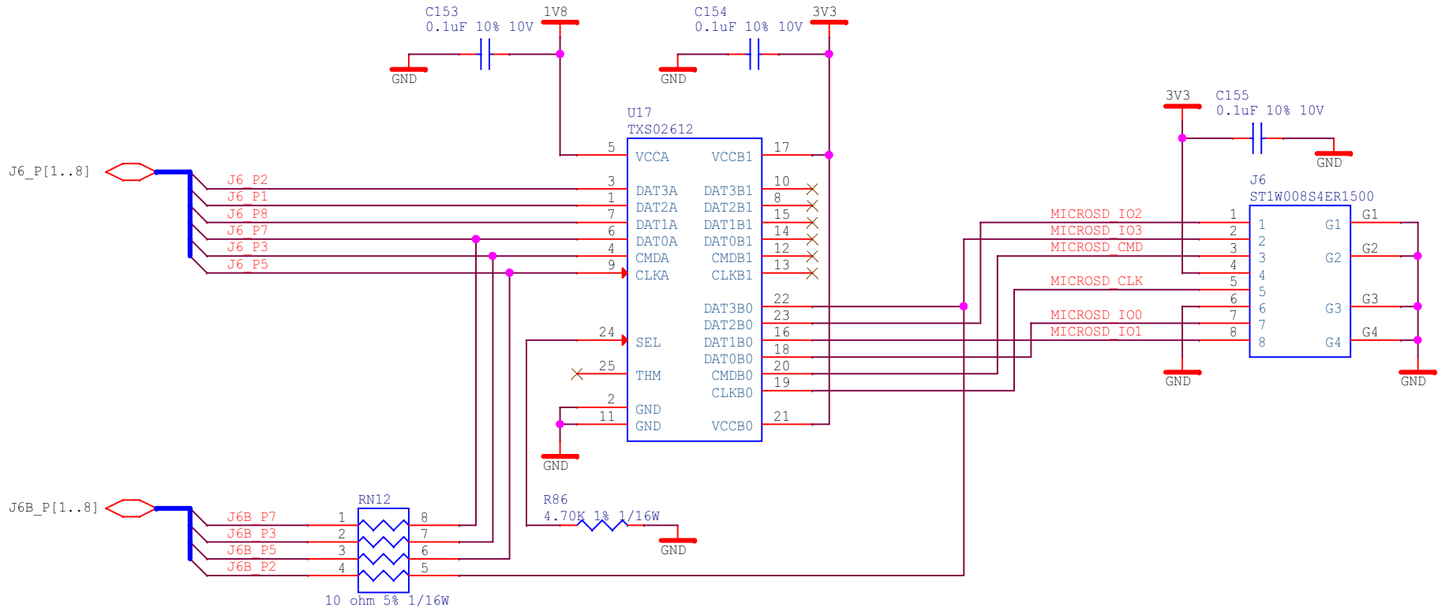
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 27 OF 30



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DRAWN BY	B. Hammond	11/22/2015
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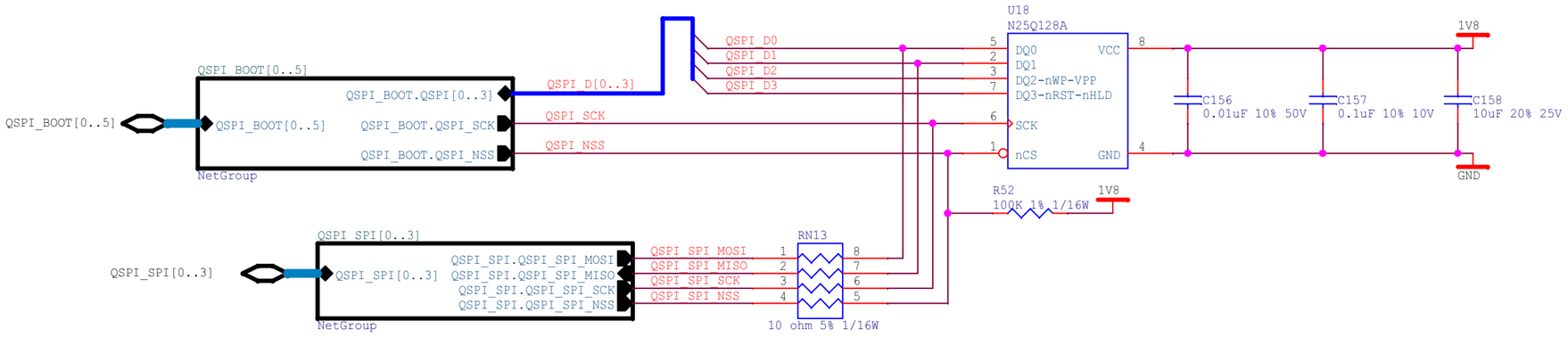
TITLE: snickerdoodle FPGA Module
PATH: /X15
DESCRIPTION: microSD Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 28 OF 30



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TITLE: snickerdoodle FPGA Module
PATH: /X16
DESCRIPTION: QSPI Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 29 OF 30

Design Note: Remove R87 and R88 to disable chip antenna.

R87 10 ohm 1% 1/16W
R88 10 ohm 1% 1/16W
ANT_SELECT_1
ANT_SELECT_2
C159 33pF 5% 50V
C160 33pF 5% 50V
RFGND
3V3_RF
R110 20.0K 1% 1/16W
R111 20.0K 1% 1/16W
WLAN_EN
WL_SDIO_IRQ
WL_SDIO_CMD
WL_SDIO_CLK
WL_SDIO[0..3]
TP101
TP102
TP103
TP104

WIFI_SDIO[0..7]
WIFI_SDIO.WLAN_EN
WIFI_SDIO.WL_SDIO_IRQ
WIFI_SDIO.WL_SDIO_CMD
WIFI_SDIO.WL_SDIO_CLK
WIFI_SDIO.WL_SDIO[0..3]
NetGroup

U22
SKY13351-378LF
VCTL1
IN
VCTL2
OUT1
GND
OUT2
EP
C161 100pF 5% 50V
C162 1.0pF +/-0.1pF
L10 Not Loaded 0402
L9 1.3nH +/-0.1nH 280mA
ANTENNA1A
ANTENNA1B
ANTENNA2
C163 100pF 5% 50V
C164 100pF 5% 50V
C165 Refer to Option Table

U20
Refer to Option Table
WLAN_EN_SOC
WLAN_IRQ
WL_SDIO_CMD
WL_SDIO_CLK
WL_SDIO_D0
WL_SDIO_D1
WL_SDIO_D2
WL_SDIO_D3
GPIO2
GPIO1
WL_UART_DBG
BT_EN_SOC
BT_HCI_RTS
BT_HCI_CTS
BT_HCI_TX
BT_HCI_RX
BT_AUD_IN
BT_AUD_OUT
BT_AUD_FSYNC
BT_AUD_CLK
BT_UART_DBG
EXT_32K
VBAT-46
VBAT-47
VIO
GND-1
GND-7
GND-9
GND-15
GND-16
GND-17
GND-19
GND-20
GND-23
GND-24
GND-28
GND-29
GND-30
GND-31
GND-33
GND-34
GND-35
GND-37
GND-39
GND-44
GND-45
GND-48
GND-49
GND-54
RF_ANT1
RF_ANT2
RESERVED3
RESERVED2
RESERVED1
RESERVED0
GPIO12
GPIO11
GPIO10
GPIO9
GPIO4
GND-G1
GND-G2
GND-G3
GND-G4
GND-G5
GND-G6
GND-G7
GND-G8
GND-G9
GND-G10
GND-G11
GND-G12
GND-G13
GND-G14
GND-G15
GND-G16
GND-G17
GND-G18
GND-G19
GND-G20
GND-G21
GND-G22
GND-G23
GND-G24
GND-G25
GND-G26
GND-G27
GND-G28
GND-G29
GND-G30
GND-G31
GND-G32
GND-G33
GND-G34
GND-G35
GND-G36
GND-63
GND-61
GND-59
GND-55

TP105
TP106
TP109
TP110
WL_SDIO0
WL_SDIO1
WL_SDIO2
WL_SDIO3
TP111
TP112
TP114
TP108
TP115
TP116
TP117
TP119
TP120
TP107
TP118
TP121
TP122
TP123

R89 0ohms 1/10W

Layout Notes: 50ohm single-ended characteristic impedance for all RF traces from U20 pins 18 and 32 through all parts to the antenna E1 and RF connectors J4 and J5. RF traces must have via stitching on the ground plane beside the RF traces on both sides. Refer to section 8 of Texas Instruments document SWRU382A "WL1837MODCOM8I WLAN MIMO and Bluetooth® Module Evaluation Board for TI Sitara™ Platform" for complete layout guidelines.

Layout Note: Add a minimum of 20 thermal vias in die attach pads GND-Gxx area for thermal considerations.

WILINK_COMM[0..11]
WILINK_COMM.ANT_SELECT_1
WILINK_COMM.ANT_SELECT_2
WILINK_COMM.WL_RS232_RX
WILINK_COMM.WL_RS232_TX
WILINK_COMM.BT_EN_SOC
WILINK_COMM.BT_HCI_RTS
WILINK_COMM.BT_HCI_CTS
WILINK_COMM.BT_HCI_TX
WILINK_COMM.BT_HCI_RX
WILINK_COMM.32KHZ_CLK_EN
WILINK_COMM.TXB0104_OE
WILINK_COMM.32KHZ_CLK
NetGroup

R90 100K 1% 1/16W
C166 0.1uF 10% 10V
C167 0.1uF 10% 10V
1V8_RF

U21
TXB0104RGYR
VCCB
VCCA
B1
B2
B3
B4
A1
A2
A3
A4
NC9
NC6
THM
OE
GND

J2_P14
J2_P13
J2_P12
J2_P11
J2_P[1..30]

Not loaded on assemblies
15081800/05-22
15081800/06-22
15081800/07-22
15081800/09-22
15081800/10-22

R91 100K 1% 1/16W

Y2
32.768kHz
EN
VDD
GND
OUT
32KHZ_CLK
R92 100K 1% 1/16W

C168 10uF 20% 25V
C169 0.1uF 10% 10V
C170 0.1uF 10% 10V
C171 1.0uF 10% 25V

C165 Option Table

Assembly	Part Number
15081800/01-22	Not Loaded
15081800/02-22	Not Loaded
15081800/03-22	GRM1555C1H101JA01D
15081800/04-22	GRM1555C1H101JA01D
15081800/05-22	Not Loaded
15081800/06-22	Not Loaded
15081800/07-22	Not Loaded
15081800/08-22	Not loaded
15081800/09-22	Not loaded
15081800/10-22	Not loaded

U20 Option Table

Assembly	Part Number
15081800/01-22	WL1831MODGBMOCR
15081800/02-22	WL1831MODGBMOCR
15081800/03-22	WL1837MODGIMOCR
15081800/04-22	WL1837MODGIMOCR
15081800/05-22	WL1801MODGBMOCR
15081800/06-22	WL1801MODGBMOCR
15081800/07-22	Not loaded
15081800/08-22	WL1831MODGBMOCR
15081800/09-22	WL1801MODGBMOCR
15081800/10-22	WL1801MODGBMOCR

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TITLE: snickerdoodle FPGA Module
PATH: /X17
DESCRIPTION: WiLink 8 Radio
SIZE: B
DRAWING NO.: 15081800-01
REV: 4.11
SHEET 30 OF 30