Power
SZ_VIO_EN
SZ_SCL
SZ_SDA
USB_D_P
USB_D_N
POWER
RISCV_3V3_EN
Power.sch
USB Data
FT2232
USB_D_P
USB_D_N
FTDI USB – UART/JTAG
JTAG_RST
JTAG_TDI
JTAG_TMS
JTAG_TDO
JTAG_TCK
UART0_TX
UART0_RX
FTDI_SDO
FTDI_SDI
FTDI_SCLK
FTDI_CS
FTDI_RESETn
FT2232.sch
GPIO_Header
BCM4
BCM5
BCM6
BCM7
BCM8
BCM9
BCM10
BCM11
BCM12
BCM13
BCM16
BCM17
BCM18
BCM19
BCM20
BCM21
BCM22
BCM23
BCM24
BCM25
BCM26
BCM27
UART_H_RX
UART_H_TX
ID_SD
ID_SC
I2C_SDA
I2C_SCL
40-PIN GPIO
GPIO_Header.sch
FPGA_Top
SZ_VIO_EN
BCM4
BCM5
BCM6
BCM7
BCM8
BCM9
BCM10
BCM11
BCM12
BCM13
BCM16
BCM17
BCM18
BCM19
BCM20
BCM21
BCM22
BCM23
BCM24
BCM25
BCM26
BCM27
UART_H_RX
UART_H_TX
ID_SD
ID_SC
I2C_SDA
I2C_SCL
FTDI_UART_TX
FTDI_UART_RX
CDONE
CRESET_B
CFG_SDI
CFG_SDO
CFG_SCK
CFG_SS
I2C_SDA
I2C_SCL
MCU_SPI_CS0
MCU_SPI_CS2
MCU_SPI_CS3
MCU_SPI_SCK
MCU_SPI_MOSI
MCU_SPI_MISO
MCU_GPIO_11
MCU_GPIO_12
MCU_GPIO_13
MCU_GPIO_18
MCU_GPIO_20
MCU_GPIO_23
UART0_TX
UART0_RX
WAKE_N
BRD_RESET
Lattice iCE40 FPGA
SZ_SCL
SZ_SDA
SZ_D0_P
SZ_D0_N
SZ_D2_P
SZ_D2_N
SZ_D4_P
SZ_D4_N
SZ_D6_P
SZ_D6_N
SZ_S16
SZ_S18
SZ_S20
SZ_S22
SZ_S24
SZ_S26
SZ_P2C_CLK_P
SZ_P2C_CLK_N
SZ_D1_P
SZ_D1_N
SZ_D3_P
SZ_D3_N
SZ_D5_P
SZ_D5_N
SZ_D7_P
SZ_D7_N
SZ_S17
SZ_S19
SZ_S21
SZ_S23
SZ_S25
SZ_S27
SZ_C2P_CLK_P
SZ_C2P_CLK_N
ETH_TXD0
ETH_TXD1
ETH_TX_EN
ETH_RXD0
ETH_RXD1
ETH_RXERR
ETH_RX_DV
ETH_MDIO
ETH_MDC
ETH_RSTN
ETH_REF_CLK
ETH_INT_RFCLKO
FPGA_MEM_RESET
FPGA_MEM_WP
FPGA_MEM_MISO
FPGA_MEM_MOSI
FPGA_MEM_CE
FPGA_MEM_SCK
FPGA_Top.sch
SYZYGY_Conn
SZ_SCL
SZ_SDA
SZ_D0_P
SZ_D0_N
SZ_D2_P
SZ_D2_N
SZ_D4_P
SZ_D4_N
SZ_D6_P
SZ_D6_N
SZ_S16
SZ_S18
SZ_S20
SZ_S22
SZ_S24
SZ_S26
SZ_P2C_CLK_P
SZ_P2C_CLK_N
SZ_D1_P
SZ_D1_N
SZ_D3_P
SZ_D3_N
SZ_D5_P
SZ_D5_N
SZ_D7_P
SZ_D7_N
SZ_S17
SZ_S19
SZ_S21
SZ_S23
SZ_S25
SZ_S27
SZ_C2P_CLK_P
SZ_C2P_CLK_N
SYZYGY Connector
SYZYGY_Conn.sch
Ethernet
ETH_TXD0
ETH_TXD1
ETH_TX_EN
ETH_RXD0
ETH_RXD1
ETH_RXERR
ETH_RX_DV
ETH_MDIO
ETH_MDC
ETH_RSTN
ETH_REF_CLK
ETH_INT_RFCLKO
Ethernet PHY
Ethernet.sch
FLASH
FPGA_MEM_RESET
FPGA_MEM_WP
FPGA_MEM_MISO
FPGA_MEM_MOSI
FPGA_MEM_CE
FPGA_MEM_SCK
FLASH
FLASH.sch
MJTP1138ATR
Reset Switch
S1
+3V3
RR1
10k
GND
Wake Switch
S2
RR2
10k
M50-3530442
J7
DNP
TP2
TP3
TP4
TP5
U1_JTAG_TCK
U1_JTAG_TDO
U1_JTAG_TMS
U1_JTAG_TDI
RISCV_3V3_EN
E310_MCU
FTDI_RESETn
BRD_RESET
RISCV_WAKE_N
RISC-V MCU
I2C_SDA
I2C_SCL
MCU_SPI_CS0
MCU_SPI_CS2
MCU_SPI_CS3
MCU_SPI_SCK
MCU_SPI_MOSI
MCU_SPI_MISO
MCU_GPIO_11
MCU_GPIO_12
MCU_GPIO_13
MCU_GPIO_18
MCU_GPIO_20
MCU_GPIO_23
UART0_TX
UART0_RX
E310_MCU.sch
PWB1
PWB
100-002
Oscilloscope Ground
TP1
5015
Place "GND" label
GND
Shield Digital Design
Schematic Notes:
All resistors are 0603, 1% unless otherwise stated
All capacitors are 0603, X5R or X7R ceramic unless otherwise stated
TODO: Modify such that all parts are rated for temp range from -40 to 85
fRISCY
FPGA + RISC-V Digital Processing Board
Top Level Schematic Sheet
Shield Digital Design
Stephen Newberry
(973) 552-8580
ShieldDigitalDesign.com
Stephen@ShieldDigitalDesign.com
Number: 200-002
File: RISCV_FPGA_Board.sch
Size: USLedger
Date: 2017-12-23
Rev: 1.1
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1
Sheet: 1/9

+3V3_RISCV_IO is switched from RISCV_3V3_EN

U1 FE310-G000

IS25LP128-JBLE U8

QSPI_DQ3 QSPI_DQ2 QSPI_DQ1 QSPI_DQ0 QSPI_CS0 QSPI_SCK

50Ω, 3W spacing

D11 BAT54 RISCV_WAKE_N

D12 BAT54 BRD_RESET

D10 1N4148W-TP

AON_LFCLK

FTDI_RESETn

RISCV_3V3_EN

I2C_SDA

I2C_SCL

U11 24AA256UIDT-I/SN

Silicon Serial Number
+MAC Address EEPROM

I2C Addr: 0b1010000 (0x50)

MCU_SPI_CS0 MCU_SPI_MOSI MCU_SPI_MISO MCU_SPI_SCK MCU_SPI_CS2 MCU_SPI_CS3 MCU_GPIO_11 MCU_GPIO_12 MCU_GPIO_13 UART0_RX UART0_TX MCU_GPIO_18 MCU_GPIO_20 MCU_GPIO_23

U1_JTAG_TCK U1_JTAG_TDO U1_JTAG_TMS U1_JTAG_TDI

16MHz Y1

PWR_FLAG

Low frequency clock

Y4 SIT1533AI-H4-DCC-32_768E

C80 0.1uF

APFA3010LSEEZGKQBKC D7

Edge mount LED
If = 2mA
Vf = [R: 1.8V, G: 2.65V, B: 2.65V]

RISC-V JTAG ESD Protection

D14 USBLC6-4SC6

fRISCY	**Shield Digital Design**
FPGA + RISC-V Digital Processing Board	Stephen Newberry
SiFive Freedom E310 RISC-V MCU	(973) 552-8580
	ShieldDigitalDesign.com
	Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: E310_MCU.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 2/9

Alternate power input

J5 53047-0210: +V_INPUT, PWR_FLAG, PWR_FLAG, GND

J3 10103594-0001LF (USB Micro-B): VBUS, D+, D-, ID, Shield, GND

+V_INPUT → PTC Fuse F1 (MF-MSMF250/16X-2)

USB_D_P, USB_D_N

Diff Pair, 90Ω, Max 150mils skew

R103 0 DNP

C15 1uF

Q1 DMG2305UX-13

U5A U5B BCM857BS,115

R4 10k, R2 47.5k

D1 SMBJ5.0A-E3/5B

C14 47uF

+5V, PWR_FLAG

USB ESD Protection

D15 USBLC6-2SC6: USB_D_N, GND, USB_D_P, +V_INPUT

Layout Notes:

Connect SNS at the output capacitor

Place 9 thermal GND vias in EP

U6 MIC23450

PVIN1 PVIN2 PVIN3 AVIN1 AVIN2 AVIN3 EN1 EN2 EN3 PG1 PG2 PG3 AGND1 AGND2 AGND3 PGND1 PGND2 PGND3 GND_EP

SW1 SW2 SW3 SNS1 SNS2 SNS3 FB1 1.2V FB2 1.8V FB3 3.3V NC

PG_1V0, PG_1V8, PG_3V3

R3 R6 R9 49.9

R12 R13 R14 10k

L1 1uH, L2 1uH, L3 1uH

R4 274k, R5 294k, R7 301k, R8 158k, R10 309k, R11 71.5k

C17 C18 C19 4.7uF

C20 C21 C22 0.1uF, C23 C24 C25 4.7uF

+1V2, +1V8, +3V3, PWR_FLAG

Power sequencing: 1.2V -> 1.8V -> 3.3V

SYZYGY Power:

VIO Buck Regulator: 5V in, 0.6 to 3.3V out, 2A maximum current draw

U13 AP3429AKTTR-G1: EN, GND, VIN, LX, FB

SZ_VIO_EN, +5V, GND

R72 100k, C76 22uF

L4 2.2uH

C77 22pF

R74 37.4k

C78 22uF, C79 22uF

+VIO, PWR_FLAG

U14 MCP4716A0T-E/CH: VREF, VDD, SCL, SDA, VOUT, VSS

SZ_SCL, SZ_SDA

R76 44.2k, R75 10k

Use DAC to set VIO voltage

See User Manual for more details

Output Voltage	DAC Code	DAC Voltage	True Output
3.3	18	0.05801	3.3026
2.5	312	1.00547	2.5009
1.8	569	1.83369	1.8001
1.2	789	2.54268	1.2002
0.9	899	2.89717	0.9002
0.6	1009	3.25166	0.6003

3V3 Load Switch for RISC-V IO Voltage

U4 SI3865DDV-T1-GE3: ON/OFF, R1/C1, R2, VIN, VOUT, VOUT

RISCV_3V3_END

R73 0

R71 100k, C75 1000pF

+3V3, +3V3_RISCV_IO, PWR_FLAG

Power supply LEDs

2Vf, 5mA

R18 604, D5 GREEN

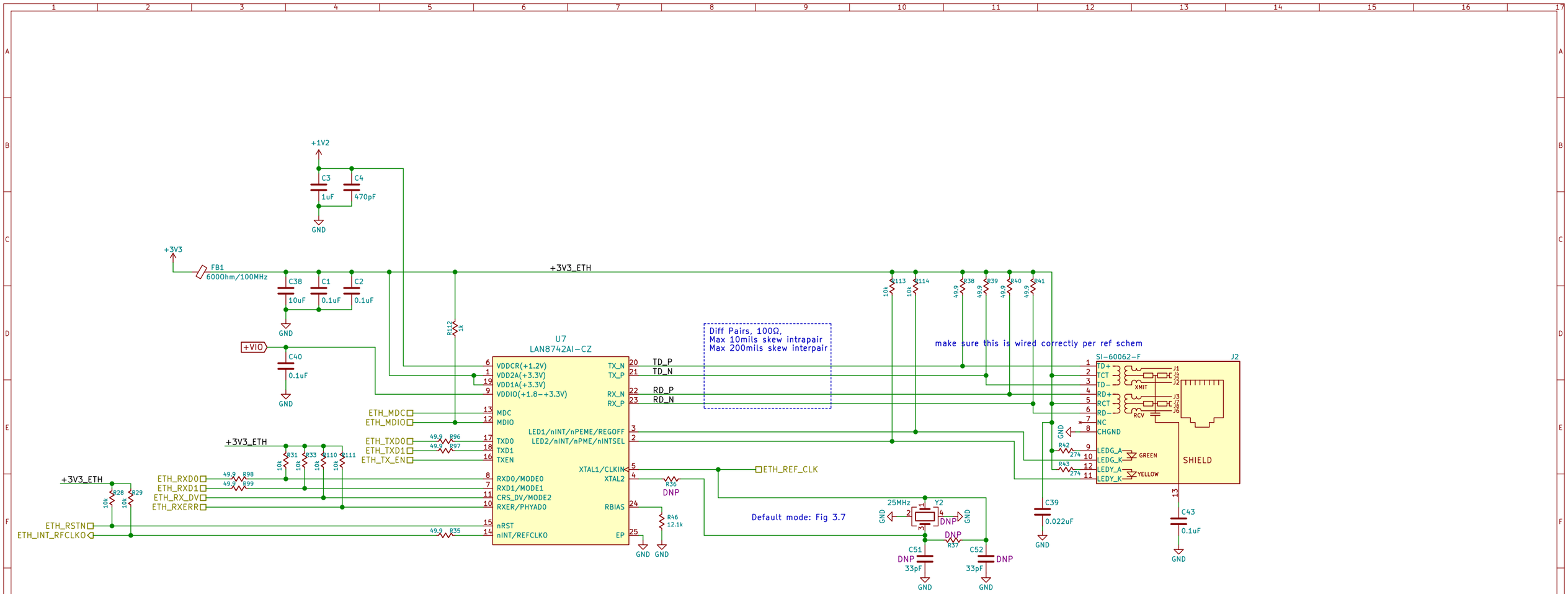
R15 604, D2 GREEN, Q2A 2N7002DW, PG_1V0

R16 604, D3 GREEN, Q2B 2N7002DW, PG_1V8

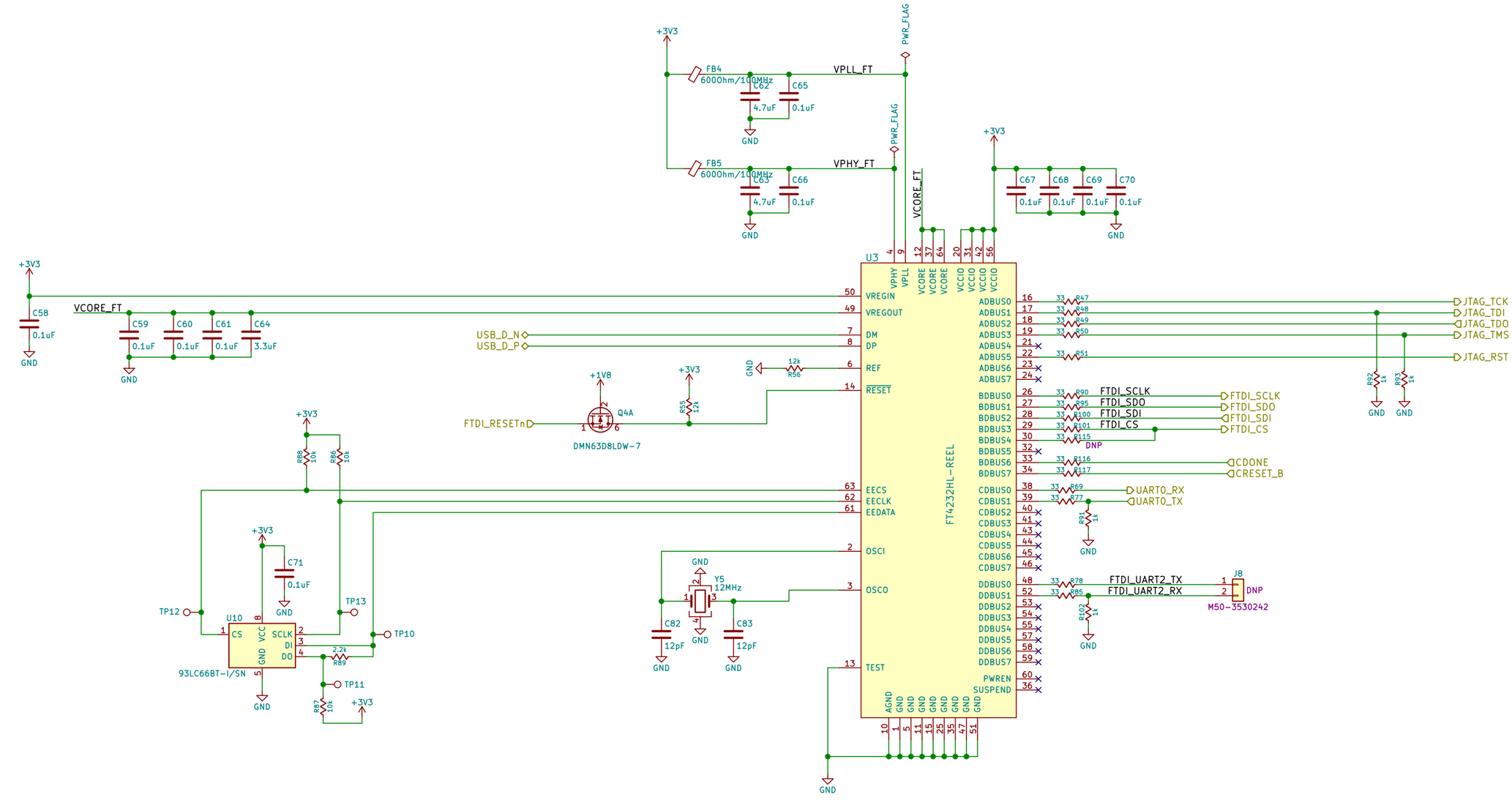
R17 604, D4 GREEN, Q3A 2N7002DW, PG_3V3

R70 261, D9 GREEN, +3V3_RISCV_IO

fRISCY	**Shield Digital Design**
FPGA + RISC-V Digital Processing Board	Stephen Newberry
Primary Power Circuitry	(973) 552-8580
	ShieldDigitalDesign.com
	Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: Power.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 3/9



fRISCY FPGA + RISC-V Digital Processing Board 10/100 Ethernet PHY	**Shield Digital Design** Stephen Newberry (973) 552-8580 ShieldDigitalDesign.com Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: Ethernet.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 4/9

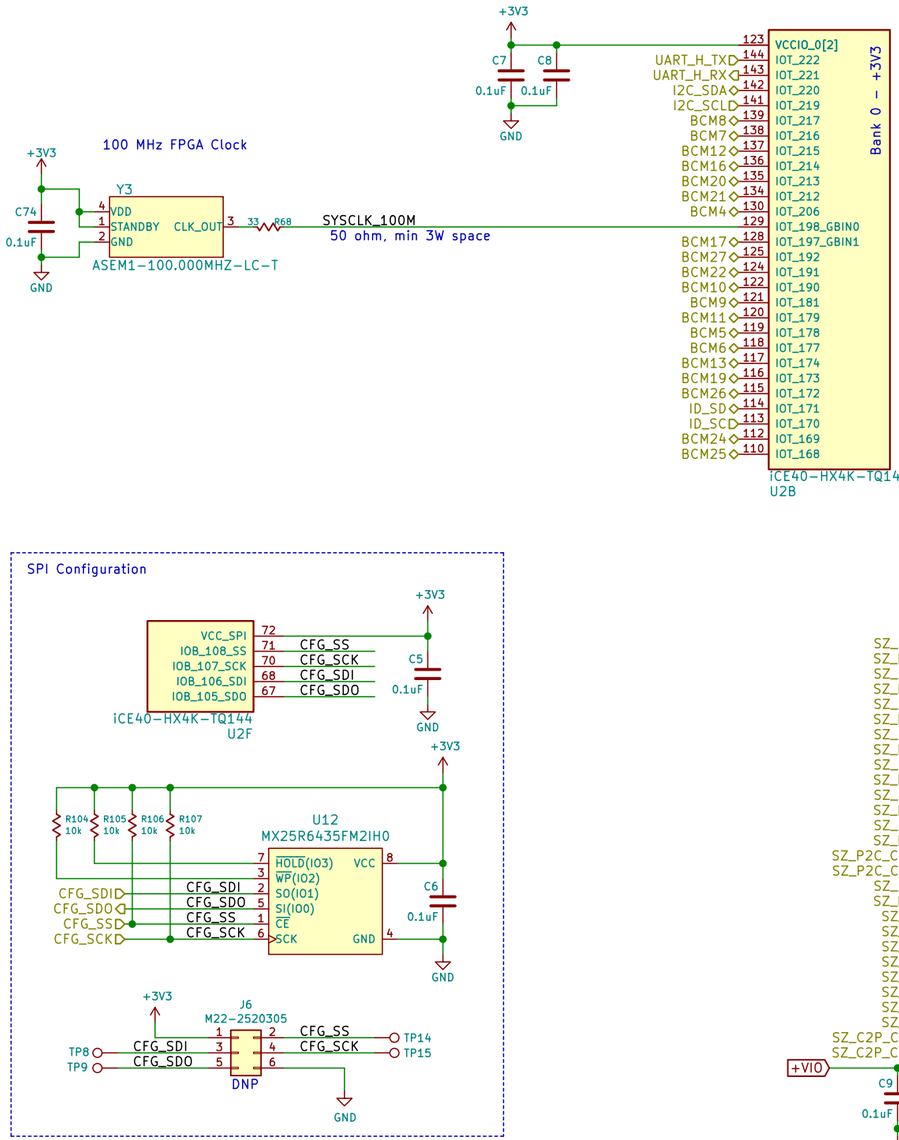


fRISCY FPGA + RISC-V Digital Processing Board FTDI USB to UART/JTAG	**Shield Digital Design** Stephen Newberry (973) 552-8580 ShieldDigitalDesign.com Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: FT2232.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 5/9

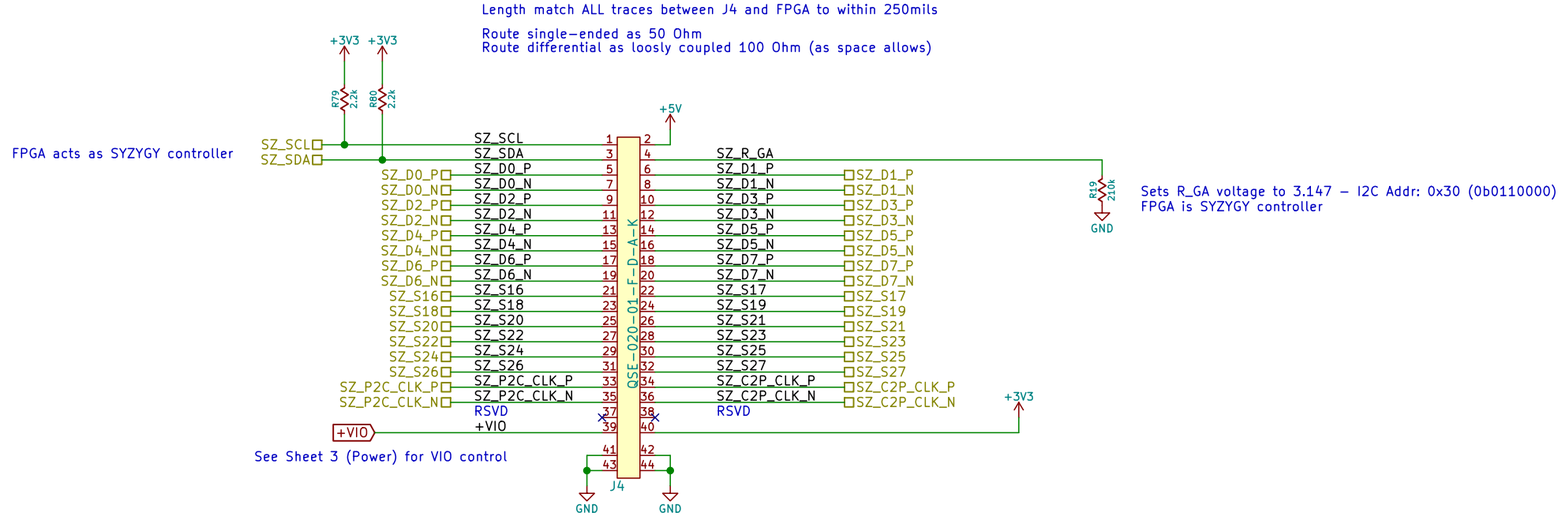
Pinout subject to change during layout

TODO:

go thru hardware checklist



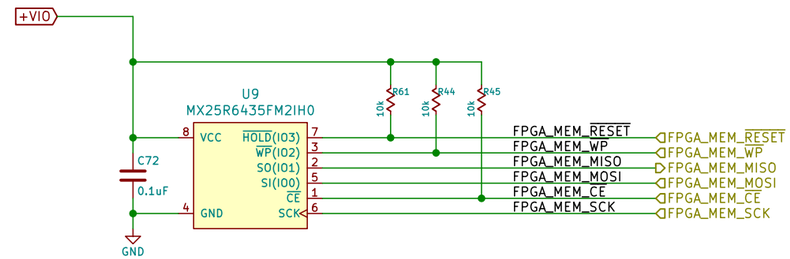
fRISCY	**Shield Digital Design**
FPGA + RISC-V Digital Processing Board	Stephen Newberry
Ice40 FPGA	(973) 552-8580
	ShieldDigitalDesign.com
	Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: FPGA_Top.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 6/9



fRISCY FPGA + RISC-V Digital Processing Board SYZYGY Connector	**Shield Digital Design** Stephen Newberry (973) 552-8580 ShieldDigitalDesign.com Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: SYZYGY_Conn.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 7/9

64Mb SPI Flash Memory

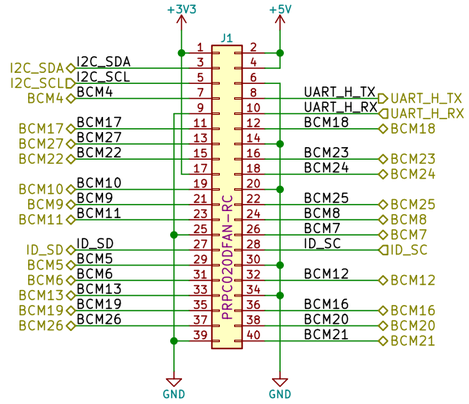
+VIO can range from 1.8V to 3.3V in general usage



Macronix uses RESETn on pin 7 rather than HOLDn

fRISCY FPGA + RISC-V Digital Processing Board NOR Flash	**Shield Digital Design** Stephen Newberry (973) 552-8580 ShieldDigitalDesign.com Stephen@ShieldDigitalDesign.com
Number: 200-002	
File: FLASH.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 8/9

40-pin, 0.1" pitch (MPN included for example, any will do)



All GPIOs to the FPGA
Only put I2C from RISC-V to the header (but share the both w/ FPGA)
Also share the ID I2C bus between RISC-V and FPGA

fRISCY FPGA + RISC-V Digital Processing Board 40-pin GPIO Header	**Shield Digital Design** Stephen Newberry (973) 552-8580 ShieldDigitalDesign.com Stephen@ShieldDigitalDesign.com
Number:	
File: GPIO_Header.sch	
Size: USLedger | Date: 2017-12-23	**Rev: 1.1**
KiCad E.D.A. kicad 5.0.0-rc1-44a33f262ubuntu17.10.1	Sheet: 9/9